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# Compact Modeling of Single Event Latchup of Integrated CMOS Circuit

A. Al Youssef, L. Artola, S. Ducret, G. Hubert

**Abstract** - This paper presents a compact model of latchup taking into account design and process dependence. The new approach is more realistic and inspired from the classical model. This model was used to confirm the single event latchup (SEL) robustness of D-Flip Flops (DFF) used in Readout Circuit of Infrared-sensors developed by Sofradir. SEL cross sections are presented by the mean of the monte Carlo tool MUSCA SEP3 in order to validate the new Latchup modeling approach.

**Index Terms**— SEE prediction, TCAD simulation, SPICE simulation, Single Event Latchup, compact modeling, cross section, design, CMOS

## I. INTRODUCTION

LATCHUP vulnerability in electronics devices used in spacecraft for space applications has become a real constraint since the 80's. For this, the development of SEL modeling was essential in order to study the latchup sensitivity of complementary metal oxide semiconductor (CMOS) gates and its evolution trend [1][2].

The latchup phenomenon is due to an inherent parasitic structure in the CMOS technology. This structure can be modeled electrically as a parasitic thyristor. In the literature, two electric modeling approaches of the latchup phenomenon were developed. The first one is based on a set of diodes and connected resistors [2]. This approach models the PNP structure as PN / NP diode junctions and the resistors which represent specific silicon volumes. The other latchup modeling approach is based on a modeling of the PNP structure as thyristor structure [1]. This classical electric approach is the most known for modeling latchup at present. The electric model of the latchup phenomenon consists in two bipolar transistors (NPN and PNP) associated and a set of resistors representing the different silicon regions in the CMOS inverter structure. This method is based on the calculation of all the external resistors from the electrical equations according to four characteristic of the Latchup: the triggering point ( $V_{trig}$ ,  $I_{trig}$ ), and the holding point ( $V_{hold}$ ,  $I_{hold}$ ). It is therefore necessary to have this key latchup characteristics to be able to calculate these resistors by technology computer aided design (TCAD) simulations [3][4] or by measurements as done in [5]. However, these works [1][3][5], the two models of bipolar transistors are the conventional bipolar junction transistor (BJT) models with assumptions of electrical characteristics of the parasitic bipolar transistor (such as the threshold voltage, order of

about 0.7V. The main weak point of such approach is that no real modeling of the intrinsic behavior of parasitic transistors is performed, and there its behavior can not takes into account design and process parameters.

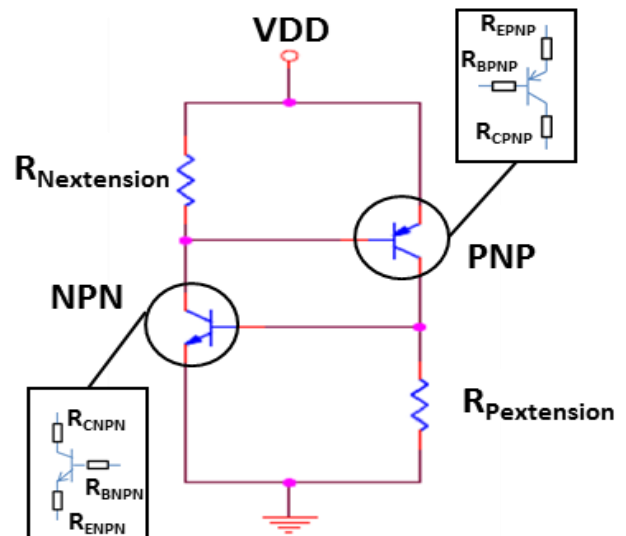
The goal of the paper is to present a new approach which proposes a more realistic compact model in order to be representative of latchup phenomenon. This approach also makes it possible to study the impact of the design and technological parameters on the Latchup sensitivity as it's not the case in the classical approach [1]. This compact model was used to confirm the SEL robustness of DFFs used in Readout Integrated Circuit (ROIC) of infrared image sensors developed by Sofradir. The SEL prediction was obtained by the mean of the Monte Carlo SEE tool MUSCA SEP3 [6] and the Transient ERROR Injection Framework for Integrated CMOS (TERRIFIC) devices [7] applied to the new compact model of Latchup.

The paper is organized in the following way: the details of the latchup modeling by compact electrical model are presented and discussed Section II. Then, the estimations of the single event latchup sensitivity of the standard D-Flip Flop (DFF) used by Sofradir in their ROIC, and the impact of the shrink of design dimensions are presented and discussed in Section III. Finally, conclusions are drawn in Section IV.

## II. LATCHUP MODELING BY COMPACT ELECTRICAL MODEL

### A. General presentation of the compact bipolar transistor modeling

The compact electric Latchup model was inspired from the same idea of classical electric model developed by Bruguier et al [1], but with a real modeling of bipolar transistors, as shown in Fig. 1.



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A. Al Youssef, L. Artola, G. Hubert, are with The French Aerospace Lab (ONERA), Toulouse, France (email: [ahmad.al\\_youssef@onera.fr](mailto:ahmad.al_youssef@onera.fr))

A. Al Youssef, S. Ducret, are with Sofradir Grenoble, France

Fig. 1: Simple presentation of Compact electric model of Latchup

The CMOS structures used in this study is a CMOS inverter whose the designs are issued a DFF used in a ROIC developed by Sofradir. Fig. 2 shows the 2-D calibrated TCAD structure of a 250 nm CMOS inverter issued from a DFF of the ROIC developed by Sofradir. The calibration of Sofradir CMOS inverter was presented in previous work [9]. The DFF design was presented in [10] and was widely investigated for the SEU point of view in previous work [8][9][10].

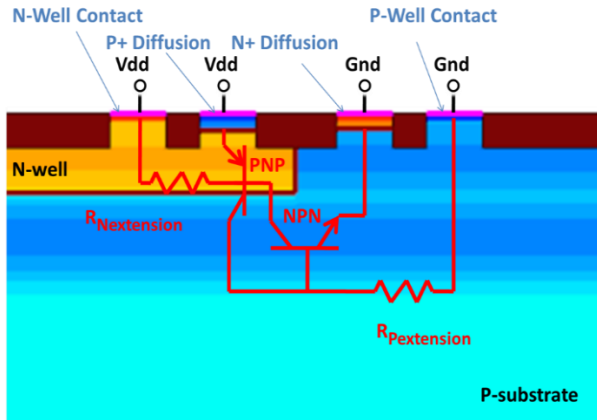


Fig. 2: 2D calibrated TCAD structure corresponding to CMOS inverter structure issued from a DFF of the ROIC developed by Sofradir

First of all, in this modeling approach, it was necessary to redefine the signification and the role of the six resistors in the classical electric model developed in [1].

In this way, the classic resistors  $R_{EW}$ ,  $R_{CS}$  and  $R_{BW}$  are respectively considered as the internal resistors of the PNP transistor: the emitter resistor  $R_{EPNP}$ , the collector resistor  $R_{CPNP}$  and base resistor  $R_{BNPN}$ . In the same way, the resistors  $R_{CW}$ ,  $R_{ES}$  and  $R_{BS}$  are respectively considered as internal resistors of the NPN transistor: the collector resistor  $R_{CNPN}$ , the emitter resistor  $R_{ENPN}$  and the base resistor  $R_{BNPN}$ .  $R_{CNPN}$  and  $R_{BNPN}$  are interconnected in N-well region as shown in Fig. 2. The silicon area in the N-well which represents the extension zone between the interconnected zone base-PNP/Collector-NPN and the top of N-well, is represented in this new modeling by the resistor  $R_{Nextension}$  as shown in Fig. 1. Thus, the sum of the resistors  $R_{Nextension}$ ,  $R_{BNPN}$  and  $R_{CNPN}$  must be equal to the resistor of N-well  $R_{N-well}$ . The resistors  $R_{BNPN}$  and  $R_{CPNP}$  are interconnected in the P-well region as presented in Fig. 1. The silicon area in the P-well which represents the extension zone between the interconnected zone base-NPN/collector-PNP and the top of P-well, is represented in this new modeling by  $R_{Pextension}$  as shown in Fig. 1. The sum of the resistors  $R_{Pextension}$ ,  $R_{BNPN}$  and  $R_{CPNP}$  must be equal to the resistor of the P-well  $R_{P-well}$ . Therefore, the compact Latchup electrical model shown in Fig. 1 consists in two bipolar transistors and two equivalent resistors,  $R_{Nextension}$  and  $R_{Pextension}$ , which represent the silicon volumes making the connection between the two bipolar transistors with the Top of the CMOS cell.

The first step was to develop the new compact modeling of bipolar transistors. This development was performed by the

mean of technology computer aided design (TCAD) and SPICE simulations. Then, the  $R_{Nextension}$  and  $R_{Pextension}$  resistors are involved to get the all elements of electrical Latchup modeling presented in Fig. 1.

### B. Development of the compact bipolar transistor modeling

It should be noted that the TCAD simulations are considered as reference in this approach [TCAD]. The presented validation corresponds to the output inverter of the DFF. The DFF was widely investigated for the SEU point of view in previous work [8][9][10]. The electrical behavior of the CMOS structure modeled by TCAD simulation was validated by the process design kit (PDK) used by Sofradir as done in previous work [9]. The physical TCAD simulation models used hydrodynamic simulation approach [9].

First, each bipolar transistor is modeled by TCAD simulation in a distinct way as shown in Fig. 3. TCAD simulations were performed in order to get the reference electric characteristic of each bipolar transistor. However, in order to keep a relevant representativeness of the CMOS structure, only the implant of the complementary bipolar transistor was removed. This allows for getting a realistic modeling of a compact model dedicated to the Latchup parasitic structure. Each bipolar parasitic transistor was characterized with build only its inherent structure as presented in Fig. 3. (a) and Fig. 3 (b) for the NPN and PNP transistor respectively. For the NPN transistor, as mentioned, the P-diffusion implant was removed from the complete structure of inverter. In the same way, PNP transistor was characterized without the N-diffusion implant. The goal of this step was to find the  $I_C/V_B$  characteristics of each bipolar transistor separately.

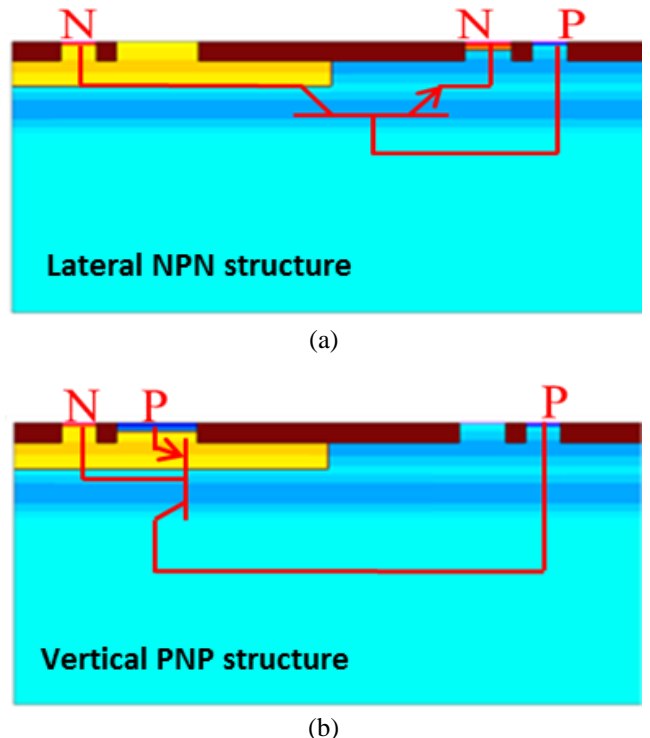


Fig. 3: Bipolar transistors built in TCAD simulation, (a) NPN transistor

structure (b) PNP transistor structure.

The  $I_C/V_B$  characteristics were obtained at the nominal voltage of the CMOS inverter of the DFF cell, i.e., 5V. The  $I_C/V_B$  characteristics are presented in red in Fig. 5.

Before going to perform the SPICE simulations of bipolar transistors and get their electrical characteristics, it was necessary to find the values of the internal resistors of each pole of bipolar transistors by TCAD simulations.

During the TCAD simulations, each pole of inherent bipolar transistors was modeled in 3D. For example, the N-well in Fig. 2 is the base of PNP transistor and in same time the collector of NPN transistor. Ohm's law was applied at the nominal voltage (5V) on N-well block in order to determine its resistance. Fig. 4 is an example of the structure used for the extraction of the resistance value of the N-well. Each pole resistor of bipolar transistors was extracted using Ohm's law calculation.

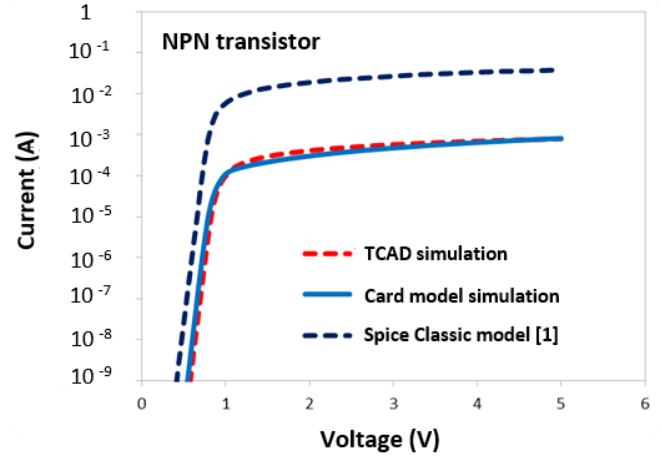


Fig.4: 2D TCAD structure used for the extraction of the N-well which corresponds to the  $R_{cnpn}$  of the compact bipolar transistor model.

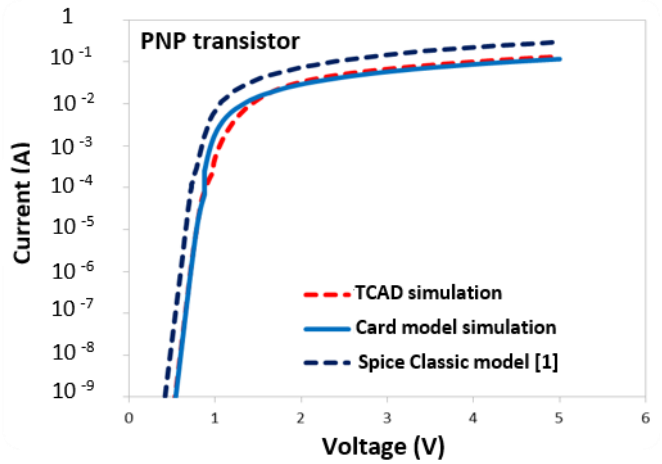
The second step in bipolar transistors modeling was based on the development of model card of each bipolar transistor by SPICE simulation. At this level, the model card in SPICE simulation of each bipolar transistor was updated by using all the internal resistors issued from the previous TCAD simulations. On the other hand, the optimization in the threshold voltage region is obtained by the update of the saturation currents of the different junctions of the parasitic transistors based on TCAD simulation extractions.

### C. Validation of the compact bipolar transistor modeling

In past, bipolar transistor model card In order to validate the new compact model of bipolar transistors, comparisons were performed. Fig. 5 (a) and Fig. 5 (b) shows respectively the  $I_C/V_B$  characteristics for the NPN and PNP transistor obtained by TCAD simulations (red dashed-line), by SPICE simulations of the compact model card (blue line) and obtained by SPICE simulation of standard BJT model [1] (blue dashed-line). In order to perform a fair comparison, the standard (classic) BJT model card was calibrated in order to be representative the design specificities of the CMOS inverter.



(a)



(b)

Fig. 5 :  $I_C/V_B$  characteristics of bipolar transistors, TCAD curves are plotted in red dashed-lines and two SPICE curves, curves dressed in blue lines represent SPICE simulations with Card model developed and the curves plotted in blue dashed-lines represent the classic card models (a) TCAD and SPICE curves of NPN transistor (b) TCAD and SPICE curves of PNP transistor

The comparison shows a very good correlation of the new compact model of bipolar transistor with the reference TCAD simulations. Moreover, the comparison with classic model (blue dashed line) highlights the improvement of the modeling and the interest of the presented work. The improvement of the modeling is more significative for the NPN transistor than the PNP transistor.

### D. Validation of the Latchup modeling

The final step of this modeling approach was to build the complete compact electric Latchup model (Fig. 1) consisting in the two bipolar transistors (presented in II.B) and the two equivalent resistors  $R_{Nextension}$  and  $R_{Pextension}$  presented in section II.A. During this step, a specific work was carried out to determine the distribution of these resistors (equation 1 and equation 2) in order to obtain a good correlation between the Latchup characteristic modeled by the SPICE simulations and the Latchup characteristic obtained by the TCAD simulations.

$$R_{N-well} = R_{Nextension} + R_{BPNP} + R_{CNPN} \quad (1)$$

$$R_{P\text{-well}} = R_{P\text{extension}} + R_{BNPN} + R_{CPNP} \quad (2)$$

Fig. 6 shows the latchup characteristic of each bipolar transistor obtained by TCAD simulation (red dashed-line), by SPICE simulation of the compact Latchup electrical model (blue line) and the classical modeling [1] (blue dashed line). As previously, in order to perform a fair comparison, the classic spice model (BJT and resistances) was calibrated in order to be representative the design specificities of the CMOS inverter.

The comparison shows that the compact Latchup model is in good agreement with the TCAD reference simulation as well in terms of latchup metrics ( $V_{trig}$ ,  $I_{trig}$ ,  $V_{hold}$ ,  $I_{hold}$ ) but also in term of shape. This comparison shows the pertinence of compact Latchup modeling. The estimation of the latchup metrics is strongly improved in comparison to standard spice models.

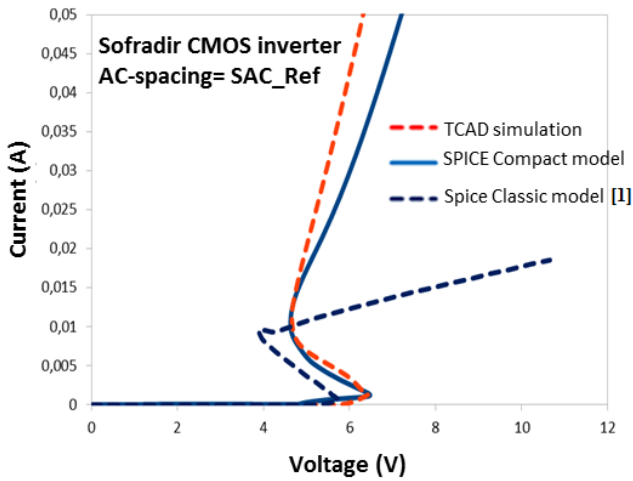


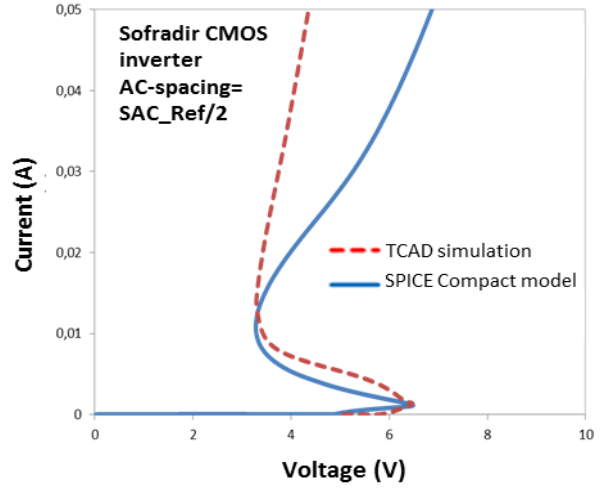
Fig. 6: Comparison of compact SPICE model, classical SPICE and TCAD simulation of Sofradir CMOS inverter reference structure.

For a quantitative point of view, the new compact model has a relative deviation from the TCAD data lower than 1% for the four latchup metrics while for the standard spice model, the relative deviation for the  $V_{trig}$ ,  $I_{trig}$ ,  $V_{hold}$ ,  $I_{hold}$  are 11%, 62%, 16%, 11% respectively.

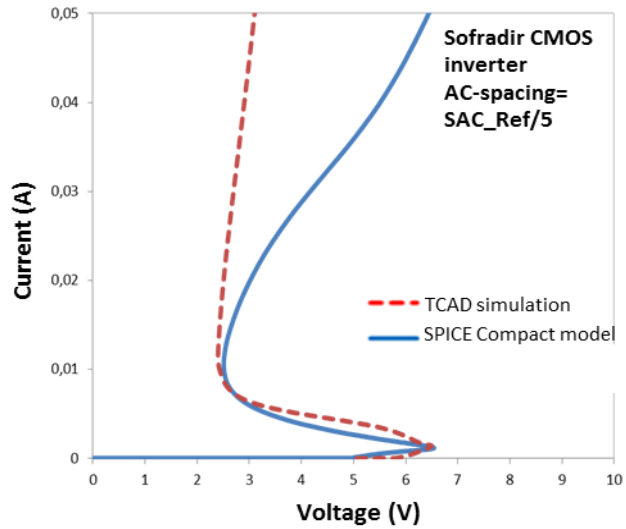
An important point of the proposed work, is the capability of the compact latchup model to taken into account the effects of the design. An example is presented for the parameter AC-spacing (SAC). The SAC is the distance between n-MOS transistor and p-MOS transistor in CMOS inverter structure. The increase in the SAC is known to improve the robustness to SEL of CMOS cell [9][5]. From an electrical point of view, the reduction of SAC distance leads to a modification of the N and P-well resistors. These two resistors are characterized in the card model of one of the bipolar transistors PNP or NPN. For confidential reasons, the reference value of the SAC is not provided.

The comparison of I/V characteristics obtained by compact modeling and TCAD simulation is presented for two values of SAC: SAC/2 and SAC/5. For fairness reasons, the spice classic model is not compared. As mentioned this model is not able to take into account the design/process parameters. The corresponding I/V characteristics are presented in Fig. 7

(a) and Fig. 7 (b).



(a)



(b)

Fig. 7: Comparison of I/V characteristics from issue TCAD simulations (red dashed line) and latchup compact model (blue line) of the CMOS Inverter Structure with two values of SAC: (a) SAC = SAC\_ref / 2 and (b) SAC = SAC\_ref / 5. The CMOS inverter designs are issued from a DFF used in a ROIC developed by Sofradir.

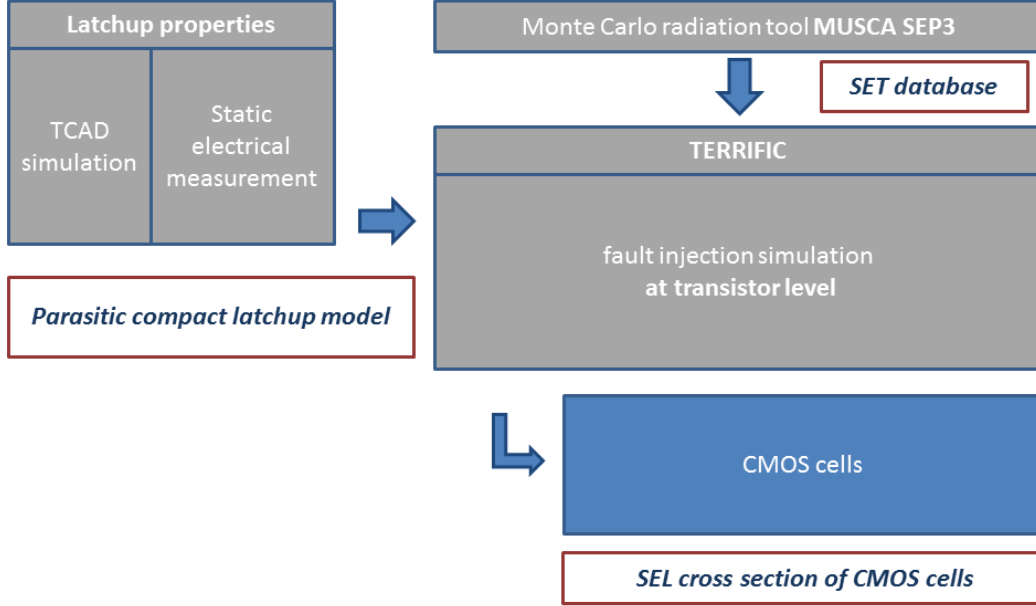


Fig. 8: Global overview of SEL modeling based on Monte Carlo radiation tool, MUSCA SEP3 coupled with fault injection simulations at transistor level performed by TERRIFIC using the parasitic compact latchup model.

The two figures highlight the robustness of the compact modeling to take into account the effect of the SAC as well in terms of shape as and in terms of Latchup key characteristics (the trigger point and the hold point).

The next section presents an application of compact modeling in order to determine the single event latchup sensitivity under heavy ions with according to different design configurations of Sofradir CMOS inverter used in D-Flip-Flop of a ROIC developed by Sofradir for their Infrared Image Sensor.

### III. SINGLE EVENT LATCHUP ESTIMATION OF DFF USED IN ROIC FROM SOFRADIR

In order to valorize this relevance of the compact modeling of Latchup, the Monte Carlo SEE prediction tool, MUSCA SEP3 [11][6], coupled with the injection platform TERRIFIC [7] were used to determine the occurrence or not of the SEL as summarized in Fig. 8.

First, MUSCA SEP3 was used to generate a realistic SET database (in term of amplitude and duration) as a function of radiation constraint (in terms of heavy ion location and linear energy transfer (LET)). The shapes of the SET currents are based on 3D analytical models of the transport and collection mechanisms of generated charges in the silicon. These models were validated in previous works and take into account the following mechanisms: ambipolar diffusion, dynamic collection, multi-collection bipolar amplification, recombination, bias dependence, and temperature dependence. The complete description of the tool was presented in previous works [6]. The SET currents were calculated for the sources of n-MOS and p-MOS transistors connected to the supply voltage of the DFF. While,

TERRIFIC was allowed injecting the source SET databases in the SEL compact model presented previously.

Fig. 9 shows the SEL cross-section of the CMOS inverter as a function of the SAC distance for a heavy ion with a LET of about  $100 \text{ MeV.cm}^2.\text{mg}^{-1}$ . This very high LET value was simulated due to the intrinsic robustness of Sofradir design and technology. The cross-section trend shows an increase in the SEL sensitivity with a decrease in the SAC distance. No Latchup event was observed for the reference value of SAC of the CMOS (SAC\_ref). This immunity is depicted by an arrow to the down, and was validated by new SEL tests campaign at University Catholic of Louvain (UCL) with LET up to  $62 \text{ MeV.cm}^2.\text{mg}^{-1}$ . The trend confirms the results already observed by TCAD simulations in this work and previous works [9].

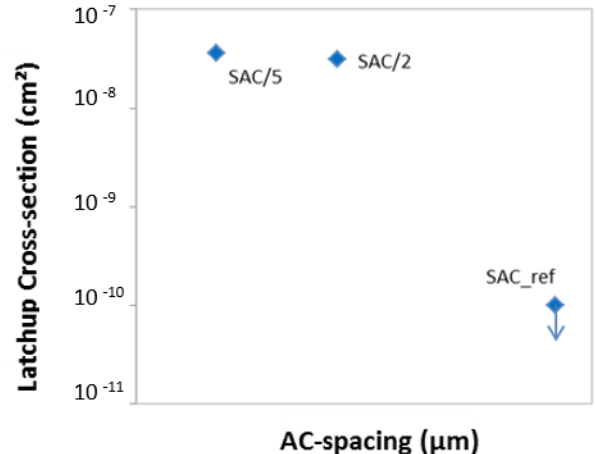


Fig. 9: SEL cross section as a function of SAC width of the inverter in the DFF at room temperature induced by heavy ions with a LET of about  $100 \text{ MeV.cm}^2.\text{mg}^{-1}$ .

In order to have a more general view of the SEL sensitivity, Fig. 10 shows the global SEL cross-section as a function of LET for the three values of SAC width (SAC\_ref, SAC / 2 and SAC/5). As expected, the SEL cross-section increases with the increase in LETs. This is entirely consistent with what exists in the literature [3][5]. Compact modeling is used to investigate the impact of a shrink of the DFF design on the Latchup sensitivity. The reference structure of Sofradir (SAC\_ref) was tested under heavy ion beam at 67 MeV.cm<sup>2</sup>.mg<sup>-1</sup> at UCL in Belgium and it was demonstrated a Latchup immunity of Sofradir technology [9]. This confirms the relevance of the SEL modeling presented in this work. However, the simulation results demonstrate that a shrink of the n-MOS to p-MOS distance below or equal to a factor 2 must induce a strong increase in the SEL susceptibility of the DFF.

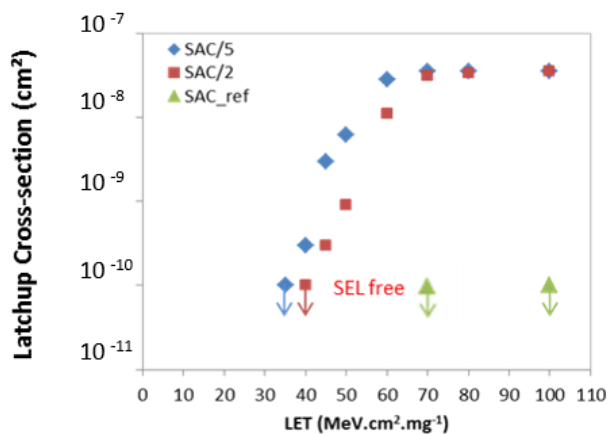


Fig. 10: The SEL cross-section of CMOS inverter for various SAC values: reference value (green triangles), SAC / 2 (red squares) and SAC / 5 (blue diamonds)

#### IV. CONCLUSIONS

In this paper, a new compact modeling approach to the Latchup phenomenon was presented. This compact modeling was validated at three levels: transistor level by PDK simulation, at compact level by electrical stress TCAD and at device level by heavy ion tests. This modeling approach has shown its effectiveness in representing Latchup key points, trigger point and Latchup hold point. The Latchup sensitivity study was performed with an application case of the Sofradir design and technology. Moreover, this work has shown in relevance to take into account the design effects on the SEL sensitivity. This point was presented for the AC-spacing parameter. The results confirmed the Latchup sensitivity trend in terms of SAC distance effect and the relevance of such a modeling approach to provide design optimization support to Sodrafir's ROIC development team. This method offers a more realistic modeling of the parasitic latchup structure induced by the CMOS technology. This approach is able to study the Latchup sensitivity for any technology and go up to the estimation of the SEL cross sections while considering the risk of the events non-destructive such as SET

or SEU.

#### REFERENCES

- [1] G. Bruguier, J.M. Palau, "Single particle induced latchup," IEEE Trans. Nucl. Sci., vol. 43, no. 2, pp. 522–532, Apr. 1996.
- [2] L. Ye, et al., Proc. IEEE 8th International Conference on ASIC, Hunan (China) 2009, (pp.1035-1038).
- [3] L. Artola, G. Hubert, T. Rousselin, "Single-Event Latchup Modeling Based on Coupled Physical and Electrical Transient Simulations in CMOS Technology," IEEE Trans. Nucl. Sci., vol. 61, no. 6, pp. 3543–3549, Dec. 2014.
- [4] Synopsys (Former ISE) TCAD Manual, USA, CA, Mountain View:Synopsys, 2016.
- [5] L. Artola, N. J.-H. Roche, G. Hubert, A. Al Youssef, A. Khachatryan, P. McMarr, H. Hughes, "Analysis of Angular Dependence of Single-Event Latchup Sensitivity for Heavy-Ion Irradiations of 0.18- $\mu$ m CMOS Technology," IEEE Trans. Nucl. Sci., vol. 62, no. 6, pp. 2539 – 2546, Dec. 2015.
- [6] G. Hubert, and L. Artola, "Single-event transient modeling in a 65-nm bulk CMOS technology based on multi-physical approach and electrical simulations," IEEE trans. Nucl. Sci., vol.60,no.6,pp. 4421–4429, Dec. 2013.
- [7] L. Artola, S. Ducret, F. Advent, G. Hubert, J. Mekki, "SEFI Modeling in Readout Integrated Circuit induced by Heavy Ions at Cryogenic Temperatures," Accepted for IEEE NSREC 2018 and under review for IEEE TNS.
- [8] L. Artola, G. Hubert ; O. Gilard ; S. Ducret ; F. Perrier ; M. Boutillier ; P. Garcia ; G. Vignon ; B. Baradat ; Nicolas Ricard, "Single Event Upset Sensitivity of D-Flip Flop of Infrared Image Sensors for Low Temperature Applications Down to 77 K," IEEE Trans. Nucl. Sci., vol. 62, no. 6, pp. 2979 – 2987, Dec. 2015.
- [9] A. Al Youssef, et al. "Investigation of Electrical Latchup and SEL Mechanisms at Low Temperature for Applications Down to 50 K, ", IEEE Trans. Nucl. Sci., vol. 64, no. 8, pp. 2089-2097, Aug. 2017.
- [10] L. Artola, A. Al Youssef, S. Ducret, Franck Perrier, R. Buiron, O. Gilard, J. Mekki, M. Boutillier, G. Hubert, and Christian Poivey"Update of Single Event Effects Radiation Hardness Assurance of Readout Integrated Circuit of Infrared Image Sensors at Cryogenic Temperature," MDPI, Sensors, vol. 18, no. 7, pp. 2338-2350, Jul 2018.
- [11] G. Hubert, S. Duzellier, C. Inguibert, C. Boatella-Polo, F. Bezerra, R. Ecoffet, "Operational SER Calculations on the SAC-C Orbit Using the Multi-Scales Single Event Phenomena Predictive Platform (MUSCA SEP3)," IEEE Trans. Nucl. Sci., vol. 56, no. 6, pp. 3032-3042, Dec. 2009.