Analysis of the Single-Event Latch-up Cross Section of a 16nm FinFET System-on-Chip using Backside Single-Photon Absorption Laser Testing and Correlation with Heavy Ion Data

M. Fongral, Vincent Pouget, F. Saigne, M. Ruffenach, J. Carron, F. Malou, J. Mekki

Analysis of the Single-Event Latch-up Cross Section of a 16nm FinFET System-on-Chip using Backside Single-Photon Absorption Laser Testing and Correlation with Heavy Ion Data

M. Fongral, V. Pouget, F. Saigne, M. Ruffenach, J. Carron, F. Malou, J. Mekki

***Abstract*—The single-event latch-up (SEL) cross section of a 16nm bulk finFET programmable system-on-chip (SoC) is investigated by combining single photon absorption (SPA) laser testing, emission microscopy and embedded instrumentation. The contributions of different SEL-sensitive areas identified by their current increase, light emission and functional signatures are measured. The effect of temperature and IO bias is evaluated. The laser results show an excellent correlation with heavy ion data, and delimit the origin of SEL in this device by excluding the occurrence of SEL in the core-logic for this technology.**

***Index Terms*—Single-Event Latch-up, bulk finFET, System-on-Chip, pulsed laser testing.**

I. INTRODUCTION

Single-event latch-up (SEL) is a well-known threat for complementary metal oxide semi-conductor (CMOS) devices exposed to radiation, which consists in the triggering in low impedance state of a parasitic thyristor p-n-p-n structure inherent to CMOS technologies that can lead to the destruction of the device [1-6]. While the most recent CMOS technologies have evolved from planar to fin field-effect transistors (finFET), the SEL phenomenon remains a major concern and has been studied and observed in finFET technologies both with technology computer-aided design (TCAD) simulations and experimentally in 16nm [7-11] and 7nm devices [12, 13]. The question whether SEL can occur in the core-logic in such devices is important because the answer can dramatically impact the SEL cross section and the required effort for designing latch-up-free circuits with those technologies. Unfortunately, classical heavy ion testing usually does not allow determination of whether an SEL is generated within the core-logic or in peripheral blocks of a device under test (DUT). Indeed, SEL testing typically consists in monitoring the supply current while the DUT is exposed to a particle beam to detect a transition to a high-current state that is the signature of the occurrence of an SEL. Note that the electrical test setup becomes more challenging with complex systems-on-chip (SoC) that have multiple voltage supply inputs and dynamic variations in the supply current of each input related to the device activity.

Laser testing is an interesting complementary technique in order to spatially locate the origin of single-event effects within a device [14]. Backside testing through the substrate using either single-photon absorption (SPA) [15] or two-photon absorption (TPA) [16] has been shown to provide interesting and quantifiable results regarding SEL [17-26].

In this work, we use single-photon absorption (SPA) laser testing to investigate the SEL susceptibility of a 16nm finFET commercial programmable SoC that is known for being sensitive to SEL under heavy ions [7-9]. An efficient test method is developed that associates a simple electrical setup and self-testing instrumentation of the DUT using embedded software and IPs. We present SEL mappings of different regions of the DUT. The regions where SEL is triggered are confirmed by in-line light emission microscopy [27-29] and their functions are clearly identified from the fault signatures related to the SEL events. The good correlation of the measured laser cross section with heavy ion data confirms that all sensitive regions were identified, and located in specific blocks of the device.

II. EXPERIMENTAL SETUP & METHOD

An overview of the experimental setup is presented in Fig. 1.

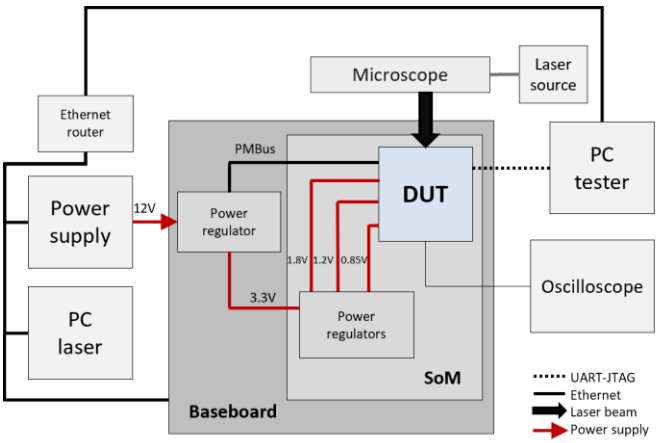

Fig. 1. Experimental setup for laser testing.

A. Device under test

The DUT is a Xilinx Zynq Ultrascale+ (XCZU3EG) device fabricated in TSMC's 16nm bulk finFET process. This SoC embeds four application processing units (APU) and two real-time processing units (RPU) forming the processing system (PS) section of the die and an array of configurable logic blocks forming the programmable logic (PL) section. It also includes different types of interfaces and input/output ports (IOs) in a large monolithic die of 91mm².

The DUT is part of a commercial system-on-module (SoM)

Manuscript received October 9, 2023.
This work was supported in part by the Region Occitanie and the CNES.
M. Fongral, V. Pouget, F. Saigne are with the Institut d'Electronique et des Systemes (IES), University of Montpellier, CNRS (UMR5214), Montpellier, France.
M. Ruffenach, J. Carron, F. Malou, J. Mekki are with the Centre National d'Etudes Spatiales (CNES), Toulouse, France.

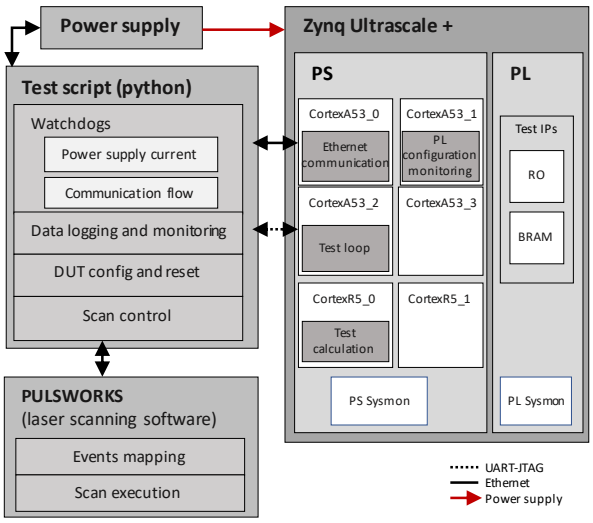

Fig. 2. Architecture of the software testbench.

that provides all the required immediate environment for operating the device, including power regulators and memory components. The SoM is mounted on a commercial base-board that provides the SoM 3.3V power supply from its 12V power input as presented in Fig. 1.

Because the DUT package is a lid-less flip-chip ball-grid array, providing direct access to the backside of the silicon die, the backside surface only had to be polished to optical quality to be compatible with backside laser testing, with a remaining substrate thickness of 700µm.

B. Electrical test setup

Power regulators on the SoM generate the three supply voltages (0.85, 1.2 and 1.8V) required by the DUT. The IO banks are supplied with 1.8V. For detecting SEL, monitoring of the power supply currents is performed externally at the level of the base-board 12V supply and by the DUT itself polling the base-board 3.3V regulator for its total current via PMBus. The lower voltages power lines on the SoM are not monitored individually, but internal voltages are retrieved within the DUT by system monitor (Sysmon) units in the PS and PL sections. This setup was found to provide sufficient observability for all the events of interest while not requiring any harware modification of the commercial boards.

C. Software test-bench and methodology

Fig. 2 presents the principles of the software testbench used for our experiments. The DUT is instrumented with IPs and embedded software to provide dynamic observability on the device functions. One APU core of the PS is in charge of executing the main test loop, while another core is dedicated to the monitoring of the PL configuration by scrubbing through the ICAP interface and a third core devoted to data output through TCP/ethernet. One RPU core performs a simple calculation and its monitoring is part of the main test loop. In the PL, 24 ring oscillators of configurable length are implemented and their frequency is periodically captured by the test loop. 16 BRAM blocks are also instanciated and tested. The PL activity can thus be dynamically controlled, providing the possibility to modulate the temperature of the chip in a range of approximately 20°C.

The experiment is controlled by a Python script that monitors the supply current as well as the data sent by the DUT. When an abnormal condition is detected by the watchdog threads, including a current higher than a defined threshold, the script pauses the laser scanning software while a power-on reset (POR) of the device is performed. An adjustable delay of at least 100ms between the detection of an SEL and the POR execution allows to capture the functional impact of SEL events.

Laser tests are performed with the single-photon absorption (SPA) laser system of the IES Preserve facility, with a wavelength of 1064nm, a pulse duration of 30ps, and a spot size of 1.1µm. The typical scanning step used in this work is between 1 and 2µm (depending on the zone) on both axis, and the laser pulse triggering frequency never exceeded 5Hz. Unless otherwise specified, all the results presented below were obtained for a stabilized DUT temperature of 64°C, as measured by the PL and PS Sysmon, and all energy threshold measurements are performed with a resolution of 7pJ.

Considering the large area of the DUT, the repetition of structures like configurable logic blocks (CLB) and IOs was used to reduce scanned zones to a representative fraction of the device. Measurements of sensitive areas were then extrapolated to the whole chip by multiplying by the number of repetition of each structure.

III. EXPERIMENTAL RESULTS

Fig. 3 presents an overview of the SEL sensitive functions identified in the DUT, with letters referring to a representative selection of scanned zones presented in details in the following. The blocks in blue correspond to functions that could be easily identified by their position and repetition from the publicly available information for this chip.

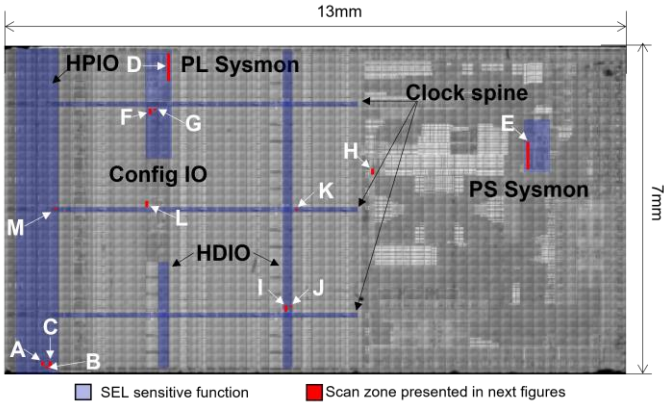

Fig. 3. Overview of the SEL sensitive blocks (in blue) on a backside infrared image of the chip.

Fig. 4 summarizes the measured laser energy thresholds for SEL triggering and the observed SEL current amplitudes for each zone. The dispersion of the measured current amplitudes within each zone was less than 10%, so Fig. 4 presents the average amplitudes for each zone. One can note the diversity of current levels for the different zones, with the smaller currents

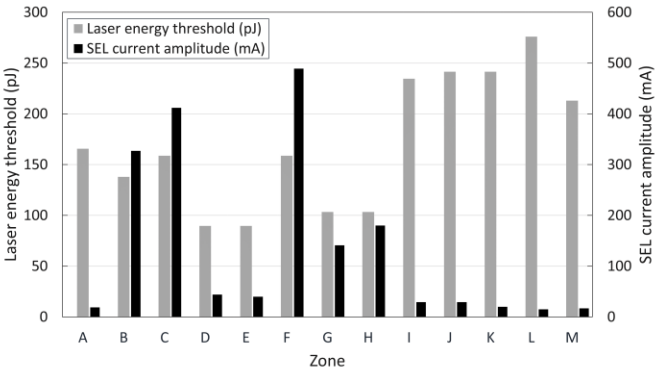

Fig. 4. SEL laser energy thresholds and current amplitudes measured at board level on the 12V power supply for the different zones identified in Fig. 3.

being mostly associated to high energy thresholds. The lowest energy threshold is observed for the Sysmon zones (D and E), while the highest established SEL current is observed in the "Config IO" region (zone F).

A. SEL sensitive regions

Various topologies of SEL sensitivity were identified during the experiments. Fig. 5 presents a set of SEL mappings obtained with the same incident pulse energy of 552pJ for zones A, B and C located in the high-performance IO (HPIO) banks, zones D and E related to PL & PS Sysmon, respectively, zones I and J related to high density IOs (HDIO), and zones L and M spotted three times in unidentified functions. Structures in

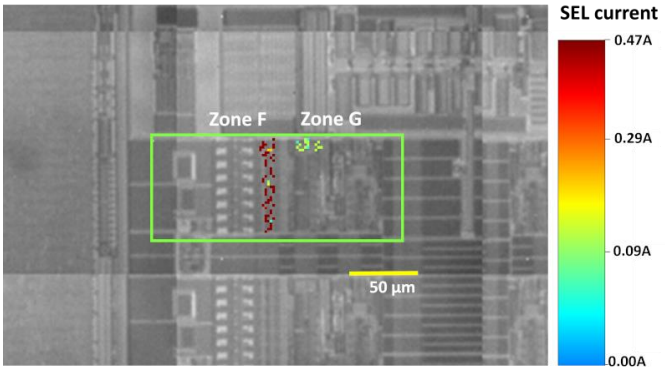

Fig. 6. SEL mapping in the Config IO region.

zones A, B and C are visibly repeated over the full width of the chip. Zone A presents four relatively small sensitive structures of a few square micrometers, for which SEL can be triggered individually, while zone C presents a single massive sensitive region. One can also note that the PL and PS Sysmon zones D and E present similar but vertically-flipped massive distributions of sensitivity, while the zones I, J, L and M present more localized points of sensitivity that could probably be related to specific locations in the layout. HDIO zones (I and J) have an energy threshold 50% higher than HPIO bank zones.

Fig. 6 presents SEL mapping for an incident energy of 276pJ of zones F and G associated with Config IO resources. One can note using the color scale that the current increase is higher for zone F, as shown previously in Fig. 4. When triggering latch-

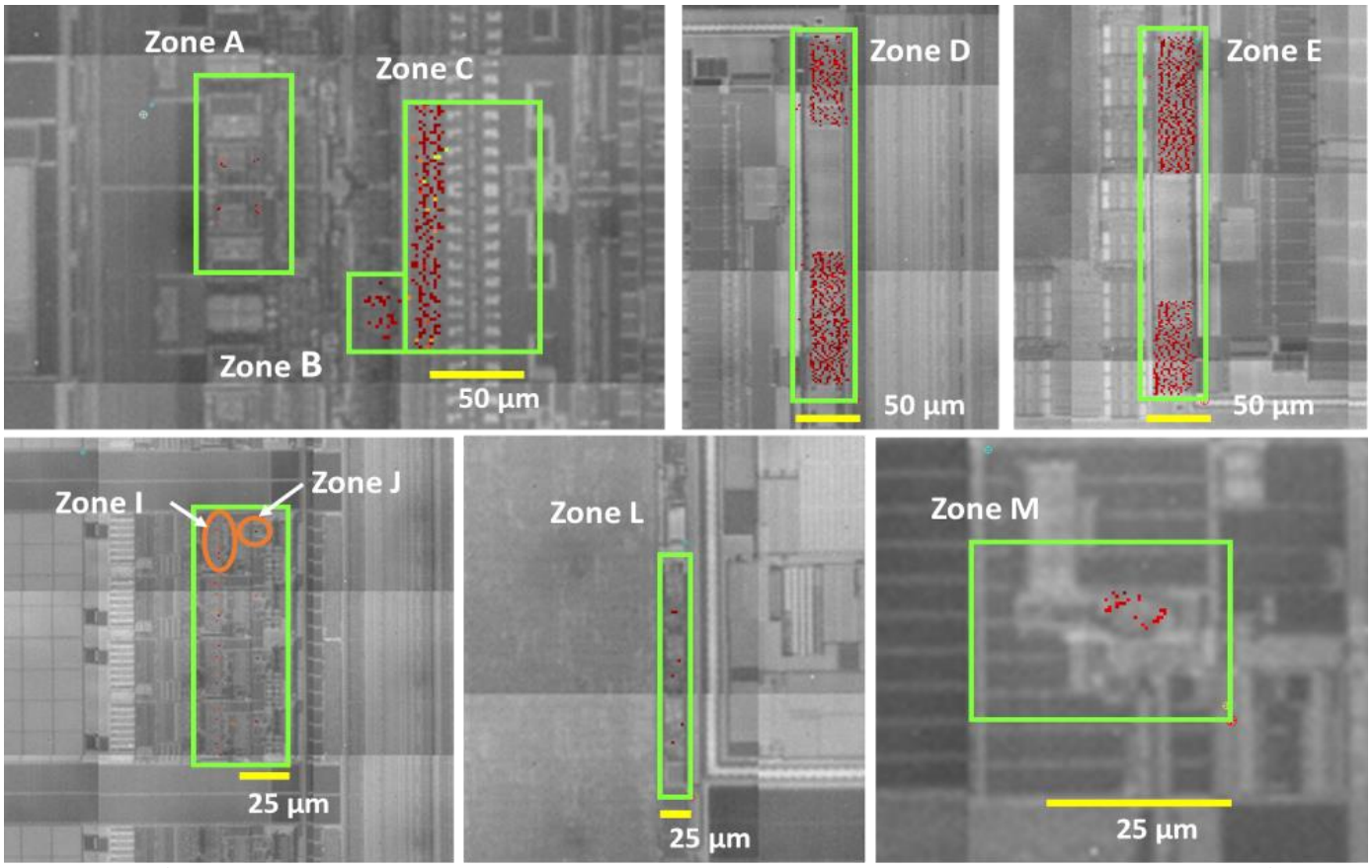

Fig. 5. Selection of scanned zones (green rectangles) and corresponding SEL mapping (red pixels) superimposed with a backside microphotography of the device.

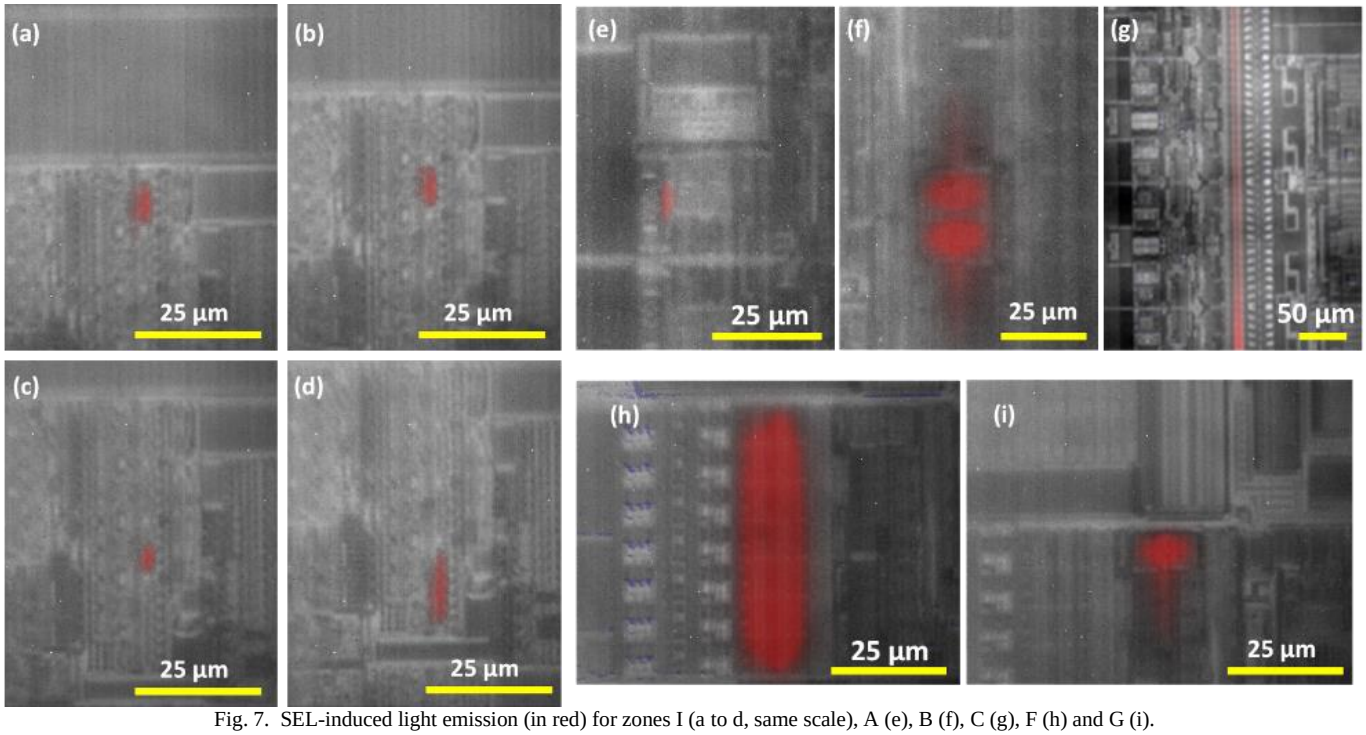

Fig. 7. SEL-induced light emission (in red) for zones I (a to d, same scale), A (e), B (f), C (g), F (h) and G (i).

up in zones F and G, small voltage drops could be measured by the Sysmon PL on VCCAUX PL, from the initial 1.8V down to 1.75V and 1.78V respectively for zones F and G.

B. SEL-induced light emission observations

Emission microscopy (EMMI) is a technique that consists in capturing the photons produced by the radiative recombination of charge carriers that naturally occurs especially in the junctions of CMOS technologies, where the level of light emission is related to the current density in the junction [27-29]. Light emission associated to the SEL high current densities was captured in-line by the infrared camera of the microscope for each SEL triggered. Such images confirm that the current increases that are measured externally are correlated to the apparition of localized high current densities within the device. Thus, they confirm the latch-up nature of the events and exclude other mechanisms that could produce a current increase like upsets in the device logic configuration that would induce bus contention or clock frequency changes. These images also provide an indication on the current paths involved in the SEL for each zone, or at least the extension of the well-substrate junction part of the parasitic thyristor responsible for the latch-up. For the DUT in this work, in-line EMMI was found to be a reliable way of detecting or confirming the occurrence of an SEL when the measured current increase was of the same order of magnitude as the chip activity-related current variations.

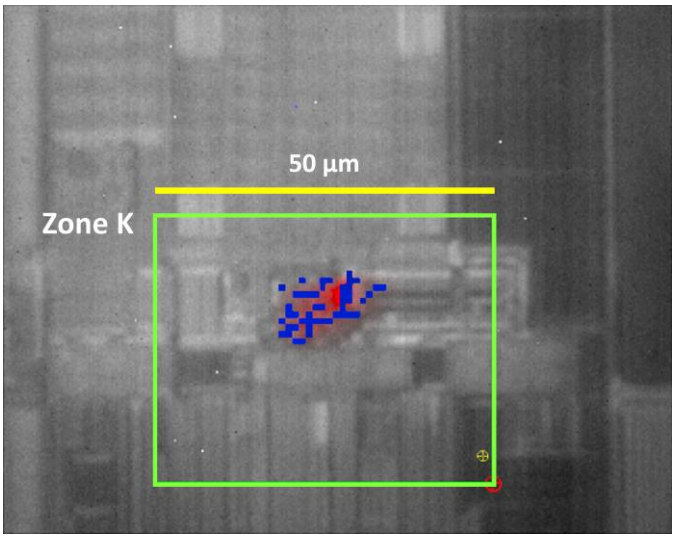

Fig. 8. SEL sensitivity mapping (blue pixels) superimposed with SEL-induced light emission (red area) for zone K.

Fig. 7 presents the EMMI images associated to SEL triggering in six different zones. Each of these images is obtained by integrating the light emission while maintaining the SEL condition for a duration of 3s. Zone I exhibits four different sensitive and light-emitting locations presented in Fig. 7-(a) to (d) that can be triggered individually. In the HPIO region, a similar behavior is observed in zone A with four independent sensitive locations (only one is activated in Fig. 7-(e)). Fig. 7-(f) and (g) show larger emitting areas, especially for zone C, in which a single SEL produces an important emission from a large area all along the structure. This could be due either to a very large well or to the propagative contamination of the initial latch-up to adjacent wells. Fig 7-(h) presents the light emission for zone F associated to the most important latch-up current. The structure involved presents clearly visible similitudes with the large sensitive area of zone C. Similarly, the structure involved in zone G (Fig 7-(i)) seems to correspond to a half of the sensitive region of zone B, which appears to be coherent with the corresponding SEL currents presented in Fig. 4: the SEL current of zone B is approximately twice the current for zone G.

Fig. 8 presents, as an example, the good correlation between the SEL mapping (in blue pixels) and the SEL-induced light emission for the zone K. Zone K is a sensitive region related to the PL clock network (see Fig. 3). This structure is repeated several times in the three Horizontal Clock Spines (HCS). One can note that the light emission is more pronounced in a small part on the top right of the sensitive structure, and more diffused towards the left side of the image. This provides an interesting visualization of the lateral extension of the parasitic structure (around 10x8µm²) involved in the SEL in this zone.

C. Correlation between light-emitting area and SEL current amplitude

From the light-emission images presented in Fig. 7, we extracted the emitting area for each zone. Note that the emission intensity can not be extracted from those images because of the non-linearity of the imaging camera, only the emitting surface can be measured. In order to observe the correlation between the maximum measured SEL current amplitude and the light-emitting surface, Fig. 9 presents one vs the other for each zone.

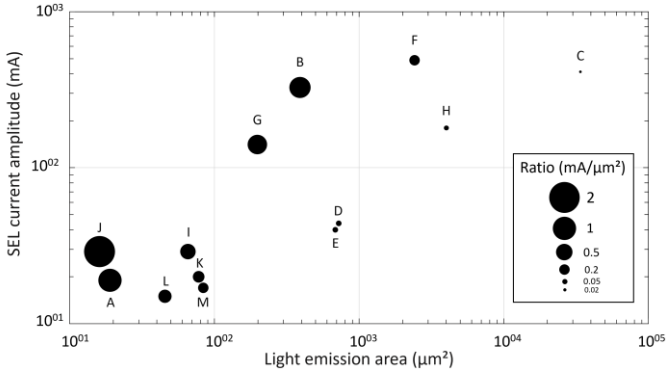

Fig. 9. SEL current amplitude vs light emission area for each zone. The size of each bubble represents the ratio between the current amplitude and the emitting area, as a possible indicator of the event criticality regarding the risk of device degradation.

One can first observe in Fig. 9 a positive relationship, with the SEL current increasing with the area of the emitting structure. This is the expected global behavior since large SEL currents are typically associated to larger or multiple parasitic structures.

In Fig. 9, the size of each bubble represents the ratio of the SEL current to the emitting area, thus in units similar to a current surface density (mA/µm²): the bigger the bubble, the higher the current or the smaller the emitting area. In this representation, it is interesting to note that zone J presents the highest ratio (biggest bubble) because, although its SEL current is not the highest, its emitting area is the smallest. This could have a direct consequence regarding the criticity of an SEL event in zone J. Indeed, for a given SEL current amplitude, if the parasitic structure that conducts this current is smaller, the resulting higher current density has typically more chance to lead to a local thermal degradation of the device structure at the origin of a latent defect. On the opposite, the zone C, which presents one of the highest SEL currents, is represented in Fig. 9 by a small bubble because light emission is distributed over a large area, probably meaning that the SEL current is distributed over a large surface. Thus, the bubble sizes in Fig. 9 could be interpreted as a first indication of the event criticality regarding the risk of device degradation or the creation of latent defects. Obviously, zones producing the highest currents remain usually the most critical regarding the impact of the SEL at board or system-level.

D. SEL functionality impact

The functional impact of each SEL was captured before the POR by the software testbench as well as by an oscilloscope monitoring the output of embedded IPs. This was used to evaluate and optimize the capability of the embedded software and IPs to self-detect and report such events as well as to confirm the type of function impacted by the SEL. Indeed, it is important to note that, when an SEL occurred in a given function of the DUT, the rest of the DUT remained totally functional until the POR was externally triggered typically a few hundreds of milliseconds later. Within this time interval, the local Joule heating associated to the SEL current produced a temperature increase that was detectable by various functions several millimeters away from the SEL location.

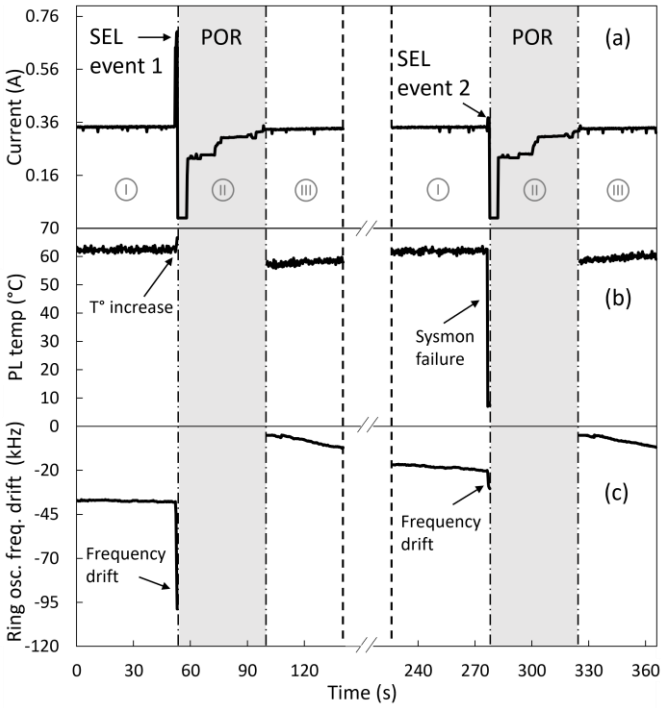

Fig. 10. Current variation (a), PL Sysmon temperature (b), and ring oscillator frequency drift (c) following SEL events in zones B (event 1) and D (event 2).

Fig. 10 presents typical SEL signatures observed on the 12V supply current, on the temperature measurement reported by the PL Sysmon and on the frequency of ring oscillators (RO) implemented in the PL. Phase I corresponds to the initial phase where the SEL is triggered, phase II is the POR phase during which no data reports from the DUT are available, and phase III is the return to the nominal operation of the embedded software. For the event 1 generated in zone B (HPIO bank), a small temperature increase is observed on the PL Sysmon as well as a significant drift of a nearby ring oscillator frequency induced by the temperature increase. For the event 2, generated

in zone D (PL Sysmon), the temperature reported by the PL Sysmon clearly indicates a failure of this function, while monitoring the ring oscillator frequency permits diagnosis of a temperature increase. Similar observations were performed on the various acquired data to confirm the function of each sensitive region.

E. Small current increases not correlated with light emission

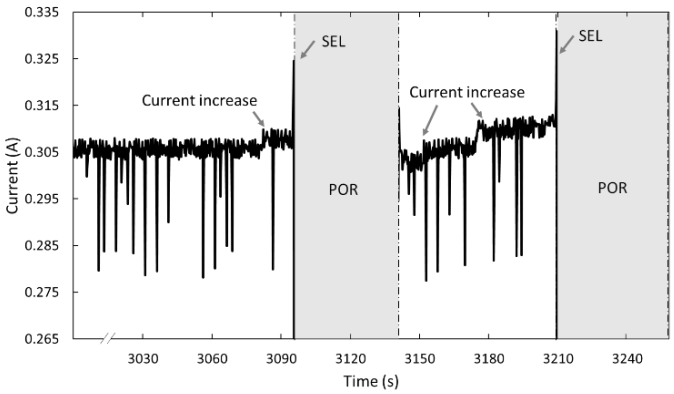

Fig. 11. Small current increases in zone I before SEL triggering.

During the latch-up mapping of zone I, multiple current increases of about 5mA each were observed. Fig. 11 shows these current variations for an incident energy of 345pJ. The SEL threshold was defined 15mA above the nominal current consumption. One can note that these small current increases occur multiple times before a significant increase of the current counted as an SEL, which leads to a power cycling.

These small current increases were not correlated with light emission, implying that they can not be attributed for sure to an SEL mechanism. Light emission was only observed in correlation with the significant current increase that followed several small increases. These observations could be explained either by the limited sensitivity of the infrared camera that prevented the capture of weak light emission, or by a circuit-specific mechanism related to, for example, an upset in the configuration of the IO.

F. Effect of temperature

To evaluate the effect of temperature on SEL [11], [13], [30-32] in this device, SEL laser energy threshold measurements were performed at die temperature of 48°C, 64°C (nominal condition) and 75°C as measured by both the PL and PS Sysmon. To change the temperature, the activity of the device was changed by adjusting the length and number of active ring oscillators in the PL. For each temperature, the SEL current threshold was set to be 15mA above the nominal current.

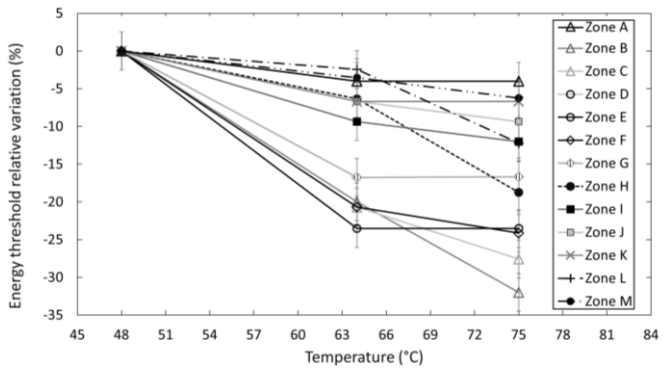

Fig. 12. SEL energy threshold relative variation as a function of device temperature for all zones defined in Fig. 3.

Fig. 12 presents the relative variation of SEL energy thresholds with temperature for each zone. As expected, an increase of the device temperature leads to a smaller SEL energy threshold. Zones in the HPIO banks present both the smallest (zone A) and highest (zones B and C) variations, with a maximum variation of 33% for zone B from 48 to 75°C. Note that the vertical error bars may mask variations smaller than 5%. The inhomogeneous or irregular behavior of the different zones with temperature could be explained by temperature inhomogeneities across the chip.

G. Impact of bias on SEL threshold

Our testbench being based on a commercial SoM, only the bias of one HDIO bank (VCCO) can be changed to explore its impact on SEL. This bank accepts three supply voltages: 1.8V (default configuration), 2.5V and 3.3V. Fig. 13 shows the impact of this bias on the SEL energy threshold for the sensitive regions identified in HDIO banks. The SEL threshold for zone J decreases when the voltage increases, which is the expected behavior [11-13]. The threshold for zone I is constant for the three supply voltages, probably meaning that the structures involved in the SEL in zone I are not biased by the VCCO voltage but rather by a constant voltage supplied by another input.

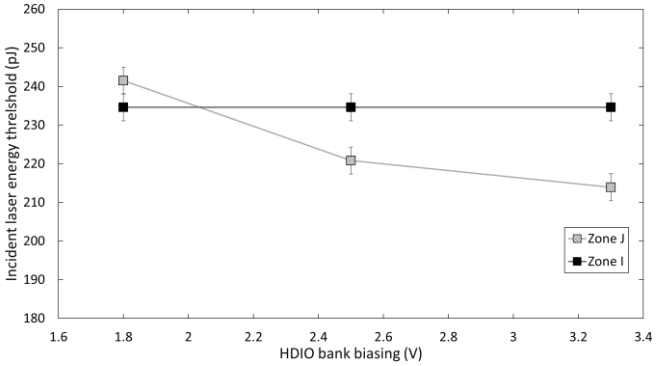

Fig. 13. SEL laser energy threshold in zones I and J as a function of the HDIO bank bias.

H. SEL laser cross section

SEL mappings were performed on the different regions with increasing laser pulse energies to extract the energy threshold for each zone as well as the sensitive area (i.e. laser cross section) as a function of the laser energy.

Fig. 14 presents the total SEL cross section as a function of the incident laser energy. This cross section was obtained by summing the contribution of each zone multiplied by its number of identified instances. For zones repeated many times within the device, only a random selection of a few instances were verified to present the same sensitivity as the mapped instance. The curve presents a threshold close to 100pJ and a saturation cross section around 10^{-3} cm^2. Error bars in Fig. 14 represent an uncertainty of ±3.5pJ on the pulse energy measurements and the

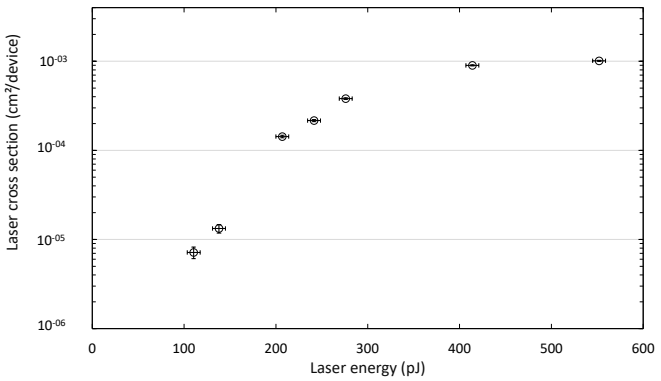

Fig. 14. Total SEL laser cross section vs incident pulse energy.

statistical error proportional to the square root of the number of events [33]. Due to the number of events observed, which is higher than a hundred at the threshold, error bars appear as relatively small and will not be represented in the following correlation with heavy ions data.

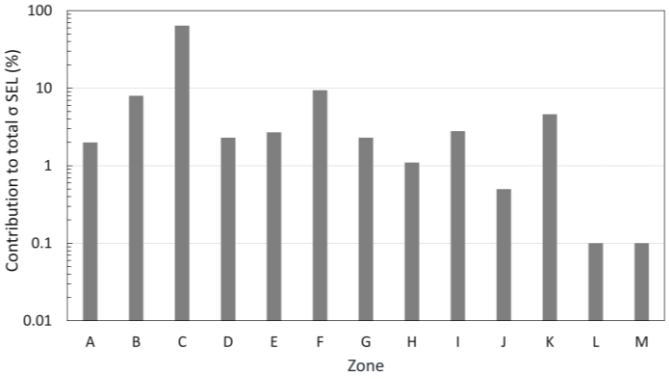

Fig. 15. Contribution of the different zones to the total SEL cross section.

Fig. 15 details the contribution of the different zones to the total SEL cross section. Zone C is by far the main contributor to the total cross section (64%), with the smallest contributions (zones L and M) being close to 3 orders of magnitude lower. Zone F, which is at the origin of the highest SEL current, has a contribution of approximately 9%. Zones I, J, and K, although repeated almost a hundred times in the DUT, each have a contribution lower than 5% to the total cross section.

I. Correlation with heavy ion data

In order to correlate the laser cross section measurements above with heavy ion data from the literature, the equivalent LET of each laser pulse energy, LET_{laser}, is calculated using [34]:

$$LET_{laser} = \frac{E_{pair}}{d_V} \iiint_V N_{laser}(r)dr, \qquad (1)$$

where E_{pair} is the average energy for electron-hole pair creation in silicon (3.6eV), N_{laser} is the pair density distribution induced by the laser pulse in the device, V is a pertinent volume, over which this density is integrated, and d_V is the thickness of the sensitive volume. N_{laser} is computed by the Pulsworks software considering reflection on the backside surface and Beer-Lambert attenuation through the substrate. For the integration volume, a classical infinite slab of thickness 1µm (no fitting) is used to get a first order of magnitude of the equivalent LET.

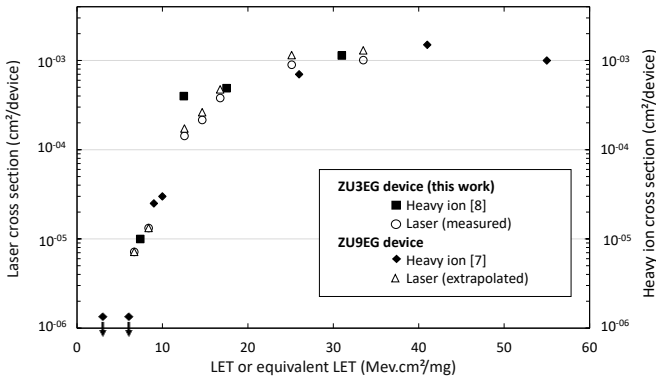

Fig. 16. SEL laser cross section correlated with heavy ion data from literature as a function of LET (heavy ion data) and equivalent LET (laser data) for the DUT tested in this work and extrapolated to a larger version of the device.

The result is presented in Fig. 16 together with heavy ion data from [8] for the same device as the one tested in this work, and from [7] for the ZU9EG version, which has one more HPIO and HDIO banks and more CLBs. The laser results obtained on the ZU3EG were extrapolated to the ZU9EG by considering the number of instances of zones A, B and C associated with one HPIO bank, and the number of instance of zones I and J associated with one HDIO bank. The correlation between laser and heavy ion data is particularly good, both for the threshold LET and the saturation cross section. Note that laser energies corresponding to equivalent LETs higher than 33MeV.cm^2/mg were not explored during our tests to limit the risk of destruction of the samples.

The good correlation of laser and heavy ion data for SEL in this 16nm FinFET device can be explained by the fact that the SEL mechanism essentially takes place in the bulk, with a crucial role of charge separation by the N-Well/P-Well or Well-Bulk junctions to trigger the event. The fact that the laser spot size is much larger than the elementary fin dimensions does not affect charge injection in those junctions, so it has no impact on our ability to trigger the mechanism and to resolve the sensitive areas.

IV. Discussion

The correlation above indicates that no significant contribution to the SEL cross section was missed during our tests, despite the lack of direct observability of the individual currents of the low voltage power supply inputs generated by the SoM regulators. The currents' observability was efficiently compensated by in-line emission microscopy and embedded instrumentation.

Given the lack of information available on the circuit and layout details of the DUT, we can still make assumptions to analyze our results. Most of the SEL sensitive zones identified in the different mappings above can be related to a device function that is susceptible to require a supply voltage higher than the core-logic voltage of 0.85V. This is obviously true for the HPIO and HDIO banks (zones A, B, C, I and J), which were nominally biased at 1.8V in our tests, as well as for the Config IO (zones F and G). This is also true for the PL and PS Sysmon (zones D and E) mixed signal circuits in charge of monitoring the various supply voltages of the DUT. The zone H, located in

the PS, was found to look very similar to the PS Sysmon structure and could thus possibly make use of voltages higher than the core. Finally, zones K, L and M, although their function is not completely identified, are all located on the edges of core logic blocks, and could also possibly make use of higher voltages. Based on those assumptions, it seems possible to conclude that, for the range of LET explored in this work and in previous heavy ion experiments, no SEL is triggered in the core-logic of both the PS and the PL and that SEL in this device can only occur in mixed-signal and IO circuits that are in some way connected to the 1.8V or 1.2V supplies.

These observations seem compatible with the results presented for a technology similar to the one tested in this work in [11], where the increased latch-up susceptibility of this finFET technology with respect to previous planar technologies is explained by an increase of the gain of the parasitic bipolar transistors involved in the latch-up due to thinner STI oxide. For the more recent 7nm technology node, it is measured in [12] an SEL holding voltage of 0.85V at elevated temperature of 125°C for neutron and alpha particle. Since this voltage is higher than the 0.7V nominal one for the core logic, it seems to indicate that the core logic can still be immune to SEL for the 7nm node, while functions that necessitate a higher supply voltage, like IOs, may still be sensitive to SEL if not carefully designed against that.

V. CONCLUSIONS

We have presented an analysis of the SEL cross section of a complex programmable SoC combining a simple electrical setup, SPA laser testing with in-line light emission microscopy and DUT-embedded instrumentation to identify the SEL sensitive areas and functions within the SoC. The obtained SEL mappings and the good correlation of laser testing results with heavy ion data indicate that no SEL is triggered in the core-logic sections of this device, and that IOs are the main contributors to the SEL cross section at high LET. This delimits the design effort for producing SEL-free designs in this 16nm finFET technology.

VI. REFERENCES

[1] A. H. Johnston and B. W. Hughlock, "Latchup in CMOS from single particles," *IEEE Trans. Nucl. Sci.*, vol. 37, no. 6, pp. 1886-1893, Dec. 1990.

[2] Y. Moreau, H. de la Rochette, G. Bruguier, J. Gasiot, F. Pelanchon, C. Sudre and R. Ecoffet, "The latchup risk of CMOS-technology in space," *IEEE Trans. Nucl. Sci.*, vol. 40, no. 6, pp. 1831-1837, Dec. 1993.

[3] F. W. Sexton, "Destructive single-event effects in semiconductor devices and ICs," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 603-621, Jun. 2003.

[4] N. A. Dodds, J. M. Hutson, J. A. Pellish, R. A. Reed, H. S. Kim, M. D. Berg, M. R. Friendlich, A. M. Phan, C. M. Seidleck, M. A. Xapsos, X. Deng, R. C. Baumann, R. D. Schrimpf, M. P. King, L. W. Massengill and R. A. Weller, "Selection of Well Contact Densities for Latchup-Immune Minimal-Area ICs," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3575-3581, Dec. 2010.

[5] C. J. Marshall, P. W. Marshall, R. L. Ladbury, A. Waczynski, R. Arora, R. D. Foltz, J. D. Cressler, D. M. Kahle, D. Chen, G. S. Delo, N. A. Dodds, J. A. Pellish, E. Kan, N. Boehm, R. A. Reed and K. A. LaBel, "Mechanisms and Temperature Dependence of Single Event Latchup Observed in a CMOS Readout Integrated Circuit From 16–300 K," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3078-3086, Dec. 2010.

[6] K. Domanski, "Latch-up in FinFET technologies," *2018 IEEE International Reliability Physics Symposium*, Burlingame, CA, USA, pp. 74-78, Mar. 2018.

[7] R. Koga, S. Davis, J. George, M. Zakrzewski and D. Mabry, "Heavy Ion and Proton Induced Single Event Effects on Xilinx Zynq UltraScale+ Field Programmable Gate Array (FPGA)," *2018 IEEE Radiation Effects Data Workshop*, Waikoloa, HI, USA, pp. 311-315, Jul. 2018.

[8] M. Glorieux, A. Evans, T. Lange, A-D. In, D. Alexandrescu, C. Boatella-Polo, R. García Alía, M. Tali, C. Urbina Ortega, M. Kastriotou, P. Fernández-Martínez and V. Ferlet-Cavrois, "Single-Event Characterization of Xilinx UltraScale+® MPSOC under Standard and Ultra-High Energy Heavy-Ion Irradiation," *2018 IEEE Radiation Effects Data Workshop*, Waikoloa, HI, USA, pp. 189-193, Jul. 2018.

[9] D. S. Lee, M. King, W. Evans, M. Cannon, A. Pérez-Celis, J. Anderson, M. Wirthlin and W. Rice, "Single-Event Characterization of 16 nm FinFET Xilinx UltraScale+ Devices with Heavy Ion and Neutron Irradiation," *2018 IEEE Radiation Effects Data Workshop*, Waikoloa, HI, USA, pp. 275-282, Jul. 2018.

[10] J. Karp, M. J. Hart, P. Maillard, G. Hellings and D. Linten, "Single-Event Latch-Up: Increased Sensitivity From Planar to FinFET," *IEEE Trans. Nucl. Sci.*, vol. 65, no. 1, pp. 217-222, Jan. 2018.

[11] C.-T. Dai S.-H. Chen, D. Linten, M. Scholz, G. Hellings, R. Boschke, J. Karp, M. Hart, G. Groeseneken, M.-D. Ker, A. Mocuta and N. Horiguchi, "Latchup in bulk FinFET technology," *2017 IEEE International Reliability Physics Symposium*, Monterey, CA, USA, pp. 698-700, Apr. 2017.

[12] D. R. Ball, C. B. Sheets, L. Xu, J. Cao, S.-J. Wen, R. Fung, C. Cazzaniga, J. S. Kauppila, L. W. Massengill and B. L. Bhuva, "Single Event Latchup in a 7-nm Bulk FinFET Technology," *IEEE Trans. Nucl. Sci*., vol. 68, pp. 830-834, May 2021.

[13] N. J. Pieper, Y. Xiong, A. Feeley, D. R. Ball, and B. L. Bhuva, "Single-Event Latchup Vulnerability at the 7-nm FinFET Node," *2022 IEEE International Reliability Physics Symposium*, Dallas, TX, USA, pp. 296-301, Mar. 2022.

[14] S. P. Buchner, F. Miller, V. Pouget and D. P. McMorrow, "Pulsed-Laser Testing for Single-Event Effects Investigations," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 1852-1875, Jun. 2013.

[15] D. Lewis, V. Pouget, F. Beaudoin, P. Perdu, H. Lapuyade, P. Fouillat, and A. Touboul, "Backside Laser Testing of ICs for SET Sensitivity Evaluation," *IEEE Trans. Nucl. Sci.*, vol 48, n°6, p. 2193-2201, Dec. 2001.

[16] D. McMorrow, S. Buchner, W. T. Lotshaw, J. S. Melinger, M. Maher and M. W. Savage, "Demonstration of single-event effects induced by through-wafer two-photon absorption," *IEEE Trans. Nucl. Sci*., vol. 51, no. 6, pp. 3553-3557, Dec. 2004.

[17] A. J. Burnell, A. M. Chugg and R. Harboe-Sørensen, "Laser SEL Sensitivity Mapping of SRAM Cells," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 4, pp. 1973-1977, Aug. 2010.

[18] P. Wang, A. L. Sternberg, J. A. Kozub, E. X. Zhang, N. A. Dodds, S. L. Jordan, D. M. Fleetwood, R. A. Reed and R. D. Schrimpf, "Analysis of TPA Pulsed-Laser-Induced Single-Event Latchup Sensitive-Area," *IEEE Trans. Nucl. Sci.*, vol. 65, no. 1, pp. 502-509, Jan. 2018.

[19] D. McMorrow, S. Buchner, M. Baze, B. Bartholet, R. Katz, M. O'Bryan, C. Poivey, K. Label, R. Ladbury, M. Maher, and F. Sexton, "Laser-induced latchup screening and mitigation in CMOS devices," *IEEE Trans. Nucl. Sci*., vol. 53, no. 4, pp. 1819-1824, Aug. 2006.

[20] S. C. Moss, S. D. LaLumondiere, J. R. Scarpulla, K. P. MacWilliams, W. R. Crain, and R. Koga, "Correlation of picosecond laser-induced latchup and energetic particle-induced latchup in CMOS test structures," *IEEE Trans. Nucl. Sci.*, vol. 42, no. 6, pp. 1948-1956, Dec. 1995.

[21] E. Faraud, V. Pouget, K. Shao, C. Larue, F. Darracq, D. Lewis, A. Samaras, F. Bezerra, E. Lorfevre, and R. Ecoffet, "Investigation on the SEL Sensitive Depth of an SRAM Using Linear and Two-Photon Absorption Laser Testing," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp. 2637-2643, Dec. 2011.

[22] N. A. Dodds, N. C. Hooten, R. A. Reed, R. D. Schrimpf, J. H. Warner, N. J.-H. Roche, D. McMorrow, S.-J. Wen, R. Wong, J. F. Salzman, S. Jordan, J. A. Pellish, C. J. Marshall, N. J. Gaspard, W. G. Bennett, E. X. Zhang and B. L. Bhuva, "Effectiveness of SEL Hardening Strategies and the Latchup Domino Effect," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2642-2650, Dec. 2012.

[23] N. A. Dodds, N. C. Hooten, R. A. Reed, R. D. Schrimpf, J. H. Warner, N. J.-H. Roche, D. McMorrow, S. Buchner, S. Jordan and J. A. Pellish, "SEL-Sensitive Area Mapping and the Effects of Reflection and Diffraction From Metal Lines on Laser SEE Testing," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 4, pp. 2550-2558, Aug. 2013.

[24] B. Ajdari, S. Sekwao, R. Ascazubi, A. Neale and N. Seifert, "On the Correlation of Laser-induced and High-Energy Proton Beam-induced Single Event Latchup," *2020 IEEE International Reliability Physics Symposium*, Dallas, TX, USA, pp. 625-629, Apr. 2020.

[25] J. M. Hales, A. Khachatrian, A. Ildefonso, S. Buchner, D. Adams, D. Wheeler, S. Messenger, C. Mishler, N. Budzinski, S. Jordan, R. Van Art

and D. McMorrow, "Pulsed-Laser Testing to Quantitatively Evaluate Latchup Sensitivity in Mixed-Signal ASICs," *IEEE Trans. Nucl. Sci.*, vol. 69, no. 3, pp. 429-435, Mar. 2022.

[26] Y.-T. Yu, J.-W. Han, G.-Q. Feng, M.-H. Cai and R. Chen, "Correction of Single Event Latchup Rate Prediction Using Pulsed Laser Mapping Test," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 2, pp. 565-570, Apr. 2015.

[27] T. Aoki and A. Yoshii, "Analysis of latchup-induced photoemission," *IEEE International Technical Digest on Electron Devices Meeting*, Washington, DC, USA, pp. 281-284, Aug. 1989.

[28] C. F. Hawkins, J. M. Soden, E. I. Cole, and E. S. Snyder, "The Use of Light Emission in Failure Analysis of CMOS ICs," *Proc. Of International Symposium for Testing and Failure Analysis*, pp.55-67, Nov. 1990.

[29] A. Glowacki and C. Boit, "Photonic localization techniques," Fault Localization Tutorial at *International Symposium for Testing and Failure Analysis*, Phoenix, Nov. 2012.

[30] A. H. Johnston, B. W. Hughlock, M. P. Baze and R. E. Plaag, "The Effect of Temperature on Single-Particle Latchup," *IEEE Trans. Nucl. Sci*., vol. 38, no. 6, pp. 1435-1441, Dec. 1991.

[31] J. M. Hutson, J. D. Pellish, G. Boselli, R. Baumann, R. A. Reed, R. D. Schrimpf, R. A. Weller and L. W. Massengill, "The Effects of Angle of Incidence and Temperature on Latchup in 65 nm Technology," *IEEE Trans. Nucl. Sci.*, vol.54, no.6, pp.2541-2546, Dec. 2007.

[32] T. F. Miyahira and F. Irom, "Results of Single-Event Latchup Measurements Conducted by the Jet Propulsion Laboratory," *2008 IEEE Radiation Effects Data Workshop*, pp.53-57, Jul. 2008.

[33] H. Quinn, "Challenges of Testing Complex Systems," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 2, pp. 766-786, Apr. 2014.

[34] V. Pouget, H. Lapuyade, P. Fouillat, D. Lewis and S. Buchner, "Theoretical Investigation of an Equivalent Laser LET," *Microelectronics Reliability*, vol. 41, pp. 1513-1518, Sep. 2001.