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A Hybrid Delay Model for Interconnected Multi-Input Gates

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Abstract—Dynamic digital timing analysis aims at substituting highly accurate but slow analog simulations of digital circuits with less accurate but fast digital approaches to facilitate tracing timing relations between individual transitions in a signal trace. This primarily requires gate delay models, where the input-to-output delay of a transition also depends on the signal history. We focus on a recently proposed hybrid delay model for CMOS multi-input gates, exemplified by a 2-input NOR gate, which is the only delay model known to us that faithfully captures both single-input switching (SIS) and multi-input switching (MIS) effects, also known as “Charlie effects”. Despite its simplicity as a first-order model, simulations have revealed that suitably parametrized versions of the model predict the actual delays of NOR gates accurately. However, the approach considers isolated gates without their interconnect.

In this work, we augment the existing model and its theoretical analysis by a first-order interconnect, and conduct a systematic evaluation of the resulting modeling accuracy: Using SPICE simulations, we study both SIS and MIS effects on the overall delay of NOR gates under variation of input driving strength, wire length, load capacitance and CMOS technology, and compare it to the predictions of appropriately parametrized versions of our model. Overall, our results reveal a surprisingly good accuracy of our fast delay model.

Index Terms—Digital circuit, delay model, dynamic timing analysis, interconnect

I. INTRODUCTION

Digital timing analysis techniques are essential for modern circuit design, as they allow to validate large designs, unlike analog simulations, e.g., using SPICE. Thanks to the elaborate static timing analysis techniques available for digital timing analysis, which employ models like CCSM [1] and ECSM [2] that facilitate an accurate corner case analysis of the delays of the gates making up a digital circuit, worst-case critical path delays can be determined accurately and fast.

Still, corner-case delay estimates from static timing analysis have limitations: they consider signal transitions in isolation, in the sense that gate and interconnect delays do not take into account the history of previous transitions. By contrast, dynamic timing analysis may uncover a circuit’s behavior that becomes only visible when considering previous signal transitions when computing some transition’s delay. Two examples where this becomes central are:

- 1) Asynchronous digital circuits. Consider the token-passing ring described and analyzed by Winstanley et al. in [3]. The circuit implements a ring oscillator made-up of stages consisting of a 2-input Muller C-gate, with its inputs connected to the previous resp. next stage. The circuit exhibits two modes of operation, namely, burst behavior versus evenly spaced output transitions, which can even switch unpredictably over time. The actual operation mode depends on the subtle interplay between two effects that determine the delay of a 2-input Muller C-gate: the *drafting effect*, a decrease of the delay happening when an output transition is close to the *previous* output transition, and the *Charlie effect*, (named after Charles Molnar, who identified its causes in the 70th of the last century, and nowadays known as a *multiple input switching* (MIS) effect [4]), an increase in the delay happening when the two inputs are switching (in the same direction) in close proximity. Consequently, to analyze the overall behavior of the ring, the timing relation of *individual* transitions need to be traced throughout the whole circuit.
- 2) Spiking neural networks (SNNs). To verify the correct operation of a delay-encoded inter-neuron link design in a hardware-implemented SNN [5], the delay between successive transitions must be tracked when they travel over the link.

Analog simulations, e.g., using SPICE, are the golden standard for such dynamic timing analyses. Unfortunately, however, their simulation times are prohibitively excessive even for moderately large circuits, as the dimension of the system of differential equations that need to be solved numerically increases with the number of transistors. By contrast, digital dynamic timing analysis techniques rest on *delay models* that provide gate delay estimations on a per-transition basis. If explicit delay formulas are available, it allows fast correctness validation and accurate performance and power estimations [6] of a large circuit even at early stages of the development.

Delay models: The simplest non-trivial delay models that are suitable for dynamic timing analysis are *single-history delay models*, as defined in [7], where the input-to-output delay $\delta(T)$ of a gate depends only on the previous-output-to-input delay T . Particularly relevant in this context is the *involution delay model* (IDM) proposed in [8], which consists of zero-time gates that are interconnected by single-input single-output

involution delay channels. Such channels are characterized by a delay function $\delta(T)$, which is a negative involution, in the sense that $-\delta(-\delta(T)) = T$. The dependence on T captures the drafting effect introduced in [3].

Unlike all other existing delay models known so far, the IDM faithfully models glitch propagation in the canonical short-pulse filtration problem [7]. Moreover, it has been shown in [9] that one can add “delay noise” to the deterministic delay function $\delta(T)$ without sacrificing faithfulness. As demonstrated in some follow-up work [10], delay noise can even be used for incorporating substantial PVT variations and aging.

The IDM is also accompanied by a publicly available timing analysis framework (the *Involution Tool* [11]), which allows to compare the accuracy of different delay models in digital timing simulation. In particular, it allows to randomly generate input traces for a given circuit, and to evaluate the accuracy of IDM predictions compared to SPICE-generated transition times and to other digital delay models. An experimental evaluation of the modeling accuracy of the IDM in [12], [11], using both measurements and simulations, has revealed very good results for inverter chains and clock trees, albeit less so for circuits containing multi-input gates. In the case of the clock tree, a speedup of a factor of 250 has been obtained relative to SPICE in terms of simulation running times.

Models capable of capturing MIS effects have been addressed in the literature before, with approaches ranging from linear [13] fitting over higher-dimensional macromodels [14] to recent machine learning methods [15]. The resulting models are very complex, however, and definitely way beyond first-order, and thus unsuitable as a basis for fast dynamic digital timing analysis. One fairly old approach for digital dynamic timing simulation, which shares some similarities with the IDM and its multi-input gate extension [16], is IRSIM [17]. The models used there consider transistors as zero-time switches, describe the resulting system as an RC network, and discretize analog switching waveforms using a comparator. Rather than employing continuous mode switching like the IDM, however, it utilizes non-continuous mode switching. Consequently, albeit IRSIM simulation models have been reported to provide good accuracy overall, they cannot model MIS effects.

In [16], Ferdowsi et al. introduced a 4-state hybrid first-order delay model for CMOS circuits, which replaces transistors by time-varying resistors according to the Shichman-Hodges transistor model [18]. As exemplified by a CMOS 2-input NOR gate (and similar gates, including NAND and Muller C-gates), they show that the resulting model faithfully captures all MIS effects. The authors also provided an explicit procedure for model parametrization and simple analytic formulas for the delay predictions, which can be used efficiently in digital dynamic timing simulations: By means of an appropriately extended version of the Involution Tool, they also showed that appropriately parametrized versions of their model predict the actual delay of NOR gates implemented in different CMOS technologies accurately and fast.

One serious limitation of [16] is that the authors have only considered gates in isolation, i.e., without any interconnecting wires. However, wires can have a substantial effect on circuit delays in practice: they have non-negligible parasitic capacitances, resistances, and inductances, which are spatially distributed and hence change with the wire length. The first main purpose of this work is to explore the delay modeling accuracy that is achievable with an augmented version of the model of [16] that covers *both* the gate and the interconnect to the successor gate. Due to lack of space, we restrict our attention solely to NOR gates; since the modeling approach of [16] is applicable to other CMOS gates as well, in particular, NAND gates and Muller C-gates, however, adding an interconnect to those gates leads to similar results.

In addition, whereas it has been shown in [16] that their model considerably outperforms the IDM in terms of average modeling in the case of circuits that also contain multi-input gates, their experiments ignored the fact that combining single-history delays with MIS effects results in a delay function $\delta(T, \Delta)$ that depends on both T and Δ . In particular, in order to maximize the average modeling accuracy (after all, very small values of T in a random trace occur rarely), their model parametrization procedure assumed $T \rightarrow \infty$. A natural question is how the prediction accuracy of a so-parametrized model behaves when both T and Δ are varied. The second main goal of the present paper is hence to conduct a refined experimental evaluation of the modeling accuracy, similar to [12], for our augmented version of the model of [16].

Detailed contributions:

- (1) We augment the model from [16] by an RC (L-type) interconnect and determine analytic expressions for the trajectories and the resulting delays. The choice for an L-type model as opposed to higher-order models is motivated by the goal of an analytically tractable and simple-to-compute first order model.
- (2) We extend the parametrization procedure from [16] to also determine the new interconnect-related model parameters. Analytic delay formulas again proved instrumental for developing a sound algorithm here.
- (3) We conduct a series of simulations to determine the accuracy of our augmented model for NOR gates interconnected by a wire. In our simulations, we consider two different CMOS technologies (15 nm and 65 nm), and vary input driving strength, wire length, load capacitance, wire resistance, and wire capacitance. Using SPICE simulations, we determine $\delta(T, \Delta)$ for different values of Δ and T , and compare those to the predictions of an appropriately parametrized version of our generalized model (determined for $T \rightarrow \infty$). Overall, our results reveal that the average accuracy of our model is surprisingly good (in the % range), and so is the worst-case accuracy, except for extremely small values of T where $\delta(T, \Delta)$ is small anyway.

Paper organization: Section II provides a brief overview of the inner workings of the advanced hybrid delay model

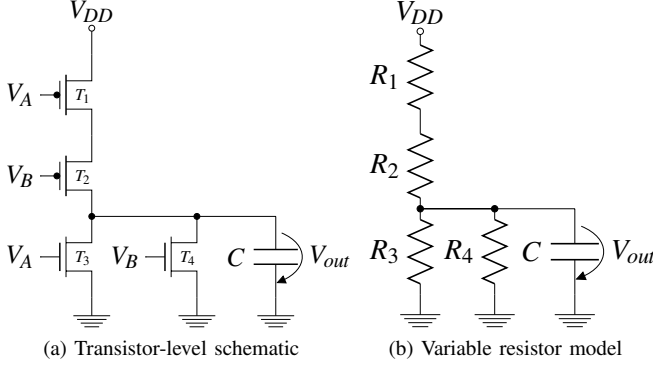


Fig. 1: CMOS NOR gate.

proposed in [16], and the main analytic results needed for developing the generalized model presented in Section III. In Section IV, we provide the results of the evaluation. We conclude in Section V and outline future research directions.

II. BACKGROUND

Since we generalize the first-order hybrid delay model for a CMOS NOR gate introduced in [16], we first provide an overview of its features. Consider the transistor implementation of a NOR gate in Fig. 1a. Let t_A , t_B , and t_O denote the points in time when the analog trajectories of input signals A , B , and the output signal O cross the *discretization threshold voltage* $V_{th} = V_{DD}/2$, respectively. Varying t_A and t_B allows to study the gate delay ($t_O - t_A$ resp. $t_O - t_B$, depending on the particular output state) over the relative *input separation time* $\Delta = t_B - t_A$.

The *advanced hybrid delay model* proposed in [16] is a generalization of the simple model introduced in [19]. Informally speaking, it replaces the immediate switching-on of the resistance of the pMOS transistors (see Fig. 1a) by the time evolution function representing the Shichman-Hodges transistor model [18], which is given by

$$R_i^{on}(t) = \frac{\alpha_i}{t - t^{on}} + R_i; \quad t \geq t^{on}. \quad (1)$$

Herein, α_i [Ω s] and on-resistance R_i [Ω] are constant slope parameters of the transistor T_i ; t^{on} represents the time when the respective transistor is switched on. Crucial in this model is that since the switching-on of the nMOS transistors is supposed to happen instantaneously, $\alpha_3 = \alpha_4 = 0$.

Applying Kirchhoff's rules to Fig. 1b leads to $C \frac{dV_{out}}{dt} = \frac{V_{DD} - V_{out}}{R_1(t) + R_2(t)} - \frac{V_{out}}{R_3(t) \parallel R_4(t)}$, which can be transformed into the non-homogeneous non-autonomous first-order ODE with non-constant coefficients

$$\frac{dV_{out}(t)}{dt} = -\frac{V_{out}(t)}{C R_g(t)} + U(t), \quad (2)$$

where $\frac{1}{R_g(t)} = \frac{1}{R_1(t) + R_2(t)} + \frac{1}{R_3(t)} + \frac{1}{R_4(t)}$ and $U(t) = \frac{V_{DD}}{C(R_1(t) + R_2(t))}$ and using the notation $R_1 = R_{pA}$, $R_2 = R_{pB}$, $R = (R_{pA} + R_{pB})/2$, $R_3 = R_{nA}$, and $R_4 = R_{nB}$ for the two

nMOS transistors T_3 and T_4 . It is well-known that the general solution of (2) is

$$V_{out}(t) = e^{-G(t)} \left[V_0 + \int_0^t U(s) e^{G(s)} ds \right], \quad (3)$$

where $V_0 = V_{out}(0)$ denotes the initial condition and $G(t) = \int_0^t (C R_g(s))^{-1} ds$. As comprehensively described in [16], depending on each particular resistor's mode in each input state transition, different expressions for $R_g(t)$ and $U(t)$ are obtained. Denoting $I_1 = \int_0^t \frac{ds}{R_1(s) + R_2(s)}$, $I_2 = \int_0^t \frac{ds}{R_3(s)}$, and $I_3 = \int_0^t \frac{ds}{R_4(s)}$, Table I summarizes them.

In order to prove that the resulting hybrid model faithfully captures all MIS effects, the authors derived analytic expressions for the trajectories of $V_{out}^{MS}(t)$ for every mode switch $MS \in \{(i, j) \rightarrow (k, l) \mid i, j, k, l \in \{0, 1\}\}$, and then determined the MIS delays for arbitrary $\Delta = t_B - t_A$ by the following procedure:

- Compute $V_{out}^{(0,0) \rightarrow (1,0)}(\Delta)$, and use it as the initial value for obtaining $V_{out}^{(0,1) \rightarrow (1,1)}(t)$; the sought gate delay is the time until the latter crosses the threshold voltage $V_{DD}/2$.
- Compute $V_{out}^{(1,1) \rightarrow (0,1)}(\Delta)$, and use it as the initial value for obtaining $V_{out}^{(0,1) \rightarrow (0,0)}(t)$; the sought gate delay is the time until the latter crosses the threshold voltage $V_{DD}/2$.

Due to some symmetry, it turned out to be sufficient to derive analytic expressions for the case $\Delta \geq 0$ only: the corresponding formulas for $\Delta < 0$ can be obtained from those by exchanging α_1 and α_2 as well as R_{nA} and R_{nB} , respectively.

Inverting the resulting trajectory formulas finally provided analytic formulas for the gate delay as functions of $\Delta \geq 0$ and the initial state, which are given in the following Theorem 1. In the proof of this theorem in [16], the range of Δ had to be split into 4 cases; an additional free parameter $\epsilon = \eta\Delta$ (for some suitably chosen $\eta \in \mathbb{R}$) was required to smoothly paste the different ranges.

Theorem 1 ([16, Thm. 2]). *Let $V_{out}^\uparrow(0)$ and $V_{out}^\downarrow(0)$ be the given initial states of respectively $V_{out}^{(1,1) \rightarrow (0,1)}$ and $V_{out}^{(0,0) \rightarrow (1,0)}$. Then, for any $0 \leq \Delta \leq \infty$, the extended delay functions for falling and rising output transitions of our model are*

$$\delta_{EM,+}^\downarrow(\Delta) = \begin{cases} -\frac{\ell C R_{nA} R_{nB} + \Delta R_{nB}}{R_{nA} + R_{nB}} + \Delta & 0 \leq \Delta < -\ell C R_{nA} \\ -\ell C R_{nA} & \Delta \geq -\ell C R_{nA} \end{cases}$$

$$\delta_{EM,+}^\uparrow(\Delta) \approx 2RC \left(\ln \left(\frac{2V_{DD}\gamma/k - 2V_{out}^\uparrow(0)e^{-\frac{\Delta}{CR_{nB}}} e^{-\frac{i_k}{C}}}{V_{DD}} \right) \right),$$

where $\ell = \ln(V_{DD}/2V_{out}^\downarrow(0))$ and Case $k \in \{1, 2, 3, 4\}$ w.r.t.

- **Case 1:** $0 \leq \Delta < \frac{\alpha_2}{2R}$,
- **Case 2:** $\frac{\alpha_2}{2R} \leq \Delta < \frac{\alpha_1 + 2\alpha_2}{4R}$,
- **Case 3:** $\frac{\alpha_1 + 2\alpha_2}{4R} \leq \Delta < \frac{\alpha_1 + \alpha_2}{2R}$,
- **Case 4:** $\frac{\alpha_1 + \alpha_2}{2R} \leq \Delta < t$.

TABLE I: Integrals $I_1(t)$, $I_2(t)$, $I_3(t)$ and $U(t)$ for every possible mode switch; $\Delta = t_B - t_A$, and $2R = R_{p_A} + R_{p_B}$.

Mode	$I_1(t) = \int_0^t \frac{ds}{R_1(s)+R_2(s)}$	$I_2(t) = \int_0^t \frac{ds}{R_3(s)}$	$I_3(t) = \int_0^t \frac{ds}{R_4(s)}$	$U(t) = \frac{V_{DD}}{C(R_1(t)+R_2(t))}$
T_-^\uparrow	0	$\int_0^t (1/R_{n_A})ds$	0	0
T_+^\uparrow	0	$\int_0^t (1/R_{n_A})ds$	$\int_0^t (1/R_{n_B})ds$	0
T_+^\uparrow	0	0	$\int_0^t (1/R_{n_B})ds$	0
T_-^\uparrow	0	$\int_0^t (1/R_{n_A})ds$	$\int_0^t (1/R_{n_B})ds$	0
T_-^\downarrow	0	0	$\int_0^t (1/R_{n_B})ds$	0
T_+^\downarrow	$\int_0^t (1/(\frac{\alpha_1}{s+\Delta} + \frac{\alpha_2}{s} + 2R))ds$	0	0	$\frac{V_{DD}t(t+\Delta)}{C(2Rt^2+(\alpha_1+\alpha_2+2\Delta R)t+\alpha_2\Delta)}$
T_+^\downarrow	0	$\int_0^t (1/R_{n_A})ds$	0	0
T_-^\downarrow	$\int_0^t (1/(\frac{\alpha_1}{s} + \frac{\alpha_2}{s+ \Delta } + 2R))ds$	0	0	$\frac{V_{DD}t(t+ \Delta)}{C(2Rt^2+(\alpha_1+\alpha_2+2 \Delta R)t+\alpha_1 \Delta)}$

Herein,

$$i_1 = \frac{(\Delta - \epsilon)^2}{2\alpha_2} - \frac{(\Delta + \epsilon)^2}{2(\alpha_1 + \alpha_2)} + \frac{4\epsilon\Delta}{\alpha_1 + 2\alpha_2} - \frac{\alpha_1 + \alpha_2}{8R^2},$$

$$i_2 = \frac{4R(\Delta - \epsilon) - (\alpha_1 + 2\alpha_2)}{8R^2} - \frac{(\Delta + \epsilon)^2}{2(\alpha_1 + \alpha_2)} + \frac{4\epsilon\Delta}{\alpha_1 + 2\alpha_2},$$

$$i_3 = \frac{4R(\Delta + \epsilon) - (\alpha_1 + 2\alpha_2)}{8R^2} - \frac{(\Delta + \epsilon)^2}{2(\alpha_1 + \alpha_2)},$$

$$i_4 = -\frac{\alpha_2}{8R^2}$$

and

$$\gamma_1 = \frac{4R^2C}{\alpha_1 + \alpha_2} e^{\frac{\alpha_1 + \alpha_2}{4R^2C}} - \frac{4R^2C}{\alpha_2}$$

$$- \left(\frac{2R(\Delta - \epsilon) - 4R^2C}{\alpha_2} - \frac{4R(\Delta - \epsilon) - 8R^2C}{\alpha_1 + 2\alpha_2} \right) e^{\frac{\Delta - \epsilon}{2RC}}$$

$$- \left(\frac{4R(\Delta + \epsilon) - 8R^2C}{\alpha_1 + 2\alpha_2} - \frac{2R(\Delta + \epsilon) - 4R^2C}{\alpha_1 + \alpha_2} \right) e^{\frac{\Delta + \epsilon}{2RC}},$$

$$\gamma_2 = \frac{4R^2C}{\alpha_1 + \alpha_2} e^{\frac{\alpha_1 + \alpha_2}{4R^2C}} - \left(1 - \frac{4R(\Delta - \epsilon) - 8R^2C}{\alpha_1 + 2\alpha_2} \right) e^{\frac{\Delta - \epsilon}{2RC}}$$

$$- \left(\frac{4R(\Delta + \epsilon) - 8R^2C}{\alpha_1 + 2\alpha_2} - \frac{2R(\Delta + \epsilon) - 4R^2C}{\alpha_1 + \alpha_2} \right) e^{\frac{\Delta + \epsilon}{2RC}}$$

$$+ \frac{4R^2C}{\alpha_2} (e^{\frac{\alpha_2}{4R^2C}} - 1),$$

$$\gamma_3 = \frac{4R^2C}{\alpha_1 + \alpha_2} e^{\frac{\alpha_1 + \alpha_2}{4R^2C}} - \left(1 - \frac{2R(\Delta + \epsilon) - 4R^2C}{\alpha_1 + \alpha_2} \right) e^{\frac{\Delta + \epsilon}{2RC}}$$

$$+ \frac{4R^2C}{\alpha_2} (e^{\frac{\alpha_2}{4R^2C}} - 1),$$

$$\gamma_4 = \frac{4R^2C}{\alpha_2} (e^{\frac{\alpha_2}{4R^2C}} - 1).$$

$\delta_{EM,-}^\downarrow(\Delta)$ and $\delta_{EM,-}^\uparrow(\Delta)$ can be easily obtained by our symmetry.

The delay formulas provided by Theorem 1 capture both multi input switching (MIS) and single input switching (SIS). For the SIS switching $(0,0) \rightarrow (1,0) \rightarrow (0,0)$, for example, it suffices to replace the initial value $V_{out}^{(1,1) \rightarrow (1,0)}(\Delta)$ in $V_{out}^{(1,0) \rightarrow (0,0)}(t)$ by the initial value $V_{out}^{(0,0) \rightarrow (1,0)}(\Delta)$, which

gives the output voltage at the time the previous switch from $(0,0)$ to $(1,0)$. For verifying the MIS effects, it even suffices to start with the initial values $V_{out}^\uparrow(0) = 1$ resp. $V_{out}^\downarrow(0) = 0$ in the case of falling resp. rising input transitions, which represent the situation where the NOR gate has been initialized to the state $(0,0)$ resp. $(1,1)$ long ago.

In [16], the authors showed how to parametrize their hybrid model for matching a given circuit, and demonstrated a very good modeling accuracy for both 15 nm and 65 nm CMOS technologies by comparing the delay predictions of the hybrid model $\delta_{EM}^{\uparrow/\downarrow}(\Delta)$ with SPICE-generated actual circuit delays $\delta_S^{\uparrow/\downarrow}(\Delta)$.

III. ADDING INTERCONNECT MODELING

Since the model of [16] considers a single NOR gate in isolation, the question arises whether and how much the delay modeling accuracy suffers when considering gates and interconnecting together. Indeed, wires can have a substantial effect on circuit delays: Actual wires have parasitic capacitances, resistances, and inductances, which are spatially distributed and hence change with the wire length. State-of-the-art interconnect modeling usually breaks up wires into segments, each of which is characterized by some lumped model, typically of Π , T, and RC type [20].

Since our focus is on exploring the modeling accuracy achievable with first-order hybrid models, we restrict our attention to the lumped RC model, as shown in Fig. 2. Although this model is known to be less accurate than e.g. the Π model in static timing analysis, it is the only one that can be added to the gate model of [16] without turning it into a second-order model: Adding a T or Π model would add another state-holding stage (capacitor) and hence raise the dimension of the ODE systems to 2.

A. The interconnect-augmented hybrid delay model

Applying Kirchhoff's rules to the interconnect-augmented variable resistor model easily lead to the non-homogeneous ODE

$$\frac{dV_{out}(t)}{dt} = -\frac{V_{out}(t)}{C R_g(t)(\frac{R_5}{R_g(t)} + 1)} + \frac{V_{DD}}{C(R_1(t) + R_2(t))(\frac{R_5}{R_g(t)} + 1)},$$

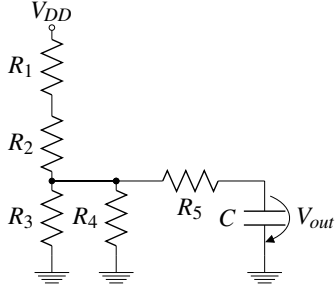


Fig. 2: CMOS NOR gate model with the lumped RC interconnect.

which is just (2) with the additional factor $f(t) = 1/(\frac{R_5}{R_g(t)} + 1)$ in all terms except $\frac{dV_{out}(t)}{dt}$. Since this non-constant factor $f(t)$ makes the already very challenging derivations leading to the analytic delay expressions given in Theorem 1 even worse, if at all tractable, we decided to take the “easy route” of approximating $f(t)$ by a constant value: A constant value F for $f(t)$ enables us to efficiently solve the above ODE, by just replacing C with $\frac{C}{F}$ in (2). In order to reduce the approximation error, however, we use different values of F in different scenarios. Note that this “easy route” also works for augmenting delay models for other gates, including Muller C-gates.

Recall that in the original hybrid model, each mode switch enables some specific ODE system, the solution of which gives the respective trajectory. Fortunately, as can be observed in Table I, all transitions except $(0,1) \rightarrow (0,0)$ and $(1,0) \rightarrow (0,0)$ lead to a constant value for $R_g(t)$ a priori. Consequently, for those six transitions, we can safely substitute $f(t)$ by the appropriate constant value.

Unfortunately, this is not the case for the transitions $(0,1) \rightarrow (0,0)$ and $(1,0) \rightarrow (0,0)$, though, so replacing $f(t)$ by some constant value introduces some approximation error. Fortunately, the time span during which $R_g(t)$ varies significantly is very small. Moreover, its variability is not very large either: In particular, as the switch-on of a transistor is fast, one may reasonably conjecture that replacing $f(t)$ by $1/(\frac{R_5}{R_{gmin}} + 1)$ should lead to a good approximation; and indeed, the results of our validation experiments in Section IV confirm this conjecture. One can infer from Table I that $(0,1) \rightarrow (0,0)$ resp. $(1,0) \rightarrow (0,0)$ leads to $1/R_g(t) = 1/(\frac{\alpha_1}{t+\Delta} + \frac{\alpha_2}{t} + 2R)$ resp. $= 1/(\frac{\alpha_1}{t} + \frac{\alpha_2}{t+\Delta} + 2R)$, which both lead to $1/R_{gmin} = 1/(2R)$. Putting everything together, Table II summarizes all exact and approximate values of $R_g(t)$ and F corresponding to each mode switch.

The results of the above discussion are summarized in the following Corollary 1, which gives the delay predictions of our generalized advanced model for the case $\Delta \geq 0$. As in the case of Theorem 1, the analogous expressions for $\delta_{M,-}^{\downarrow}(\Delta)$ and $\delta_{M,-}^{\uparrow}(\Delta)$ can be obtained by exchanging α_1 and α_2 as well as R_{n_A} and R_{n_B} , respectively.

Corollary 1. Let $V_{out}^{\uparrow}(0)$ and $V_{out}^{\downarrow}(0)$ be the given initial states of respectively $V_{out}^{(1,1) \rightarrow (0,1)}$ and $V_{out}^{(0,0) \rightarrow (1,0)}$. Then, for

TABLE II: Inputs mode switching and the resulting values for $R_g(t)$ and the corresponding approximation F for $f(t)$.

MS	$R_g(t)$	$f(t)$
$(0,0) \rightarrow (1,0)$	$= R_{n_A}$	$= \frac{R_{n_A}}{R_5 + R_{n_A}}$
$(1,0) \rightarrow (1,1)$	$= \frac{R_{n_A} R_{n_B}}{R_{n_A} + R_{n_B}}$	$= \frac{R_{n_A} R_{n_B}}{R_5(R_{n_A} + R_{n_B}) + R_{n_A} R_{n_B}}$
$(0,0) \rightarrow (0,1)$	$= R_{n_B}$	$= \frac{R_{n_B}}{R_5 + R_{n_B}}$
$(0,1) \rightarrow (1,1)$	$= \frac{R_{n_A} R_{n_B}}{R_{n_A} + R_{n_B}}$	$= \frac{R_{n_A} R_{n_B}}{R_5(R_{n_A} + R_{n_B}) + R_{n_A} R_{n_B}}$
$(1,1) \rightarrow (0,1)$	$= R_{n_B}$	$= \frac{R_{n_B}}{R_5 + R_{n_B}}$
$(1,1) \rightarrow (1,0)$	$= R_{n_A}$	$= \frac{R_{n_A}}{R_5 + R_{n_A}}$
$(0,1) \rightarrow (0,0)$	$\approx 2R$	$\approx \frac{2R}{R_5 + 2R}$
$(1,0) \rightarrow (0,0)$	$\approx 2R$	$\approx \frac{2R}{R_5 + 2R}$

any $0 \leq \Delta \leq \infty$, the delay functions for falling and rising output transitions of our model are

$$\delta_{M,+}^{\downarrow}(\Delta) = \begin{cases} -\frac{\ell C_2 R_{n_A} R_{n_B} + \Delta R_{n_B}}{R_{n_A} + R_{n_B}} + \Delta & 0 \leq \Delta < -\ell C_1 R_{n_A} \\ -\ell C_1 R_{n_A} & \Delta \geq -\ell C_1 R_{n_A} \end{cases}$$

$$\delta_{M,+}^{\uparrow}(\Delta) \approx 2RC_4 \left(\ln \left(\frac{2V_{DD}\gamma_k - 2V_{out}^{\uparrow}(0)e^{-\frac{\Delta}{C_4 R_{n_B}}} e^{-\frac{i_k}{C_4}}}{V_{DD}} \right) \right),$$

where $C_1 = \frac{C(R_5 + R_{n_A})}{R_{n_A}}$, $C_2 = \frac{C(R_5(R_{n_A} + R_{n_B}) + R_{n_A} R_{n_B})}{R_{n_A} R_{n_B}}$, $C_3 = \frac{C(R_5 + R_{n_B})}{R_{n_B}}$, and $C_4 = \frac{C(R_5 + 2R)}{2R}$. Besides, γ_k , and i_k for $k \in \{1, \dots, 4\}$ are as defined in Theorem 1.

A mandatory prerequisite for using our generalized model and, in particular, for conducting the validation experiments in Section IV, is a parametrization procedure that allows to determine suitable model parameters. It will be developed in Section III-B. Given the additional parameter (R_5), the procedure is considerably more involved than the one used for the original model in [16].

B. Parametrization procedure

Recall the model’s primary objective, which is capturing the MIS effects as well as possible. As in [16], our parametrization procedure aims at matching the characteristic Charlie delay values $\delta_S^{\downarrow}(-\infty)$, $\delta_S^{\downarrow}(0)$, $\delta_S^{\downarrow}(\infty)$ and the values $\delta_S^{\uparrow}(-\infty)$, $\delta_S^{\uparrow}(0)$, and $\delta_S^{\uparrow}(\infty)$ of a real circuit by the corresponding predicted delay values of our model given in Corollary 1 as closely as possible.

Whereas just applying the least square fitting approach advocated in [16] seemed appropriate at the first glance, it turned out that the additional R_5 term considerably changed the situation. To be more precise, assuming that the on-resistors of the two nMOS transistors R_{n_A} and R_{n_B} are roughly be the same, it turns out that $\frac{\delta_{M}^{\downarrow}(\infty)}{\delta_{M}^{\downarrow}(0)} \approx 1 + \frac{R_{n_A}}{2R_5 + R_{n_A}}$. In the case of $R_5 = 0$, which represents the original model, this translates to $\frac{\delta_{M}^{\downarrow}(\infty)}{\delta_{M}^{\downarrow}(0)} \approx 2$. In [16], this was ensured by choosing a suitable pure delay δ_{min} , also present in the original IDM, which defers the switching to the new state upon an input transition. This way, $\frac{\delta_{M}^{\downarrow}(\infty) - \delta_{min}}{\delta_{M}^{\downarrow}(0) - \delta_{min}} \approx 2$ could be enforced.

In the case of $R_5 \geq 0$, we have this resistor as another handle on matching a given ratio $\frac{\delta_M^\downarrow(\infty)}{\delta_M^\downarrow(0)}$, besides δ_{\min} . Any setting of these parameters that satisfies

$$\frac{\delta_S^\downarrow(\infty) - \delta_{\min}}{\delta_S^\downarrow(0) - \delta_{\min}} \approx 1 + \frac{R_{n_A}}{2R_5 + R_{n_A}} \quad (4)$$

is a feasible choice here.

Indeed, contrary to our initial conjecture that the additional R_5 term might make the parametrization of the generalized model more difficult than the parametrization of the original model, it turned out that the relation $R_5 \approx \frac{R_{n_A}}{2} \left(\frac{\delta_S^\downarrow(0) - \delta_{\min}}{\delta_S^\downarrow(\infty) - \delta_S^\downarrow(0)} - 1 \right)$ implied by (4) enabled us to completely decouple the parametrization process for the falling and rising output transition cases. We therefore arrived at the parametrization procedure shown in Algorithm 1, where the outer loop searches for the best value of δ_{\min} within some a priori given range $[\hat{\delta}_{\min}, \hat{\delta}_{\min}]$.

Algorithm 1: *Parametrization procedure.*

Input: Desired load capacitance C , range $[\bar{\delta}_{\min}, \hat{\delta}_{\min}]$

Output: Chosen model parameters

- 1 $w \leftarrow$ a fixed step size;
 - 2 $\delta_{\min} \leftarrow \bar{\delta}_{\min}$;
 - 3 **while** $\delta_{\min} \leq \hat{\delta}_{\min}$ **do**
 - 4 Simultaneously determine R_{n_A} and R_{n_B} to respectively match $\delta_{M,+}^\downarrow(\infty)$, $\delta_{M,+}^\downarrow(0)$, and $\delta_{M,-}^\downarrow(-\infty)$ with $\delta_S^\downarrow(\infty) - \delta_{\min}$, $\delta_S^\downarrow(0) - \delta_{\min}$, and $\delta_S^\downarrow(-\infty) - \delta_{\min}$;
 - 5 $R_5 \leftarrow \frac{R_{n_A}}{2} \left(\frac{\delta_S^\downarrow(0) - \delta_{\min}}{\delta_S^\downarrow(\infty) - \delta_S^\downarrow(0)} - 1 \right)$;
 - 6 Determine the remaining parameters R , α_1 , α_2 and η , to respectively match $\delta_{M,+}^\uparrow(\infty)$, $\delta_{M,+}^\uparrow(0)$, and $\delta_{M,-}^\uparrow(-\infty)$ to $\delta_S^\uparrow(\infty) - \delta_{\min}$, $\delta_S^\uparrow(0) - \delta_{\min}$, and $\delta_S^\uparrow(-\infty) - \delta_{\min}$;
 - 7 Store δ_{\min} , all the parameters, and the average relative error obtained;
 - 8 $\delta_{\min} \leftarrow \delta_{\min} + w$;
 - 9 **Retrieve and return**
 $(\delta_{\min}, C, R_{n_A}, R_{n_B}, R_5, R, \alpha_1, \alpha_2, \eta)$ leading to the smallest relative error;
-

IV. EVALUATION OF ACCURACY

We conducted simulations to evaluate the prediction accuracy of our generalized model. As illustrated in Fig. 3, we instantiated a NOR gate connected to an inverter, acting as its load, via a controlled wire. The inputs of the NOR gate are driven by a chain of 4 inverters acting as signal shaping gates. The chain input is stimulated by a saturated ramp with a rise/fall time of 0.1 fs, which leads to “natural” signal waveforms at the chain output.

For every setting, the following steps were performed:

- (1) Based on a Verilog description of our CMOS NOR gate implementation, we used the Cadence tools Genus and

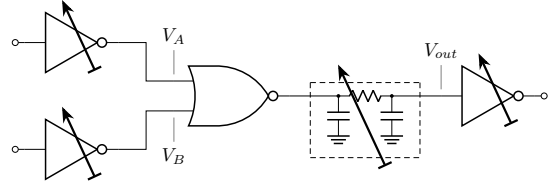


Fig. 3: *Experimental setup.*

Innovus (version 19.11) for placing and routing our design.

- (2) Using the extracted parasitic networks from the final layout, we performed SPICE simulations to determine $\delta^{\uparrow/\downarrow}$ for different values of T and Δ .
- (3) Using the measured delay values $\delta_S^\downarrow(\infty)$, $\delta_S^\downarrow(0)$, and $\delta_S^\downarrow(-\infty)$ as well as $\delta_S^\uparrow(\infty)$, $\delta_S^\uparrow(0)$, and $\delta_S^\uparrow(-\infty)$ obtained for $T = \infty$ and an estimate¹ of the lumped load capacitance C , we used Algorithm 1 for finding a suitable parametrization of our model.
- (4) Using the equations given in Corollary 1, we computed the predictions of the parametrized model for different values of T and Δ , and compared the outcome to the measured delays.

The different settings used in the evaluation range from different implementation technologies to varying driving strengths and load capacitances to different wire lengths, wire resistances, and wire capacitances. A representative sample of our results will be presented in the following subsections. Most of them have been obtained for a CMOS NOR gate from the 15 nm Nangate Open Cell Library featuring FreePDK15TM FinFET models [21] ($V_{DD} = 0.8$ V). Qualitatively similar results have been obtained for the UMC 65 nm technology with $V_{DD} = 1.2$ V supply voltage.

Overall, the accuracy of our generalized model is good. This is in stark contrast to the original model [16], however, where it turned out that even the parametrization procedure in step (3) already failed in most scenarios. This confirms that adding R_5 is really instrumental for modeling interconnected gates.

A. MIS accuracy

1) *Wire length:* Using the 15 nm technology, we varied the length of the wire driven by the NOR gate between $l = 3$ and $l = 15$ (in micrometer²), i.e., within a factor of 5. The dashed red curves in Fig. 4 show the resulting delays for $T = \infty$ and varying Δ ; the case $T < \infty$ will be considered in Section IV-B. The blue curve in Fig. 4 depicts the delay predictions of the model parametrized according to Table III, which match the real delays well.

2) *Wire resistance and capacitance:* In order to verify the ability of our model to adapt to varying parasitic networks, we artificially changed the resistances and capacitances of the

¹Actually, the parametrization procedure can adapt to a large range of values for C , by scaling the resistors R_{n_A} , R_{n_B} and R appropriately.

²Note that l is actually the parameter \$LENGTH in the command *relative-Place inv1 nor1 -relation R -xOffset \$LENGTH -yOffset 0* and hence almost (i.e., besides vias) the length in μm .

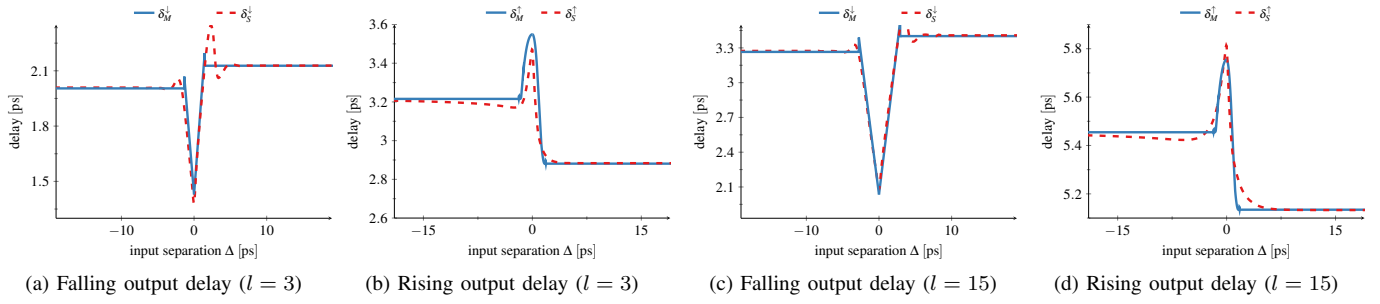


Fig. 4: SPICE ($\delta_S^{\uparrow/\downarrow}(\Delta)$) and computed ($\delta_M^{\uparrow/\downarrow}(\Delta)$) MIS delays for a 15 nm technology NOR gate for different wire lengths l .

TABLE III: Model parameter values for some wire lengths.

Parameters for $l = 3$				
$\delta_{\min} = 0.66$ ps	$C = 0.9431$ fF	$R_{n_A} = 2.0385$ k Ω	$R_{n_B} = 1.8505$ k Ω	$R_5 = 0.2060$ k Ω
$R = 1.35796$ k Ω	$\alpha_1 = 3.379 \cdot 10^{-9}$ Ω s		$\alpha_2 = 1.658 \cdot 10^{-9}$ Ω s	
Parameters for $l = 15$				
$\delta_{\min} = 0.49$ ps	$C = 1.2831$ fF	$R_{n_A} = 2.8275$ k Ω	$R_{n_B} = 2.6765$ k Ω	$R_5 = 0.4560$ k Ω
$R = 2.1819$ k Ω	$\alpha_1 = 5.799 \cdot 10^{-9}$ Ω s		$\alpha_2 = 3.068 \cdot 10^{-9}$ Ω s	

extracted network for wire length $l = 15$: In one setting, we halved all the resistor values, in another setting, we doubled the values of all capacitors. Fig. 5 shows both the real delays (dashed red curves) and the predictions of our model (blue curves) parametrized according to Table IV.

TABLE IV: Model parameter values for different wire resistances and capacitances.

Parameters for doubling the capacitances				
$\delta_{\min} = 0.54$ ps	$C = 0.7831$ fF	$R_{n_A} = 7.4575$ k Ω	$R_{n_B} = 7.1865$ k Ω	$R_5 = 0.6960$ k Ω
$R = 6.1819$ k Ω	$\alpha_1 = 14.629 \cdot 10^{-9}$ Ω s		$\alpha_2 = 7.598 \cdot 10^{-9}$ Ω s	
Parameters for half the resistor values				
$\delta_{\min} = 0.48$ ps	$C = 0.7831$ fF	$R_{n_A} = 4.8275$ k Ω	$R_{n_B} = 4.5965$ k Ω	$R_5 = 0.49605$ k Ω
$R = 3.6819$ k Ω	$\alpha_1 = 9.599 \cdot 10^{-9}$ Ω s		$\alpha_2 = 5.268 \cdot 10^{-8}$ Ω s	

3) *Input gate driving strength*: In two other settings, we varied the driving strength of the two input inverters in Fig. 3 that drive V_A and V_B of the 15 nm NOR gate driving a wire with length $l = 15$. More specifically, we used both a strong input inverter (with four parallel pMOS and nMOS transistors) and a weak input inverter, which was simulated by letting the input inverters drive three more NOR gates, which resulted in a fan-out of four. Fig. 6 shows the results for both cases, which have been obtained using the model parameters given in Table V.

TABLE V: Model parameter values associated with different input gate driving strength.

Parameters for weak input				
$\delta_{\min} = 0.93$ ps	$C = 0.7831$ fF	$R_{n_A} = 5.7795$ k Ω	$R_{n_B} = 5.7265$ k Ω	$R_5 = 0.9260$ k Ω
$R = 3.9819$ k Ω	$\alpha_1 = 11.129 \cdot 10^{-9}$ Ω s		$\alpha_2 = 5.898 \cdot 10^{-9}$ Ω s	
Parameters for strong input				
$\delta_{\min} = 0.45$ ps	$C = 0.7831$ fF	$R_{n_A} = 4.637$ k Ω	$R_{n_B} = 4.316$ k Ω	$R_5 = 0.4160$ k Ω
$R = 3.5819$ k Ω	$\alpha_1 = 9.169 \cdot 10^{-9}$ Ω s		$\alpha_2 = 6.248 \cdot 10^{-8}$ Ω s	

4) *Load capacitance*: We also varied the load capacitance of the 15 nm NOR gate with wire lengths $l = 3$ and $l = 15$, by increasing its fan-out: We replaced the single inverter used in the previous settings by inverters that consist of 2, 4 and 8 parallel pMOS and nMOS transistors. Fig. 7 shows the results, using the parametrization given in Table VI.

TABLE VI: Model parameter values corresponding to different load capacitances.

Parameters for Fig. 7a				
$\delta_{\min} = 0.61$ ps	$C = 2.065$ fF	$R_{n_A} = 1.3085$ k Ω	$R_{n_B} = 1.2205$ k Ω	$R_5 = 0.106$ k Ω
$R = 0.9579$ k Ω	$\alpha_1 = 2.339 \cdot 10^{-9}$ Ω s		$\alpha_2 = 1.108 \cdot 10^{-9}$ Ω s	
Parameters for Fig. 7c				
$\delta_{\min} = 0.64$ ps	$C = 6.689$ fF	$R_{n_A} = 9.7385$ k Ω	$R_{n_B} = 9.4005$ k Ω	$R_5 = 0.1059$ k Ω
$R = 0.8546$ k Ω	$\alpha_1 = 2.239 \cdot 10^{-9}$ Ω s		$\alpha_2 = 1.158 \cdot 10^{-9}$ Ω s	
Parameters for Fig. 7e				
$\delta_{\min} = 0.47$ ps	$C = 3.652$ fF	$R_{n_A} = 1.1422$ k Ω	$R_{n_B} = 1.0855$ k Ω	$R_5 = 0.2160$ k Ω
$R = 0.9434$ k Ω	$\alpha_1 = 2.059 \cdot 10^{-9}$ Ω s		$\alpha_2 = 0.898 \cdot 10^{-9}$ Ω s	
Parameters for Fig. 7g				
$\delta_{\min} = 0.51$ ps	$C = 7.266$ fF	$R_{n_A} = 1.1725$ k Ω	$R_{n_B} = 1.1365$ k Ω	$R_5 = 0.1050$ k Ω
$R = 1.0259$ k Ω	$\alpha_1 = 2.469 \cdot 10^{-9}$ Ω s		$\alpha_2 = 1.198 \cdot 10^{-9}$ Ω s	

B. SIS accuracy

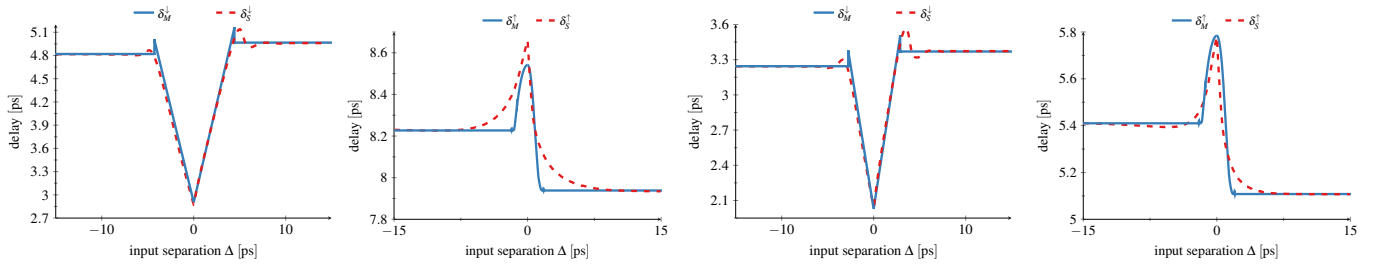
Up to now, we have exclusively focused on evaluating the modeling accuracy w.r.t. varying Δ for the case $T = \infty$. Since the model parametrization is exclusively based on this choice of delay values, it is essential to also assess the accuracy of the resulting model's predictions for the case of small previous-output-to-input delays $T < \infty$. In this subsection, we will hence vary T while choosing $|\Delta| = \infty$, which is equivalent to the SIS case.

Fig. 8a, Fig. 8b, Fig. 8c, and Fig. 8d compare the real gate delays (dashed red curve) and the delays predicted by our model (blue curve) as a function of T , for different wire lengths, wire capacitances and input driving strengths. The green curve depicts the absolute prediction error.

Whereas the perfect matching between the real delays and the model prediction for $T = \infty$ is not surprising, given that the parametrization procedure relies on the delay values for $|\Delta| = \infty$, the reasonably small prediction error for small values of T is remarkable. Significant errors occur only for extremely small values of T , in particular, for short wires ($l = 3$), where the circuit delay is extremely small anyway.

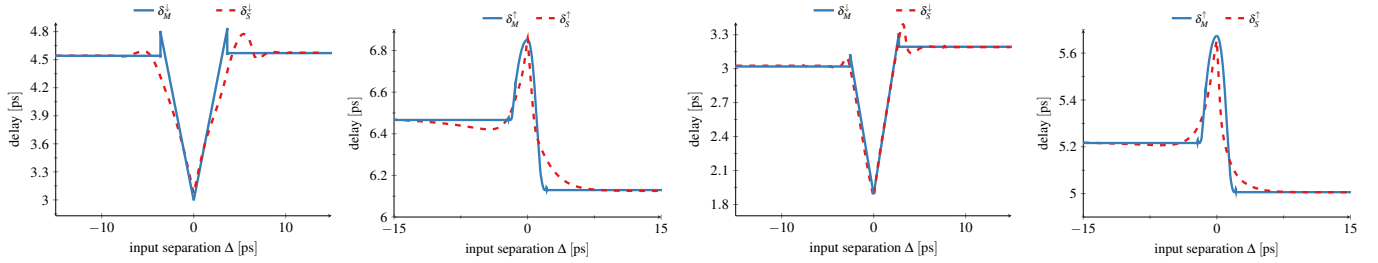
C. Delay accuracy in terms of both T and Δ

Whereas the cases $T = \infty$ resp. $|\Delta| = \infty$ considered in the two previous subsections are arguably the most relevant ones for typical signal traces, it is also important to study the delay prediction accuracy for arbitrary values of T and Δ . To this end, Fig. 9 provides the appropriate 3D diagrams for the 15 nm NOR with wire length $l = 15$: Fig. 9a shows the delay obtained by our model, Fig. 9b provides the results from SPICE simulations, and Fig. 9c shows the difference. It



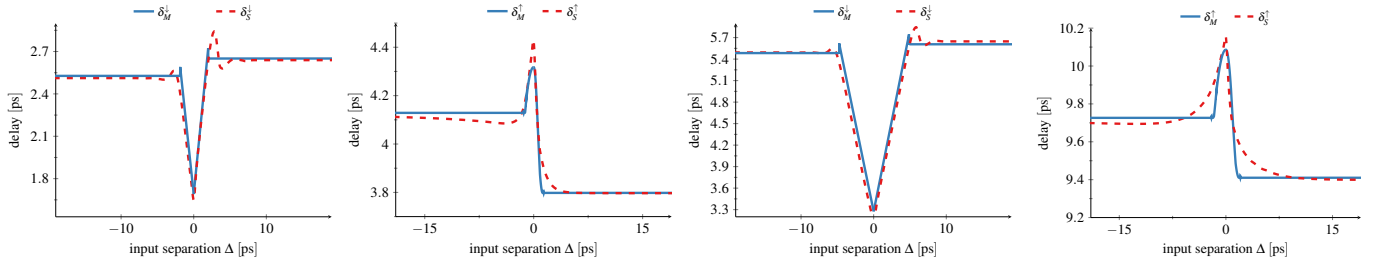
(a) Falling output delay (double capacitance) (b) Rising output delay (double capacitance) (c) Falling output delay (half resistance) (d) Rising output delay (half resistance)

Fig. 5: $SPICE(\delta_S^{\uparrow/\downarrow}(\Delta))$ and computed $(\delta_M^{\uparrow/\downarrow}(\Delta))$ MIS delays for a 15 nm technology NOR gate for wire length $l = 15$ when the wire capacitances are doubled (two left figures) resp. the wire resistors are halved (two right figures).

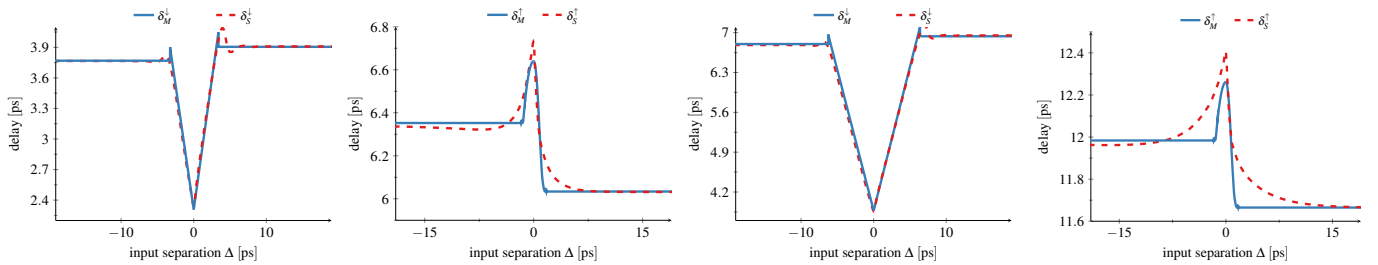


(a) Falling output delay (weak input) (b) Rising output delay (weak input) (c) Falling output delay (strong input) (d) Rising output delay (strong input)

Fig. 6: $SPICE(\delta_S^{\uparrow/\downarrow}(\Delta))$ and computed $(\delta_M^{\uparrow/\downarrow}(\Delta))$ MIS delays for a 15 nm technology NOR gate for wire length $l = 15$ with weak input drivers (two left figures) resp. strong input drivers (two right figures).



(a) Falling output delay ($l = 3$) (b) Rising output delay ($l = 3$) (c) Falling output delay ($l = 3$) (d) Rising output delay ($l = 3$)



(e) Falling output delay ($l = 15$) (f) Rising output delay ($l = 15$) (g) Falling output delay ($l = 15$) (h) Rising output delay ($l = 15$)

Fig. 7: $SPICE(\delta_S^{\uparrow/\downarrow}(\Delta))$ and computed $(\delta_M^{\uparrow/\downarrow}(\Delta))$ MIS delays for a 15 nm technology NOR gate driving two parallel pMOS and nMOS transistors (two left figures) and eight parallel pMOS and nMOS transistors (two right figures) for different wire lengths l .

is apparent that the model's inaccuracy increases substantially only (i) in the region where T gets close to 0, for any value of Δ , and (ii) in the two "dipped" regions in T direction, for some

value of $\pm\Delta$ close to 0. Indeed, (i) is confirmed by Fig. 8b, which reveals a notable relative error already for $T \leq 14$ ps for $\Delta = \infty$. Similarly, Fig. 4c shows that the model predictions do

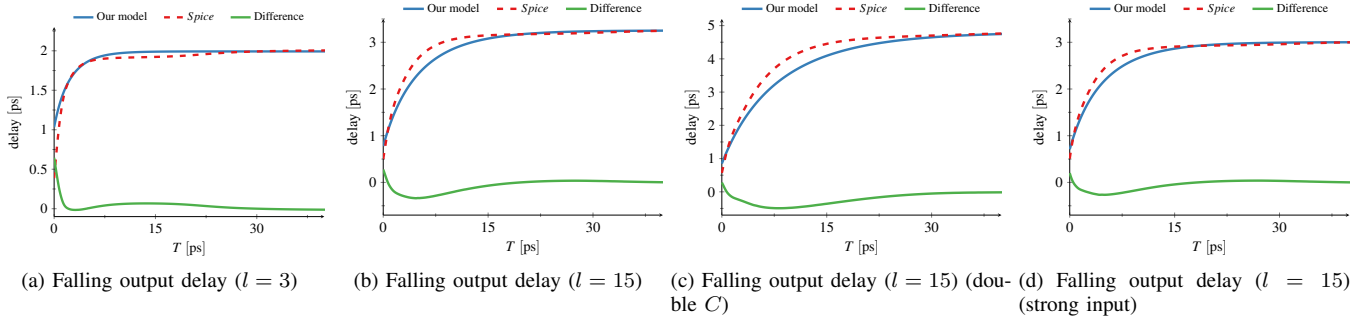


Fig. 8: Delay dependency on T in the SIS case ($|\Delta| = \infty$) obtained by our model in a 15 nm technology NOR gate w.r.t. different settings.

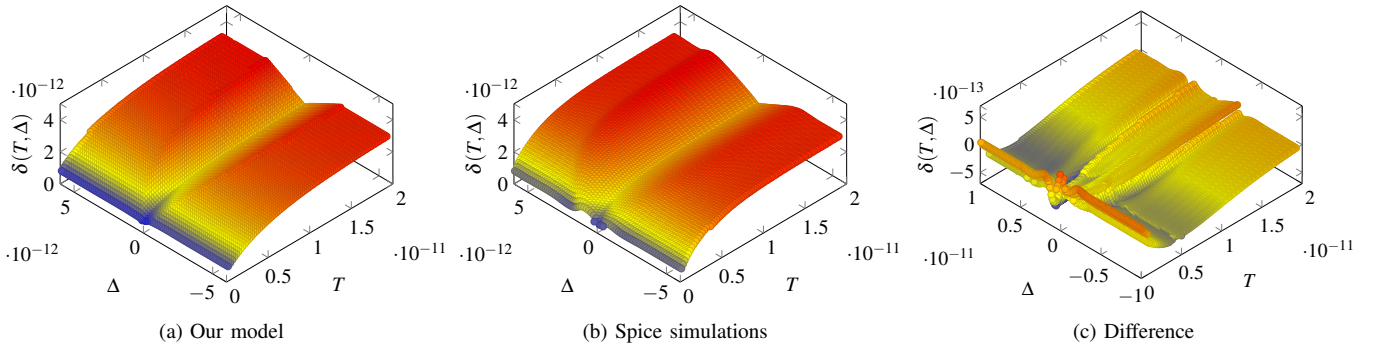


Fig. 9: Three-Dimensional delay curves $\delta(T, \Delta)$ for the 15 nm NOR gate with wire length $l = 15$.

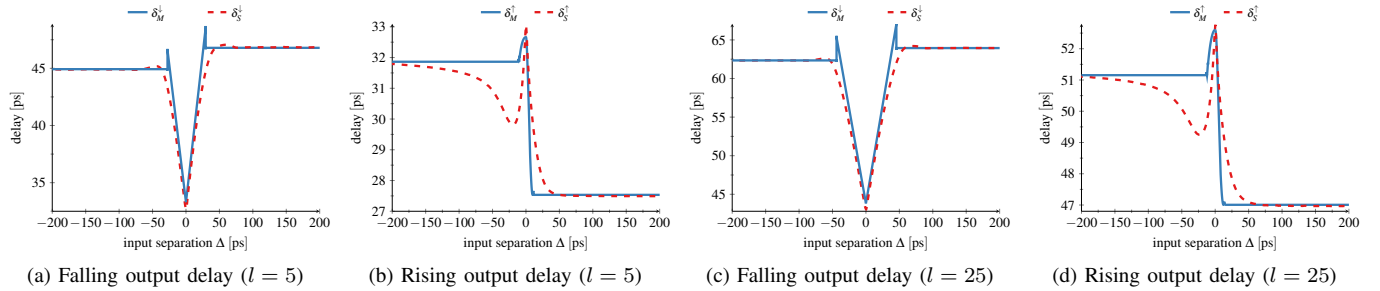


Fig. 10: SPICE ($\delta_S^{\uparrow/\downarrow}(\Delta)$) and computed ($\delta_M^{\uparrow/\downarrow}(\Delta)$) MIS delays for a 65 nm technology NOR gate with different the wire lengths $l \in \{5, 25\}$.

not perfectly match the “oscillating” real delays in the range $\Delta \in [3, 5]$ ps, for example. The worst-case absolute error in these regions is 0.567 ps, which occurs for a very small value of T where the real circuit delay is as low as 2.8 ps. The overall root-mean-square absolute error is only 0.215 ps.

Accordingly, the worst-case relative error is up to 20%, which is small given the small circuit delays in the region close to $T = 0$ where such errors occur. Overall, the RMS relative error is 7.6%, which is primarily caused by the moderately large error throughout region (i). Outside of these regions (i) and (ii), however, the achieved accuracy is indeed surprisingly small for a first-order model like ours.

TABLE VII: Model parameter values for different wire lengths in 65 nm technology.

Parameters for $l = 5$				
$\delta_{\min} = 17.3$ ps	$C = 0.9531$ fF	$R_{nA} = 39.410$ k Ω	$R_{nB} = 36.588$ k Ω	$R_S = 5.226$ k Ω
$R = 4.5879$ k Ω	$\alpha_1 = 1.308 \cdot 10^{-8}$ Ω s		$\alpha_2 = 8.759 \cdot 10^{-8}$ Ω s	
Parameters for $l = 25$				
$\delta_{\min} = 18.4$ ps	$C = 0.9531$ fF	$R_{nA} = 59.710$ k Ω	$R_{nB} = 57.288$ k Ω	$R_S = 9.226$ k Ω
$R = 15.987$ k Ω	$\alpha_1 = 8.808 \cdot 10^{-8}$ Ω s		$\alpha_2 = 34.589 \cdot 10^{-8}$ Ω s	

D. Other technologies

To validate that our model achieves comparable modeling accuracies also in different technologies, we re-run simulations also for a NOR gate in UMC 65 nm technology with $V_{DD} = 1.2$ V. Since the results are qualitatively similar, we will present only a small subset of those in this paper. Fig. 10 shows the results for two different wire lengths $l \in \{5, 25\}$,

using the parameters given in Table VII.

V. CONCLUSIONS

We generalized a recently proposed hybrid delay model for a 2-input NOR gate to accurately predict both SIS and MIS delays in the presence of interconnecting wires. We demonstrated its surprising modeling accuracy by means of simulations performed in a wide range of different settings: varying wire lengths, resistances/capacitances, input driving strengths, output load capacitances, and two different CMOS technologies. Part of our current/future work is devoted to applying our modeling approach to larger circuits.

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