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Exploring the Potential of Hafnium Oxide-Based Ferroelectric Memories for Next-Generation Storage Class Memories

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Abstract: Hafnium oxide (HfO_2) -based ferroelectric memories are emerging as appealing candidates for storage class memory (SCM) applications due to their scalability, low energy consumption, and compatibility with complementarymetal-oxide-semiconductor (CMOS) technology. Their strong ferroelectric properties at nanoscale thicknesses make them suitable for high-density memory, effectively bridging the gap between volatile and non-volatile storage. Key factors influencing their performance include the selection of dopants, the quality of the interfaces, defect management, and overall reliability, all of which impact endurance, retention, and the device's stability.

Keywords: hafnium oxide, ferroelectric memory, storageclass memory, FeFET.

I. Introduction: Modern computing demands memory solutions that combine high performance with low power consumption to address the "memory wall" in von Neumann architectures. While technologies like SRAM, DRAM, and Flash are crucial, data-centric applications require faster and more efficient emerging non-volatile memory (eNVM). HfO_2 -based ferroelectric memory is a promising option that offers rapid write speeds, low operating voltages, and high endurance.

Storage Class Memory (SCM) merges the advantages of DRAM and NAND Flash, providing high speed and non-volatility. Technologies such as Phase-Change Memory (PCM) and magneto-resistive RAM (MRAM) enhance endurance, speed, and power efficiency, making SCM vital for applications in AI and real-time data processing. Ideal SCM features include:

- Latency of 50 nanoseconds to 10 microseconds
- Minimum bandwidth of over 100 MB/s
- High endurance of over 100 million write cycles
- Low hard error rate of 1 in 10,000 bits per terabyte
- Lifespan of around 2 million hours
- Energy consumption of 100 mW during operation and under
- 1 mW on standby
- Cost under \$5 per GB

Ferroelectric materials are promising for SCM due to their fast switching and high endurance. While lead zirconate titanate (PZT) has compatibility issues, *HfO*₂-based ferroelectric materials maintain strong properties while being more compatible with CMOS technology, making them a focus for future development in SCM applications.

II. A Tour d'horizon to Ferroelectricity:



Fig. 1: History of ferroelectricity

In La Rochelle, France, the history of salt began with Jehan Seignette, who took over his father's pharmacy in 1592. His

brother, Elie, created "sel polychreste" in 1665. Rochelle salt gained prominence in the 19th century when David Brewster discovered its pyroelectricity in 1824, and the Curie brothers termed it piezoelectric in 1880. Professor Peter Debye suggested that certain molecules have a permanent electric dipole, leading to infinite dielectric constants at specific temperatures. Erwin Schrödinger introduced "ferroelectric" in 1912, arguing that all solids could show ferroelectricity at low temperatures.

Joseph Valasek highlighted Rochelle salt's piezoelectric properties in 1920, noting its electric hysteresis and polarization. Paul Scherrer and Georg Busch acknowledged research linking ferroelectricity in potassium salts to mobile hydrogen atoms. The first artificial ferroelectric material, barium titanate ($BaTiO_3$), was discovered between 1942 and 1944, demonstrating ferroelectricity in simple oxides without hydrogen. In 2011, Tim Böscke found ferroelectricity in HfO_2 , with films doped with less than 4% SiO_2 exhibiting ferroelectric properties after annealing, primarily in a metastable polar orthorhombic phase. [1-7]

Types of Ferroelectric Memories and Recent Progress:



Fig. 2: Different types of ferroelectric memories

Among the various types, Ferroelectric Field-Effect Transistors (FeFETs), Ferroelectric Random-Access Memory (FeRAM), and 1T1C FeFET configurations are gaining significant attention due to their unique advantages and potential for integration into next-generation storage class memory systems.

FeRAM (Ferroelectric Random-Access Memory): In FeRAM, data is written by switching the polarization of the ferroelectric material while read operations detect the polarization state. FeRAM is known for its fast read/write speeds, low power consumption, and endurance compared to traditional non-volatile memories like Flash, though it is typically more expensive to manufacture.

In this series of studies on FeRAM, the advanced engineering of hafnium zirconium oxide (*HZO*) thin films and FeRAM architectures are demonstrated to improve retention, endurance, and switching characteristics for FeRAM and FeFET applications, with quantitative milestones showing the technology's scalability. A $Hf_{1-x}Zr_xO_2$ nanolaminate structure with thin tetragonal phase layers achieved over 10 years of retention at 85 °C and an endurance surpassing 10¹⁰ cycles at operating voltages as low as 1.0 V in 5.5 nm-thick devices. A ferroelectric-antiferroelectric layered design also enabled a coercive field reduction and an ultrafast switching time of 780 ps at 2 V, verified using a high-speed pulsed measurement system and nucleation-limited switching models. Comprehensive benchmarking of 1T1C FeRAM arrays fabricated with the HfO2 process showed fast switching, lower read/write latencies, and energy consumption, and detailed analysis of plate line driver and bit line capacitances highlighted key performance improvements. For film scaling studies, 8-nm HfO2 samples exhibited a higher tolerance to dielectric breakdown under cycling conditions, outperforming 10-nm samples with capacitance areas as small as 0.20 µm². Furthermore, a novel capacitor-under-bitline structure achieved a large remanent polarization ($2P^r > 40 \mu C/cm^2$), projected endurance beyond 10¹¹ cycles, and robust data retention over ten years at 85 °C, demonstrating stable CMOS-compatible integration with an operation voltage of 2.5 V and read/write speeds below 10 ns. These advances mark significant steps toward ultra-lowvoltage, high-endurance ferroelectric memories, positioning them for future system-on-chip applications. [8-11]

Ferroelectric Capacitive Memory: Recent advancements in hafnium zirconate-based ferroelectric capacitors (FeCAPs) have led to energy-efficient, non-volatile memory elements that allow non-destructive read operations. The authors achieved a record capacitive memory window (CMW) of ~8.7 at 0 V in HZO-based metal-ferroelectric-metal (MFM) capacitors through interfacial engineering that introduced interface asymmetry, along with non-destructive reading capability ensures device reliability, with read endurance surpassing 10¹¹ cycles. FeCAPs are a key for CIM applications, particularly in machine learning, as they enable efficient operations without additional selectors. While challenges like limited capacitance ratios may cause minor errors in computations, co-design approaches are being explored to address these issues. Enhancements in ferroelectric properties, such as a $2P^r$ of 66.5 μ C/cm², were achieved by integrating novel interfacial layers, ensuring compatibility with CMOS technology. These developments highlight the transformative potential of hafnium zirconatebased FeCAPs in scalable and efficient memory technologies [12-16].

Silicon FeFET (Ferroelectric Field-Effect Transistor): Ferroelectric field-effect transistors (FeFETs), which use ferroelectric materials as gate dielectrics, are promising for eNVM and neuromorphic computing. They offer high-speed switching, low power consumption, and scalability, making them suitable for advanced computing. The polarization of the ferroelectric layer influences the transistor's threshold voltage, enabling persistent charge states for data storage. Integrating FeFETs with CMOS processes improves their use in sub-20nm technology. Recent developments show that FeFETs can maintain high-temperature retention and support distinct memory states for IoT devices. Additionally, FeFETbased crossbar architectures reduce variations in drain current, achieving about 97% accuracy on MNIST datasets crucial for neuromorphic computing.

Silicon-based FeFETs, particularly Si-FeFinFETs, have garnered attention in the context of neuromorphic computing. These devices have exhibited 3-bit-per-cell functionality and have demonstrated high endurance, with all-ferroelectric neural networks achieving an impressive accuracy of 97.91%. Binary neural networks optimized with Fe-FinFETs have sustained 95.2% accuracy across an extensive temperature range, from -40°C to 125°C, effectively addressing the challenges associated with temperature stability. Implementing tri-gate FeFETs with 40nm gate lengths has revealed strong ferroelectric switching capabilities, rendering them suitable for online training tasks. The scalability, multilevel storage capacity, and temperature resilience of Si-FeFETs position them as versatile candidates for next-generation computing architectures [17-24].

Metal-Oxide Channel FeFET: Recent advancements in metal oxide semiconductor channel-based FeFETs strengthen their potential for low-power, high-performance memory applications. The use of Hf_{0.5}Zr_{0.5}O₂ with back-end-of-line (BEOL) compatibility has led to monolithic 3D (M3D) architectures, achieving a remnant polarization density of 40 μ C/cm², a 0.45V memory window in 20nm transistors, write speeds of about 100ns, and endurance over 10⁸ cycles. M3D FeFETs offer three times the energy efficiency of static random-access memory (SRAM) in compute-in-memory (CIM) tasks, making them suitable for compact energyefficient systems.

Additionally, IL-free BEOL FeFETs with amorphous indium tungsten oxide (IWO) channels feature a 1.6V memory window, read-after-write latency under 300ns, and endurance over 1011 cycles. Innovations like anti-ferroelectric zirconium dioxide (ZrO₂) with IGZO channels reduce coercive fields, enhance endurance (up to 10° cycles), and support ultra-low operating voltages of 2V, with retention exceeding 10 years. Collectively, these developments highlight the transformative potential of FeFETs in memory and computing, integrating seamlessly with standard CMOS processes and innovative architectures like M3D, positioning them as a disruptive technology for energy-efficient, highdensity memory and neuromorphic computing [25,26,27].

ITIC FeFET (One-Transistor-One-Capacitor FeFET): The ITIC FeFET architecture combines a single transistor with a ferroelectric capacitor, creating a compact and efficient solution for memory applications. This design enhances data retention and reliability by using the ferroelectric capacitor to maintain polarization while the transistor handles read and write operations. It effectively balances speed and scalability, making it ideal for high-density, low-power non-volatile memory systems.

Advancements in ferroelectric memory architectures, such as 2TnC, 1T1C, and 2T2C configurations, have improved compute-in-memory (CiM) systems for edge AI and embedded applications. The 2TnC design uses two transistors and multiple ferroelectric capacitors to enhance scalability and signal integrity, allowing simultaneous read and write operations and reducing the need for 3D integration.

The 2T2C memory cell supports dual functionality, operating as either ferroelectric RAM (FeRAM) or a memristive ferroelectric tunnel junction (FTJ), enabling independent programming of its devices while facilitating inmemory processing essential for edge computing.

Further advancements in the 1T1C architecture, specifically through the C²FeRAM approach, have improved endurance and energy efficiency, achieving four times better efficiency and a 200-fold increase in inference speed compared to traditional FeRAM. Additionally, integrating ferroelectric capacitors with HK/MG MOSFETs in FeMFET configurations enhances compatibility with standard CMOS processes at ultra-low write voltages, marking significant progress towards scalable and energy-efficient ferroelectric CiM systems for future intelligent devices [28,29].

Where do ferroelectric memories find a place in the memory hierarchy?: Ferroelectric memories exhibit exceptional promise for integration across various applications, particularly in storage-class memory (SCM), where they effectively bridge the performance gap between DRAM and NAND flash. While offering access times as low as 10–20 ns, DRAM is limited by its volatility. With higher latency (50–100 μ s) and limited endurance (10³–10⁶ cycles), NAND flash struggles to meet the requirements of high-write

workloads. Ferroelectric memories, leveraging materials like doped HfO_2 , achieve sub-10 ns access times, endurance over 10^{10} , and retention capabilities spanning multiple years, making them viable for SCM applications.

As nonvolatile DRAM (nvDRAM), these



Fig. 3: Overview of semiconductor memory and possible areas of integration of ferroelectric memory

combine DRAM-equivalent speeds memories with nonvolatility, which is critical for servers, HPC systems, and real-time applications that demand high-speed data persistence during power interruptions. Furthermore, ferroelectric nonvolatile SRAM (nvSRAM) offers the speed (<5 ns) and energy efficiency of SRAM while enabling data retention, making it a compelling candidate for IoT and edge computing systems. With scalable 3D integration and densities rivaling NAND flash (terabit scale), ferroelectric memories can mitigate challenges like device scaling and thermal budgets, offering a pathway for next-generation memory solutions to replace or complement existing architectures. This technological leap positions ferroelectric memories as a cornerstone in evolving semiconductor memory hierarchies [30-35].

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