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Exploring the Potential of Hafnium Oxide-Based Ferroelectric Memories for Next-Generation Storage Class Memories

Sourav De

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measurement system and nucleation-limited switching models. Comprehensive benchmarking of 1T1C FeRAM arrays fabricated with the HfO_2 process showed fast switching, lower read/write latencies, and energy consumption, and detailed analysis of plate line driver and bit line capacitances highlighted key performance improvements. For film scaling studies, 8-nm HfO_2 samples exhibited a higher tolerance to dielectric breakdown under cycling conditions, outperforming 10-nm samples with capacitance areas as small as $0.20 \mu\text{m}^2$. Furthermore, a novel capacitor-under-bitline structure achieved a large remanent polarization ($2P^r > 40 \mu\text{C}/\text{cm}^2$), projected endurance beyond 10^{11} cycles, and robust data retention over ten years at 85°C , demonstrating stable CMOS-compatible integration with an operation voltage of 2.5 V and read/write speeds below 10 ns. These advances mark significant steps toward ultra-low-voltage, high-endurance ferroelectric memories, positioning them for future system-on-chip applications. [8-11]

Ferroelectric Capacitive Memory: Recent advancements in hafnium zirconate-based ferroelectric capacitors (FeCAPs) have led to energy-efficient, non-volatile memory elements that allow non-destructive read operations. The authors achieved a record capacitive memory window (CMW) of ~ 8.7 at 0 V in HZO-based metal-ferroelectric-metal (MFM) capacitors through interfacial engineering that introduced interface asymmetry, along with non-destructive reading capability ensures device reliability, with read endurance surpassing 10^{11} cycles. FeCAPs are a key for CIM applications, particularly in machine learning, as they enable efficient operations without additional selectors. While challenges like limited capacitance ratios may cause minor errors in computations, co-design approaches are being explored to address these issues. Enhancements in ferroelectric properties, such as a $2P^r$ of $66.5 \mu\text{C}/\text{cm}^2$, were achieved by integrating novel interfacial layers, ensuring compatibility with CMOS technology. These developments highlight the transformative potential of hafnium zirconate-based FeCAPs in scalable and efficient memory technologies [12-16].

Silicon FeFET (Ferroelectric Field-Effect Transistor): Ferroelectric field-effect transistors (FeFETs), which use ferroelectric materials as gate dielectrics, are promising for eNVM and neuromorphic computing. They offer high-speed switching, low power consumption, and scalability, making them suitable for advanced computing. The polarization of the ferroelectric layer influences the transistor's threshold voltage, enabling persistent charge states for data storage. Integrating FeFETs with CMOS processes improves their use in sub-20nm technology. Recent developments show that FeFETs can maintain high-temperature retention and support distinct memory states for IoT devices. Additionally, FeFET-based crossbar architectures reduce variations in drain current, achieving about 97% accuracy on MNIST datasets—crucial for neuromorphic computing.

Silicon-based FeFETs, particularly Si-FeFinFETs, have garnered attention in the context of neuromorphic computing. These devices have exhibited 3-bit-per-cell functionality and have demonstrated high endurance, with all-ferroelectric neural networks achieving an impressive accuracy of 97.91%. Binary neural networks optimized with Fe-FinFETs have sustained 95.2% accuracy across an extensive temperature range, from -40°C to 125°C , effectively addressing the challenges associated with temperature stability. Implementing tri-gate FeFETs with 40nm gate lengths has revealed strong ferroelectric switching capabilities, rendering them suitable for online training tasks. The scalability, multilevel storage capacity, and temperature

resilience of Si-FeFETs position them as versatile candidates for next-generation computing architectures [17-24].

Metal-Oxide Channel FeFET: Recent advancements in metal oxide semiconductor channel-based FeFETs strengthen their potential for low-power, high-performance memory applications. The use of $Hf_0.5Zr_0.5O_2$ with back-end-of-line (BEOL) compatibility has led to monolithic 3D (M3D) architectures, achieving a remnant polarization density of $40 \mu\text{C}/\text{cm}^2$, a 0.45V memory window in 20nm transistors, write speeds of about 100ns, and endurance over 10^8 cycles. M3D FeFETs offer three times the energy efficiency of static random-access memory (SRAM) in compute-in-memory (CIM) tasks, making them suitable for compact energy-efficient systems.

Additionally, IL-free BEOL FeFETs with amorphous indium tungsten oxide (IWO) channels feature a 1.6V memory window, read-after-write latency under 300ns, and endurance over 10^{11} cycles. Innovations like anti-ferroelectric zirconium dioxide (ZrO_2) with IGZO channels reduce coercive fields, enhance endurance (up to 10^9 cycles), and support ultra-low operating voltages of 2V, with retention exceeding 10 years. Collectively, these developments highlight the transformative potential of FeFETs in memory and computing, integrating seamlessly with standard CMOS processes and innovative architectures like M3D, positioning them as a disruptive technology for energy-efficient, high-density memory and neuromorphic computing [25,26,27].

1T1C FeFET (One-Transistor-One-Capacitor FeFET): The 1T1C FeFET architecture combines a single transistor with a ferroelectric capacitor, creating a compact and efficient solution for memory applications. This design enhances data retention and reliability by using the ferroelectric capacitor to maintain polarization while the transistor handles read and write operations. It effectively balances speed and scalability, making it ideal for high-density, low-power non-volatile memory systems.

Advancements in ferroelectric memory architectures, such as 2TnC, 1T1C, and 2T2C configurations, have improved compute-in-memory (CiM) systems for edge AI and embedded applications. The 2TnC design uses two transistors and multiple ferroelectric capacitors to enhance scalability and signal integrity, allowing simultaneous read and write operations and reducing the need for 3D integration.

The 2T2C memory cell supports dual functionality, operating as either ferroelectric RAM (FeRAM) or a memristive ferroelectric tunnel junction (FTJ), enabling independent programming of its devices while facilitating in-memory processing essential for edge computing.

Further advancements in the 1T1C architecture, specifically through the $C^2\text{FeRAM}$ approach, have improved endurance and energy efficiency, achieving four times better efficiency and a 200-fold increase in inference speed compared to traditional FeRAM. Additionally, integrating ferroelectric capacitors with HK/MG MOSFETs in FeMFET configurations enhances compatibility with standard CMOS processes at ultra-low write voltages, marking significant progress towards scalable and energy-efficient ferroelectric CiM systems for future intelligent devices [28,29].

Where do ferroelectric memories find a place in the memory hierarchy?: Ferroelectric memories exhibit exceptional promise for integration across various applications, particularly in storage-class memory (SCM), where they effectively bridge the performance gap between DRAM and NAND flash. While offering access times as low as 10–20 ns, DRAM is limited by its volatility. With higher latency (50–100 μs) and limited endurance (10^3 – 10^6 cycles), NAND flash struggles to meet the requirements of high-write

workloads. Ferroelectric memories, leveraging materials like doped HfO_2 , achieve sub-10 ns access times, endurance over 10^{10} , and retention capabilities spanning multiple years, making them viable for SCM applications.

As nonvolatile DRAM (nvDRAM), these

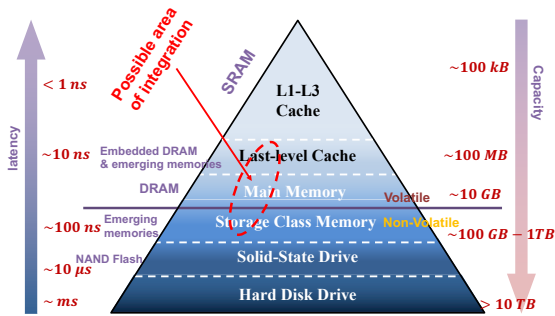


Fig. 3: Overview of semiconductor memory and possible areas of integration of ferroelectric memory

memories combine DRAM-equivalent speeds with nonvolatility, which is critical for servers, HPC systems, and real-time applications that demand high-speed data persistence during power interruptions. Furthermore, ferroelectric nonvolatile SRAM (nvSRAM) offers the speed (<5 ns) and energy efficiency of SRAM while enabling data retention, making it a compelling candidate for IoT and edge computing systems. With scalable 3D integration and densities rivaling NAND flash (terabit scale), ferroelectric memories can mitigate challenges like device scaling and thermal budgets, offering a pathway for next-generation memory solutions to replace or complement existing architectures. This technological leap positions ferroelectric memories as a cornerstone in evolving semiconductor memory hierarchies [30-35].

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