A GaN-Based Three-Level Dual Active Half Bridge Converter With Active Cancellation of the Steady-State DC Offset Current

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***Abstract*—The dual active bridge (DAB) is a widely used isolated DC-DC converter topology, particularly in automotive on-board charger (OBC) applications due to its high power density, inherent bidirectional power flow and reliability. Besides, the implementation of multilevel switching cells helps reduce the voltage stress in all devices, allowing the converter to be used in high voltage battery systems (600 V and higher). Due to circuit non-idealities, a steady-state DC offset current occurs at the transformer which leads to increased power losses, loss of zero-voltage switching and possibly magnetic core saturation. This paper discusses the physical implementation of an active cancellation method of the steady-state DC offset current, applied to a GaN-based three-level dual active half bridge (DAHB). The proposed method uses a duty cycle modulation in the primary half-bridge to compensate the non-ideal behavior of the devices. Experimental validation is done on a 1.5 kW three-level dual active half bridge converter based on 650 V GaN transistors.**

***Index Terms*—Dual active bridge (DAB), Offset current, On-board Charger, GaN, bidirectional, multilevel**

I. Introduction

Recently, EVs have been gaining popularity due to their contribution in reducing greenhouse gas by using cleaner energies [1] and their performance [2]. However, the range of EVs remains one of the major obstacle of the wide adoption of EV technology [3]. Reducing the weight of the power electronics while increasing the conversion efficiency can help increase the range of EVs. Furthermore, upgrading 400 V battery system to 800 V battery system helps to reduce the weight of the wiring harness and charging time [4].

Wide-bandgap (WBG) devices are expected to enable the next generation of EVs battery charging systems due to their performances such as low $R_{DS,on}$ and high switching frequency [5]. Silicon-carbide (SiC) and Gallium Nitride (GaN) materials are the best candidates for WBG devices due to their technological process maturity [6]. GaN in particular is suitable for medium power applications.

The Dual Active bridge (DAB) is a popular choice in automotive applications in general and in DC-DC stage in OBCs in particular [7] due to its high power density, high efficiency, ease of zero-voltage switching (ZVS), galvanic isolation, bidirectional power flow and reliability [8]. It is based on two bridges linked through a high frequency AC-link transformer, allowing bidirectional power flow. Advantages and disadvantages of different DAB configurations are presented in [9]. In 800 V OBCs DC-DC stage, the utilization of 650 V GaN HEMT devices, which are readily available, require the use of multilevel topologies to lower the voltage stress across the devices down to an acceptable level. Furthermore, multilevel topologies help reduce the voltage change rate dv/dt which reduce electromagnetic interference (EMI), as well as reduce the output voltage harmonic content. In addition, employing multilevel topologies in DAB converter generates additional voltage levels, which adds more control degrees of freedom [10] [11].

However, any mismatch between the different devices parameters, such as delay in gate signals, unequal turn-on and turn-off times and dispersion of the multiple devices $R_{DS,on}$ cause a steady-state DC offset current in the transformer which can lead to the magnetic core saturation.

This paper reports the physical implementation of a GaN-based three-level dual active half bridge (3-L DAHB) with active cancellation of the steady-state DC offset current. In section II, the operation of the 3-L DAHB with the dual phase shift control is explained. In addition, the DC offset current phenomenon is explained and the proposed solution in the literature are discusses. In section III, the active cancellation technique is presented and verified in simulation. The physical implementation of the 3-L DAHB converter as well as the active cancellation technique are detailed in section IV, and experimental results are discussed in section V.

II. Control of a 3-L DAHB converter

A. Modulation strategy of the 3-L ANPC leg

As shown in Fig. 1, the proposed three-level DAHB converter is made up of two three-level ANPC legs, one half-bridge on each side of the transformer. Each half-bridge consists of 6 active devices, and is able to generate a three-level voltage. S_1–S_8 are regular NPC switching devices, while D_1–D_4 are active clamping devices. Table I shows the switching

states corresponding to the three level voltage applied to the primary side ($\frac{V_{in}}{2}$, 0 and $-\frac{V_{in}}{2}$).

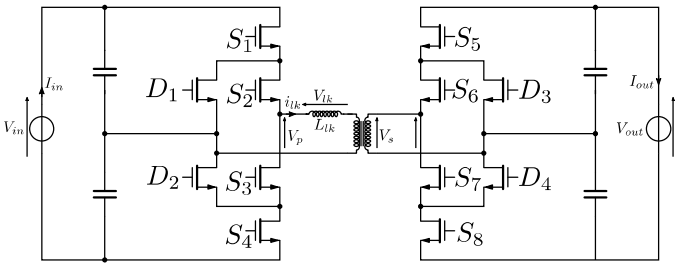

Fig. 1. The topology of the proposed bidirectional three-level ANPC dual active half bridge.

TABLE I
SWITCHING STATES OF A THREE-LEVEL ANPC HALF-BRIDGE

$S_1/\overline{D_1}$	S_2	S_3	$S_4/\overline{D_2}$	V_p
1	1	0	0	$\frac{V_{in}}{2}$
1	0	1	0	0
0	0	1	1	$-\frac{V_{in}}{2}$

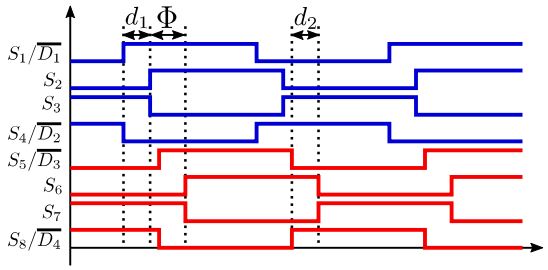

Fig. 2. PS-PWM gate drive signals applied to the three-level DAHB

Phase-Shifted Pulse Width Modulation (PS-PWM) is applied to the primary and secondary ANPC half-bridges in order to generate the three-level square voltage. Fig. 2 shows the gate drive signals of the different devices in the proposed converter, all devices switch at 50% duty cycle with a phase shift applied between the outer switches (S_1–S_4 and S_5–S_8) and inner switches (S_2–S_3 and S_6–S_7). The phase shift d_1 is applied to the primary half-bridge, while d_2 is applied to the secondary half-bridge. To simplify the analysis and the design of the proposed converter, d_1 and d_2 are considered equal and are referred to as d_1 in the following. PS-PWM modulation is selected for its multiple advantages such as natural voltage balancing of the different devices, even losses distribution and ease of implementation [12]. The natural voltage balancing is highly desirable as it eliminates the need of using sophisticated and resource-heavy active voltage balancing algorithms.

B. Power flow equation

Similar to the two-level DAB converter, the power flow of the three-level DAHB converter is controlled by adjusting the phase shift Φ between the two square voltages of the primary and secondary half-bridges. This phase shift creates a voltage across the series inductor, which leads to a power transfer from the leading half-bridge to the lagging half-bridge. The transferred power from the primary side to the secondary side is described by (1) [11], in which P_{out} is the average output power, ω is the switching angular frequency, and n is the turn ratio of the AC-link transformer. This equation is valid only in the case of $d_1 < \Phi < \frac{\pi}{2}$ [11]. The value and the direction (direct or reversed) of the transferred power can be controlled by choosing the appropriate combination of d_1 and Φ.

$$P_{out_{3L}} = \frac{n \cdot V_p \cdot V_s}{\omega \cdot L_{lk_{3L}}} \cdot (\Phi - \frac{\Phi^2}{\pi} - \frac{d_1^2}{\pi}) \quad (1)$$

$$P_{out_{2L}} = \frac{n \cdot V_p \cdot V_s}{\omega \cdot L_{lk_{2L}}} \cdot (\Phi - \frac{\Phi^2}{\pi}) \quad (2)$$

If $d_1 = 0°$ in (1), the equation is reduced to the conventional two-level DAB converter equation (2) [13]. Furthermore, under the same conditions (same power, frequency and input/output voltages), the ratio between the series inductance of the two-level DAB and three-level DAHB is always less than 1 (3). Thus, the series inductance value is smaller in three-level DAHB converter compared to the two-level DAB converter, eventually leading to greater compactness.

$$R = \frac{L_{lk_{3L}}}{L_{lk_{2L}}} = 1 - \frac{d_1^2}{\pi \cdot (\Phi - \frac{\Phi^2}{\pi})}, \; d_1 < \Phi < \frac{\pi}{2} \quad (3)$$

Fig. 3 shows the different theoretical waveforms of the three-level ANPC DAHB under the condition of $d_1 < \Phi < \frac{\pi}{2}$. This condition can be considered the generalized case [11].

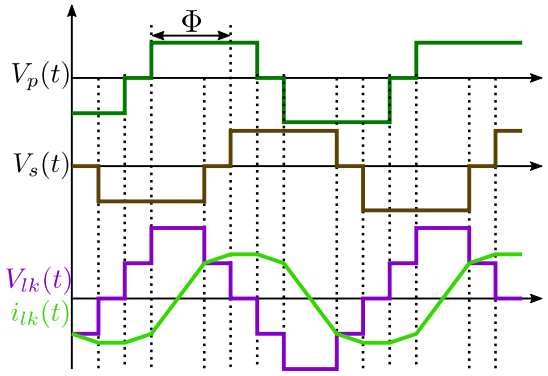

Fig. 3. Three-level DAHB converter waveforms

C. DC offset current

In practice, the mismatch between the different devices along with their non-ideal behavior lead to an unbalanced voltage applied to the transformer, which causes a DC component in the input current of the transformer. This DC current can cause magnetic core saturation, which translates to an increase of the conduction losses and loss of zero voltage switching (ZVS) [14]. Several solutions have been proposed to eliminate the problem of the steady-state DC offset current in two-level DAB converters. A straightforward method

consists in adding a DC blocking capacitor in series with the inductor L_{lk} [15]. However, the use of bulky series capacitors impacts considerably the power density and increases power loss. Adding an air-gap to the magnetic core decreases the permeability of the core, which makes the transformer more tolerable to the saturation [16]. Nonetheless, this method does not eliminate the DC component and leads to the decrease of the magnetizing inductance L_m which increases the RMS current. In [16], it is shown that by measuring the input current or the magnetic flux of the transformer, an active feedback loop can be implemented to eliminate the DC component by controlling the duty cycle of one or the two bridges of the DAB converter. In [17], the DC offset current is measured by implementing a digital averaging filter and then used to implement a feedback PI loop on the primary bridge of the DAB converter. This method requires the sampling frequency of the averaging filter to be much higher than the switching frequency, which can be difficult to implement without a very high performance controller. The steady state DC offset current is caused by both bridges of the DAB converter. Thus, in order to eliminate completely the DC offset current, [14] proposes a measure of the DC offset current on both sides of the transformer using Tunnel-Magnetoresistor (TMR) to implement two PI feedback loops. All the aforementioned methods are applied to the classic two-level DAB topology.

Multilevel DAB topologies have the same problem. Authors proposed to eliminate the steady state DC offset current in three-level DAB converter by adding a series capacitors on each side of the transformer [18]. This method increases the output voltage range. Nonetheless, it requires 200 µF high current capacitors, which considerably compromises the power density of the converter. In this paper, an active method is proposed to eliminate the steady state DC offset current without using series capacitors.

III. Active Offset Current Control Technique

As stated before, the switches of the three-level DAHB converter under dual phase shift modulation are operating at 50%. The proposed DC offset current cancellation solution consists of implementing an average current feedback loop that changes the duty cycle of the primary switches depending on the value of the DC offset current, while the secondary leg switches always operate at 50% duty cycle. This method does not require the introduction of additional bulky DC-blocking series capacitors. Fig. 4 shows the equivalent block diagram of the proposed solution. A measurement of the DC offset current is obtained by sensing the primary current and passing it through an analog low-pass filter.

A small-signal model from the duty cycle to the average input current of the transformer is derived using the method presented in [19]. The model helps to design a controller for eliminating the DC offset current.

A simulation model of the three-level DAHB converter is developed using *PLECS* to validate the proposed solution in eliminating the offset current. A positive DC offset current

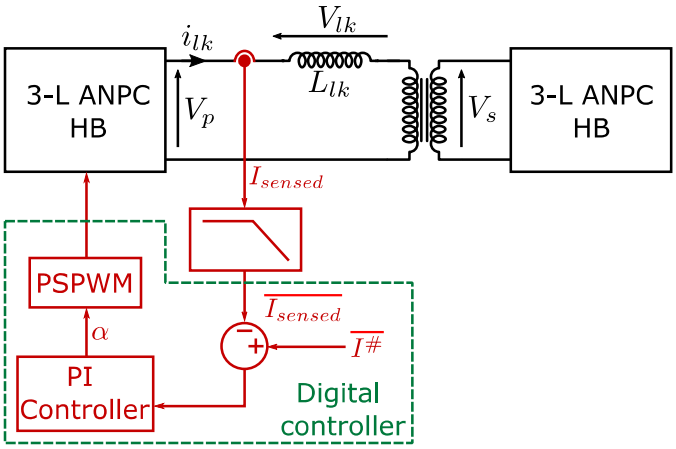

Fig. 4. Proposed controller for eliminating DC offset current in three-level DAHB

can be inserted into the simulation model by making S_1 non-ideal. The non-ideal behavior is introduced by changing the $R_{DS,on}$ of $S_1$1 from 0 mΩ to 125 mΩ. A negative DC offset can be inserted by changing the $R_{DS,on}$ of S_4. Fig. 5 shows the operation of the three-level DAHB converter with an inserted positive DC offset current of approximately 3 A.

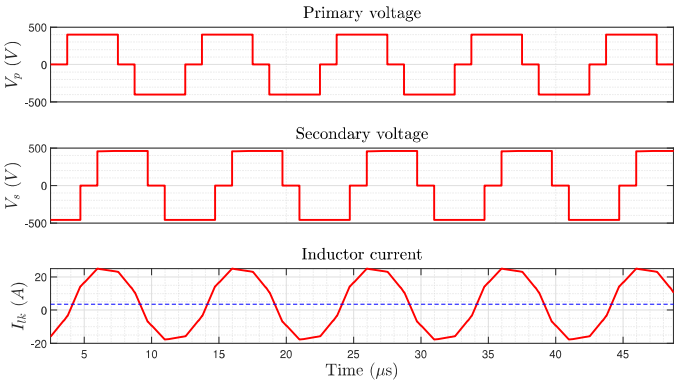

Fig. 5. 3-L DAHB converter waveforms with positive dc offset current.

Fig. 6 shows the waveforms of the three-level DAHB converter with the proposed controller. Since the DC offset current is positive, the controller compensates the unbalanced voltage of the primary half bridge by increasing slightly the duty cycle. The same can be done for negative DC offset current by reducing the duty cycle.

IV. Physical Implementation

The realized three-level DAHB converter is modular. Each ANPC leg is built as a motherboard with three daughter boards, as seen in Fig. 7. Each daughter board implements a GaN-based two-level half-bridge optimized for very low power loop stray inductance. The daughter boards are implemented using STMicroelectronics 650 V GaN HEMTs with a typical $R_{DS,on}$ of 75 mΩ. A series inductor is used to emulate a 1:1 transformer (without galvanic isolation). The main parameters of the realized prototype are given in Table II.

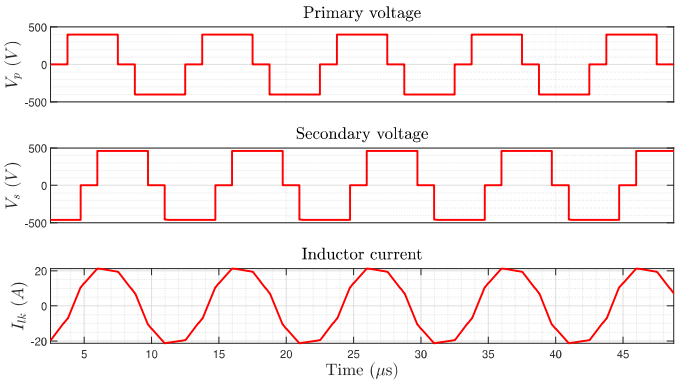

Fig. 6. 3-L DAHB converter waveforms with proposed controller

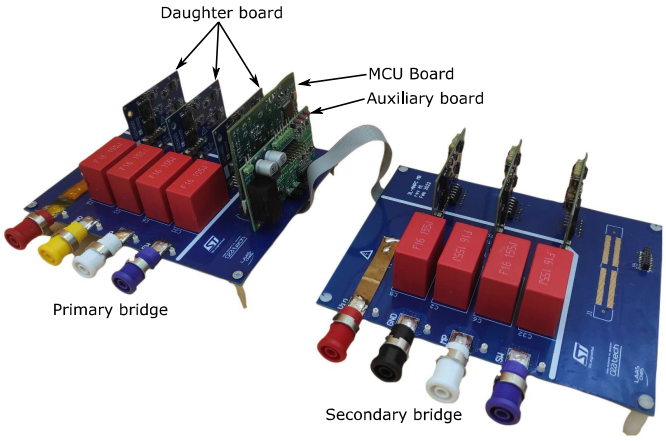

Fig. 7. View of the realized three-level DAHB converter

The dual phase shift modulation strategy used to control the power flow of the converter is implemented on a 32-bit MCU clocked at 100 MHz. The proposed DC offset cancellation controller is implemented on the same MCU. The transformer's input current is measured using a Hall-effect current sensor. Then, the sensed current is passed through a low-pass filter to extract the DC offset current, which is used by the MCU to perform the appropriate duty cycle modulation.

V. Experimental Results

Fig. 8 shows the measured input offset current of the transformer with and without the active cancellation technique.

TABLE II
Parameters of the Three-Level DAHB Converter

Parameter		Value		
		Min	Typ.	Max
Input voltage	V_{in}	600 V		800 V
Output voltage	V_{out}	600 V		800 V
Rated output power	P_{out}			3300 W
transformer turns ration	n_p/n_s		1:1	
Switching frequency	f_{sw}		100 kHz	
Series inductor	L_{lk}		47 µH	

The offset current values are extracted for V_{in} = V_{out} = 600 V and for different output current values up to P = 1.5 kW.

The offset current of the three-level DAHB without active cancellation was measured only up to 450 W as it reaches a significant value (1.9 A) which could saturate the magnetic core and eventually damage the converter. The offset current values for the remaining output current values are extracted using the simulation model. On the other hand, the offset current is kept under 20 mA using the implemented active cancellation technique. The implemented technique works over the entire output power range.

Fig. 9 shows the experimental waveforms of the three-level DAHB converter with the active cancellation technique for V_{in} = V_{out} = 600 V and P_{out} = 1.5 kW. In the example shown, the implemented cancellation technique adjusts the duty cycle of the primary half-bridge to 54.6% to compensate for switching devices non-idealities. Furthermore, this additional control technique has no noticeable effect on the converter operation is negligible. In this work, the controlled 3-L DAHB converter achieves a peak efficiency of 98.25%.

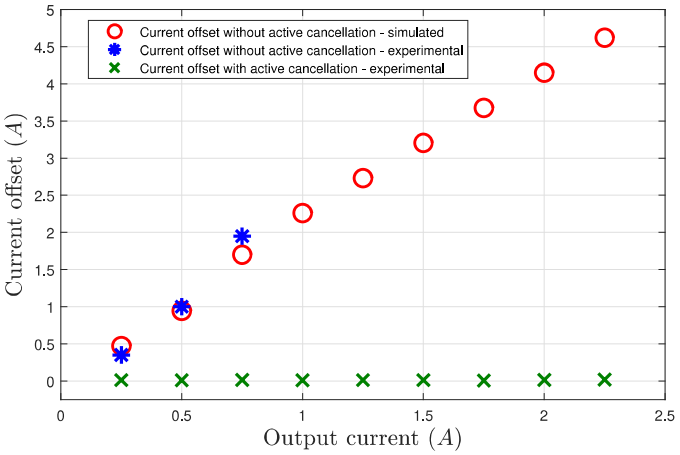

Fig. 8. Offset current vs. output current in the three-level DAHB with and without active cancellation. V_{in} = V_{out} = 600 V

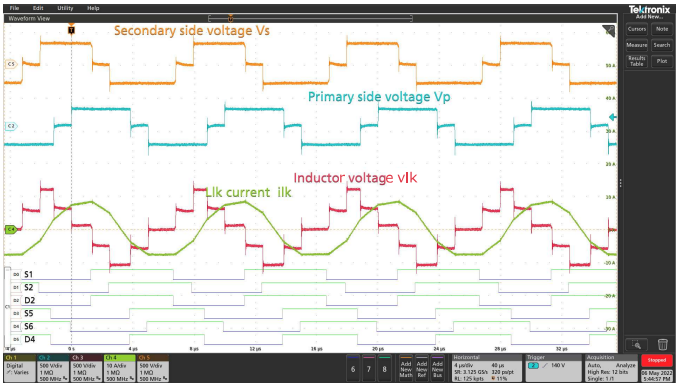

Fig. 9. Experimental waveforms of the three-level DAHB converter with active cancellation of the steady state DC offset current. V_p (blue) 500 V/div, V_s (orange) 500 V/div, V_{lk} (red) 500 V/div, i_{lk} (green) 10 A/div

VI. Conclusion

This paper has presented the design and realization of a GaN-based three-level DAHB converter for high voltage automotive OBC applications. The converter works under dual-phase shift modulation and features an active control method for cancelling the steady state DC offset current. The converter design and its control have been verified in simulation. Experimental validation has been done using a 1.5 kW prototype, on which the implemented active cancellation technique has shown to work over a wide range of output power. This technique eliminates the need for bulky and expensive DC-blocking capacitors, which eventually leads to a better power density.

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