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# Transient thermal simulation of a SiP FO-WLP embedding a GaN power amplifier

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**Abstract** - This article presents various multi-physics and multi-scale simulation activities conducted within the framework of the SMART3 project of the Nano2022 plan. The main objectives are to evaluate and develop a new generation of 2D and 3D packaging to address the heterogeneous integration of different semiconductor technologies for designing fully integrated systems (SiP). The project focuses particularly on the Fan Out Wafer Level Packaging (FO-WLP) [1] technology. As an illustrative example, a study is conducted on a Test Vehicle (TV) equipped with a GaN power amplifier (PA). The analyses presented aim to ensure the proper functioning and reliability of the device under a specified temperature threshold, considering its reference temperature and the required maximum dissipated power. Additionally, the article explores the impact of geometric scale ratio in a transient thermal study, as well as the coupling between different stages of the TV. Due to thickness variations among different layers, the transition between GaN and SiC will be modeled using a Thermal Contact Conductance (TCC) [2] [3]. Its significance in simulation and its consideration will be discussed in detail.

**Keywords** – Fan-Out Wafer Level Packaging (FO-WLP), measurements, numerical modeling and simulation, thermal, GDS, HEMT GaN, System in Package (SiP)

## INTRODUCTION

This study involves validating the device's performance over time through a transient thermal analysis. This analysis aims to determine not only the time it takes for the device to reach its steady state but also to assess the influence of the scale ratio of the different layers on this study. As discussed in the article [4], a steady-state thermal analysis was conducted following specific steps, and we will proceed similarly for this transient thermal analysis. In the case of SiP assembled on a PCB, it should be noted that the multilayer PCB will be exposed. Improvements have been made to the previous structure defined in [4]. We have added two passivation layers and a significant BCB layer to protect the

active part of the device and to be used for future thermomechanical study on the assembly reliability of the device.

## METHODOLOGY

To address the outlined issues, the following steps were undertaken : begin by using the 2D GDS [5] file provided by the UMS foundry. This file serves as the initial basis for the design. The Figure 1 gives the methodology used for the creation of the TV4x4 RIC with ANSYS Workbench. This device has a dimension of 4x4 mm<sup>2</sup>.

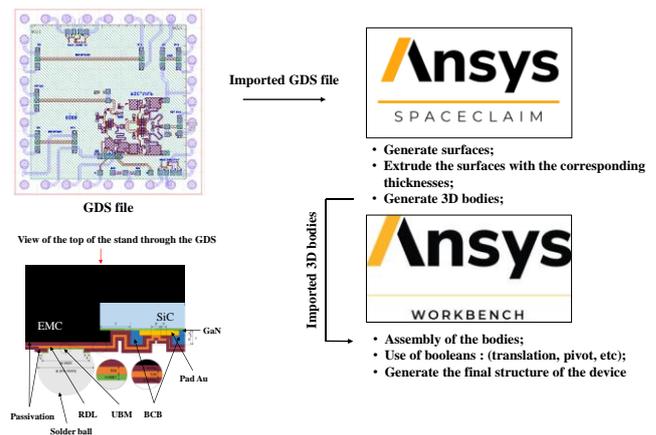


Figure 1 : The methodology used for the conception of the device geometry

This methodology results in the structure shown in Figure 2. This structure consists of: GaN, SiC, SiN, BGA ball, via hole, passivation, BCB (Benzocyclobutene), UBM (Under Bump Metallization), RDL (Redistribution Layer), epoxy resin, the active part made of gold, and two thermal sensors used to monitor temperature during electrical measurement. Details in Figure 3 show that there are three transistors: one transistor in stage 1 and two transistors in

stage 2. It also provides the composition of a GH15 transistor.

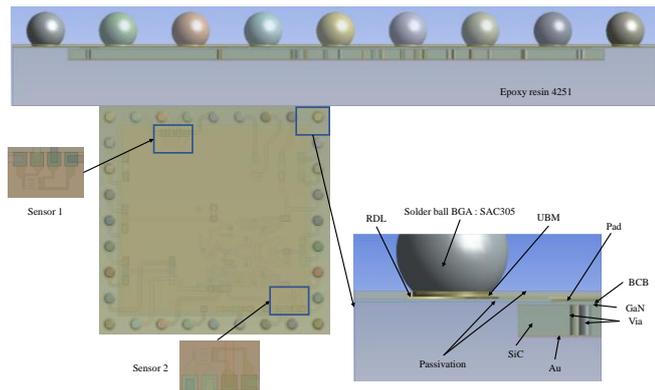


Figure 2 : final structure of the TV4x4 RIC obtained with ANSYS Workbench

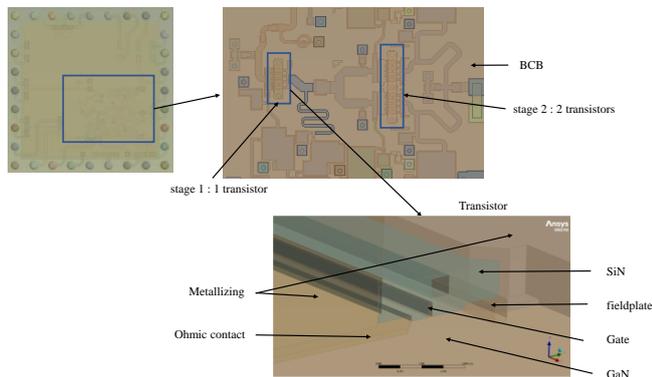


Figure 3 : Details of the TV4x4 RIC

- GH15 8x60  $\mu\text{m}$  transistor transient thermal study for model and assembly validation

Upon completing the assembly, it's crucial to validate the full model. We start first at the transistor level and we isolate a transistor, such as the GH15 8x60  $\mu\text{m}$  transistor [6] (Figure 4), from the structure of the TV4x4 RIC.

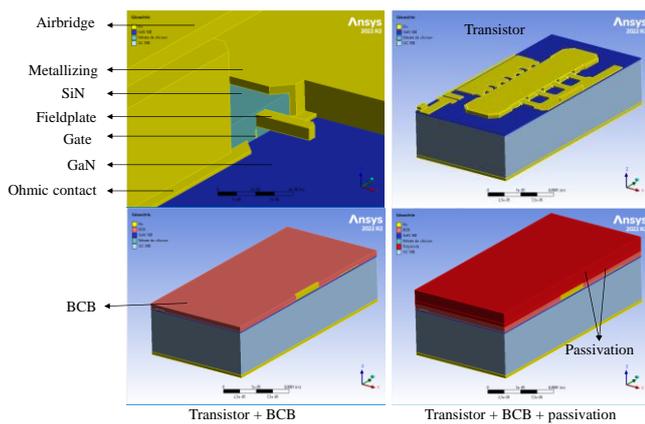


Figure 4 : Transistor GH15 8x60  $\mu\text{m}$

Then we perform transient thermal simulation to this isolated transistor. This simulation is then compared with data provided by the UMS foundry regarding this technology type. The transient thermal simulation step on ANSYS Workbench software is defined on the Figure 5.

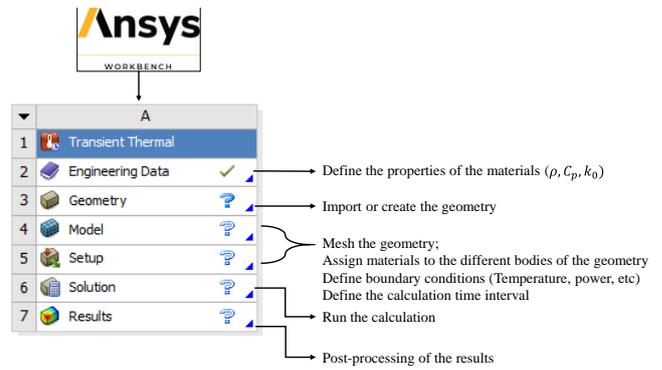


Figure 5 : Transient thermal simulation step on ANSYS Workbench

This typically involves applying power dissipation at the Gates feet and imposed a reference temperature under the backside of the GH15 8x60  $\mu\text{m}$  transistor see Table 2. The different materials and their thermal conductivity are defined in the Table 1.

Materials	$k_0$ (W/m $^{\circ}$ C)	$n$	$C_p$ (J/Kg/ $^{\circ}$ C)	$\rho$ (Kg/m $^3$ )
Silicon Carbide (SiC)	390	1.5	390	3220
Gallium nitrite (GaN)	160	1.45	490	6100
Nickel (Ni)	90	-	444	8900
Gold (Au)	315	-	137	19300
Copper (Cu)	390	-	500	8300
BCB	0.40	-	500	8300
EMC : Epoxy resin	0.65	-	236	1820
Solder Ball (SAC 305)	60	-	232	7370
Silicon Nitrate (SiN)	16	-	691	2400
FR4	$k_{0x}$	0.38	1200	1840
	$k_{0y}$	0.38		
	$k_{0z}$	0.3		

Table 1 : Materials properties

The density and heat capacity are assumed to be constant with temperature for all materials. The thermal conductivity of GaN and SiC obeys equation (1) defined below:

$$k(T) = k_0 \cdot \left(\frac{T}{300}\right)^{-n} \quad \#(1)$$

Once the simulation is executed, the results are analyzed thoroughly and validated with known data and measurements. The results of the transient thermal study are shown in Figure 6, Figure 7 and Table 2.

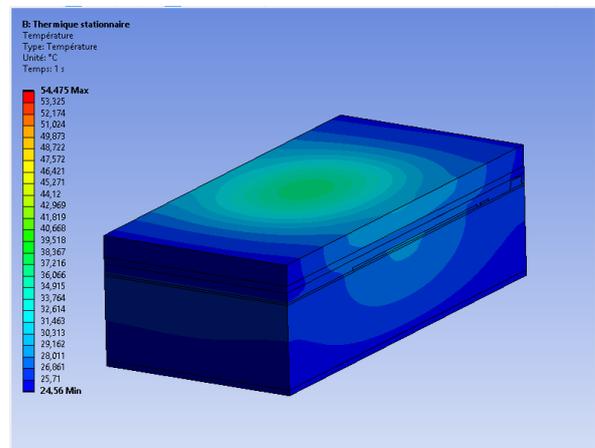


Figure 6 : Thermal simulation of GH15 8x60  $\mu\text{m}$  transistor

	Data Project [7]	Result of the simulation
Number of gate fingers	8	8
Gate width ( $W_g$ )	60 $\mu\text{m}$	60 $\mu\text{m}$
Chip backside temperature ( $T_o$ )	25 $^{\circ}\text{C}$	25 $^{\circ}\text{C}$
Dissipated power ( $P_{\text{diss}}$ )	$\sim 1.17$ W	$\sim 1.17$ W
Max. temperature ( $T_{\text{jmax}}$ )	57 $^{\circ}\text{C}$	54 $^{\circ}\text{C}$
Thermal resistance ( $R_{\text{th}}$ )	27 $^{\circ}\text{C}/\text{W}$	$\sim 25$ $^{\circ}\text{C}/\text{W}$

Table 2 : Comparison of results (measurement and simulation) for the GH15 8x60  $\mu\text{m}$  transistor

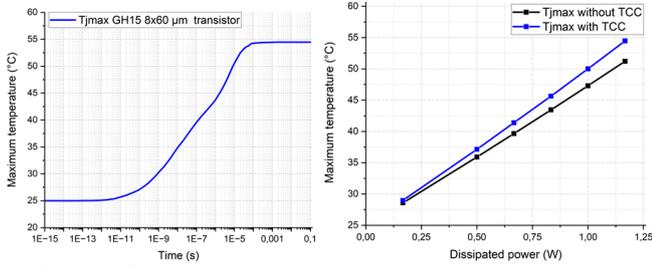


Figure 7 : Transient response curve and effect of the thermal contact conductance (TCC)[8] on the (transient and steady-state) thermal simulation results of the GH15 8x60  $\mu\text{m}$  transistor

These results are in a good agreement with the values provided by UMS and measurements already performed on the same technology, ie  $27 \times 0.48 = 13$  mm. $^{\circ}\text{C}/\text{W}$  [7]. Steady-state conditions for this study are reached after 70  $\mu\text{s}$ . In Figure 7, we observe the effect of the thermal contact conductance on the simulation. We notice that at low dissipated powers, there is no difference between the results obtained with or without this coefficient (for example, for low dissipated power). However, as the dissipated power increases, the difference between the results becomes more pronounced. Thus, this coefficient proves to be crucial in numerical simulation. With high dissipated power, the temperature difference reaches 4 $^{\circ}\text{C}$ . The thermal conductance coefficient used in this study at 1.17 W is  $6.78 \times 10^7$  W/m $^2$ / $^{\circ}\text{C}$ .

#### TV 4x4 RIC transient thermal Study

Upon successful validation, we can extend the study to the complete system, ensuring that all components and interactions are considered in the thermal analysis. By following these steps, we can effectively address the issues related to the design and thermal performance of the circuit, ensuring its reliability and functionality. For this study, we expected the test vehicle to be powered by a nominal voltage  $V_d = 25$  V and current  $I_d = 140$  mA, producing a nominal dissipated power equal to 3.5 W, corresponding approximately to 1.17 W for each transistor of TV4x4 RIC. The reference temperature ( $T_{\text{ref}}$ ) applied to the top of the epoxy resin EMC is chosen equal to 25  $^{\circ}\text{C}$ . The objective of this analysis is to evaluate the reliability and the maximum allowable thermal operating conditions (power dissipation and reference temperature) of the SiP assembled on a PCB to represent its real operating conditions. Indeed the maximum temperature ( $T_{\text{max}}$ ) of the TV 4x4 RIC and TV4x4 RIC assembled on a multilayer PCB must stay below 200 $^{\circ}\text{C}$ .

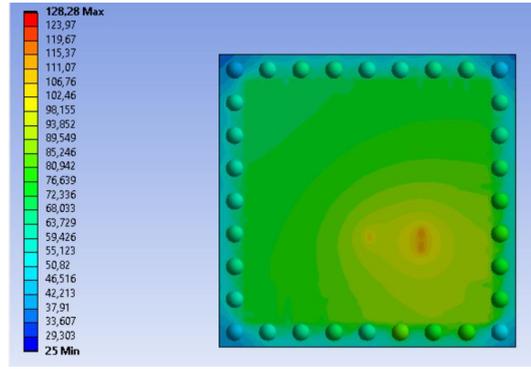


Figure 8 : Thermal simulation of the TV4x4 RIC at the reference temperature of 25  $^{\circ}\text{C}$  and dissipated power of 2 W.

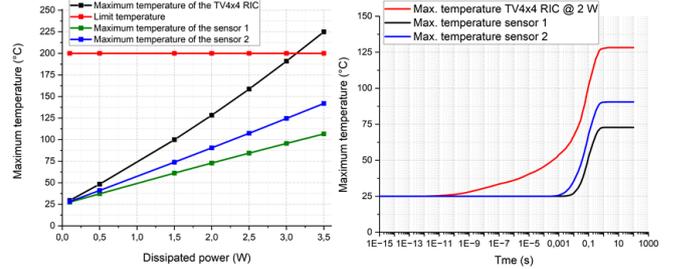


Figure 9 : left/ Determination of the critical dissipated power of the TV4x4 RIC at the reference temperature of 25  $^{\circ}\text{C}$ , right/ Transient curve of the TV4x4 RIC and integrated sensors

According to Figure 8 the total dissipated power limit for this device with a reference temperature of 25  $^{\circ}\text{C}$  is equal to 3 W. However, if the reference temperature increases, the dissipated power limit should be reduced. To stay on the safe side, we will assume that the dissipated power limit is 2 W may be 2.5 W. This value is better because as the reference temperature increases, there is more margin to reach the maximum temperature target. The TV4x4 RIC reaches its steady state after 2 s; its representative curve is the red one. Sensor 2 (blue curve) reaches its steady state after 0.8  $\mu\text{s}$  and sensor 1 (black curve) reaches her steady state after 0.6  $\mu\text{s}$ .

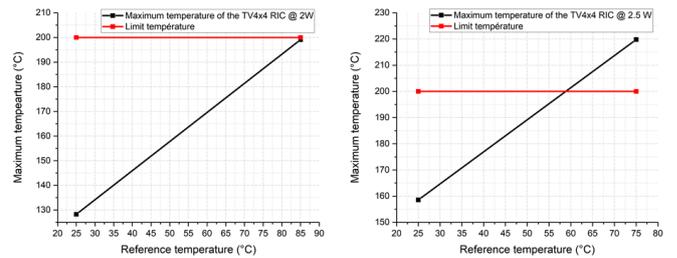


Figure 10 : Limit reference temperature of the TV4x4 RIC to reach the maximum operating temperature of 200  $^{\circ}\text{C}$  : left/ dissipated power of 2 W, right/ dissipated power of 2.5 W.

This hypothesis is supported by Figure 10. We can clearly see that the reference temperature can rise up to 85  $^{\circ}\text{C}$  for 2 W and 58  $^{\circ}\text{C}$  for 2.5 W before reaching the maximum peak junction temperature limit.

	Interstage coupling TV4x4 RIC - P <sub>dis</sub> @ 2 W et T <sub>ref</sub> @ 25 °C				
	Stage 1 ON	Stage 21 ON	Stage 22 ON	Stage 21 & 22 ON	Stage 1 & 21 & 22 ON
	Stage 21 & 22 OFF	Stage 1 & 22 OFF	Stage 1 & 21 OFF	Stage 1 OFF	
T <sub>jmax</sub> (°C)	44.042	44.767	44.866	65.238	85.199
T <sub>average</sub> Sensor 1 (°C)	41.503	40.833	40.51	55.93	71.737
T <sub>average</sub> Sensor 2 (°C)	43.874	46.518	47.805	69.811	89.174
T <sub>average</sub> stage 1 (°C)	68.175	45.542	45.634	66.453	114.53
T <sub>average</sub> stage 21 (°C)	45.55	69.184	51.599	99.427	123.39
T <sub>average</sub> stage 22 (°C)	45.645	51.605	69.728	100.02	124.15

	Interstage coupling TV4x4 RIC - P <sub>dis</sub> @ 2 W et T <sub>ref</sub> @ 25 °C				
	Stage 1 ON	Stage 21 ON	Stage 22 ON	Stage 21 & 22 ON	Stage 1 & 21 & 22 ON
	Stage 21 & 22 OFF	Stage 1 & 22 OFF	Stage 1 & 21 OFF	Stage 1 OFF	
T <sub>jmax</sub> (°C)	71.773	72.521	73.182	103.88	128.28
T <sub>maximum</sub> Sensor 1 (°C)	41.78	41.185	40.834	56.645	72.801
T <sub>maximum</sub> Sensor 2 (°C)	44.2	46.872	48.262	70.71	90.501
T <sub>maximum</sub> stage 1 (°C)	71.773	45.707	45.908	66.921	118.65
T <sub>maximum</sub> stage 21 (°C)	45.729	72.521	53.347	103.6	127.88
T <sub>maximum</sub> stage 22 (°C)	45.765	53.192	73.182	103.88	128.28

Table 3 : Inter-stage coupling of the TV4x4 RIC for a nominal dissipated power of 2 W and a reference temperature of 25 °C

The blue curve (sensor 2) and the green curve (sensor 1) illustrate the evolution of the maximum temperature of the sensors as a function of the dissipated power (Figure 9). Analysis of the interaction between the different stages reveals that sensor 1 cannot indicate which transistor of stage 1 or stage 2 is powered, as its temperatures remain constant regardless of the stage. In contrast, sensor 2 shows temperature variations, allowing this information to be identified, as indicated in Table 3.

	Transistor GH15 8x60 μm	TV4x4 RIC with one transistor powered
Number of gate fingers	8	8
Gate width (W <sub>g</sub> )	60 μm	60 μm
Imposed temperature T <sub>ref</sub> = 25 °C	Chip backside	Epoxy resin EMC backside
Dissipated power (P <sub>dis</sub> )	~ 1.17 W	~ 1.17 W
Max. temperature (T <sub>jmax</sub> )	54 °C	112 °C
Thermal resistance (R <sub>th</sub> )	~ 25 °C/W	~ 75 °C/W

Table 4 : the impact of geometric scale ratio

In Table 4, we observe the impact that the geometry scaling ratio can have. Referring to the results of the isolated transistor and the one within the package or SiP, both powered alone with the same dissipated power of approximately 1.17 W, we see a temperature change from 54 °C to 112 °C, a difference of 58 °C. This difference is due to the environment in which the transistor is located as well as the boundary conditions and the poor thermal conductivity of the EMC.

- Transient thermal study TV4x4 RIC assembled on a multilayer PCB

The multilayer PCB consists of 11 layers of FR-4 dielectric and 12 layers of copper. The PCB dimensions are 40x40x1.807 mm<sup>3</sup>. Figure 11 is used to perform thermal characterization of the proper functioning and reliability of the device.

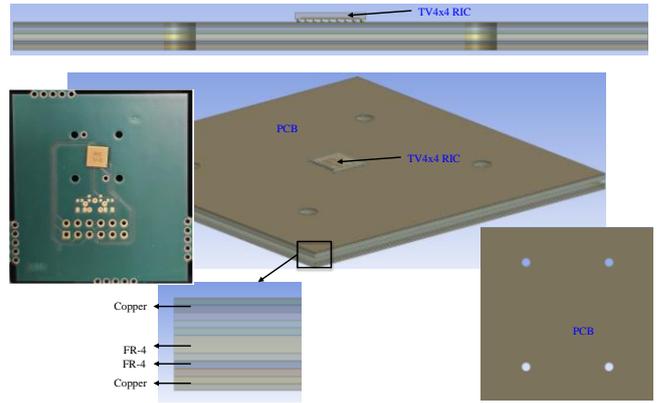


Figure 11 : TV4x4 RIC assembled on a multilayer PCB

We are aiming to dissipate the heat accumulated by the device, in order to meet the total nominal dissipated power of 2 W. Due to the absence of an integrated heatsink within the device, heat dissipation occurs solely through the BGA balls connected to a multilayer PCB. The boundary conditions used are as follows: a dissipated power of 2 W applied to the legs of the grids of the three transistors, resulting in approximately 0.67W per transistor; a temperature of 25°C applied to the back side of the PCB; and the initial temperature is set to 25°C.

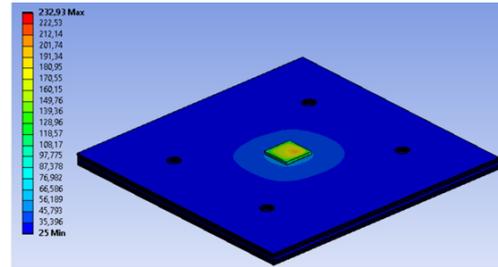


Figure 12 : Thermal simulation of TV4x4 RIC assembled on a multilayer PCB

To dissipate heat considering the result from Figure 12, we assume that the device is exposed to ambient air using natural convection, or with the aid of a ventilation device to add forced convection to the previous boundary conditions. The various results are listed in Table 5. To optimize heat dissipation, we opt for forced convection with a heat transfer coefficient of  $h = 200 \text{ W/m}^2/\text{°C}$ , providing sufficient margin to adjust the reference temperature and achieve a maximum temperature of 200 °C. We could have chosen  $h = 100 \text{ W/m}^2/\text{°C}$ , but this would limit the maximum reference temperature to around 30 °C.

Simulation	Max. temperature
Without convection	232.93 °C
With convection $h = 5 \text{ W/m}^2/\text{°C}$ [9]	230.66 °C
With convection $h = 25 \text{ W/m}^2/\text{°C}$ [9]	222.24 °C
With convection $h = 100 \text{ W/m}^2/\text{°C}$ [9]	197.74 °C
With convection $h = 200 \text{ W/m}^2/\text{°C}$ [9]	176.25 °C

Table 5 : steady-state thermal analysis result of the TV4x4 RIC assembled on a multilayer PCB for a nominal dissipated power of 2 W and a reference temperature of 25 °C

Setting the heat transfer coefficient  $h = 200 \text{ W/m}^2/\text{°C}$  and selecting a maximum reference temperature of 100 °C results in a maximum temperature of 203.75 °C. To achieve a temperature of 200 °C, it is necessary to choose a

reference temperature of 90 °C, which corresponds to the intersection point between the maximum temperature curve of the TV4x4 RIC assembled on a multilayer PCB and the temperature limit curve (see Figure 13).

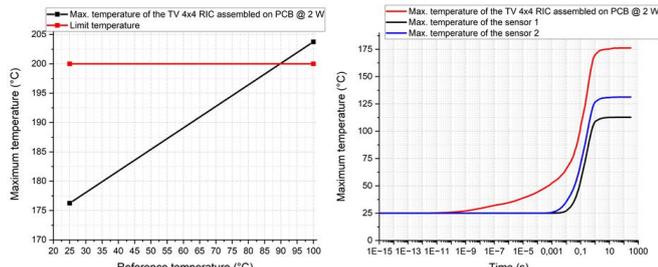


Figure 13 : left/ Limit reference temperature of the TV4x4 RIC assembled on PCB of 2 W to reach the maximum operating temperature of 200 °C. right/ Transient curve of the TV4x4 RIC assembled on PCB and integrated sensors of 2 W

Figure 13 also shows the transient thermal analysis of the TV4x4 RIC mounted on a multilayer PCB. Both the device and sensor 2 reach steady state at 20 s, while sensor 1 reaches steady state at 4 s. (inverse entre 1 et 2)

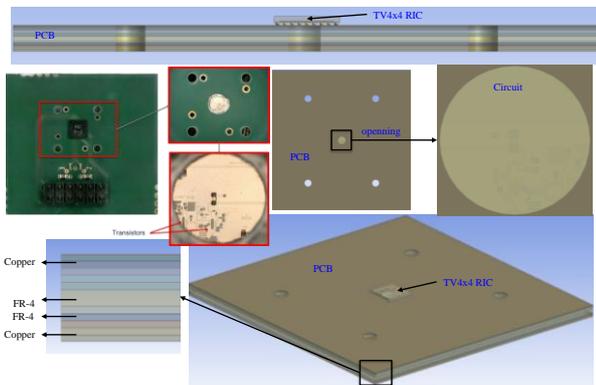


Figure 14 : TV4x4 RIC structure used for electrical and infrared measurements

Figure 14 shows the design used to perform infrared and electrical measurements. The electrical measurement is conducted at the sensors. These sensors enable temperature monitoring through the connections shown in Figure 14.

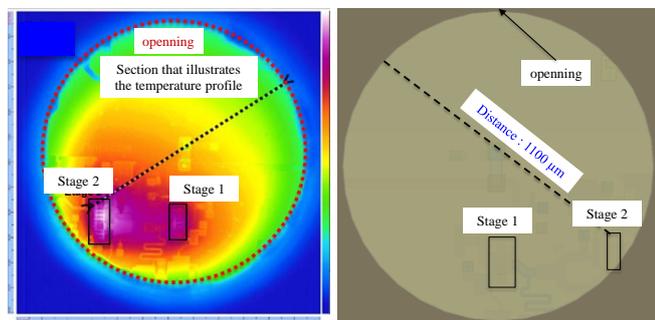


Figure 15 : Infrared measurement zone

Figure 15 shows the opening that provides access to the active part of the TV4x4 RIC, allowing for infrared measurement. The infrared measurement is conducted along a trajectory from stage 2 to sensor 1 (Figure 15). Since we do not have access to sensor 1 due to the limitation of the opening, we will restrict our measurements to the boundary

of the opening. The measurement results are listed in Table 6. For the simulation, the applied boundary conditions consist of imposing a temperature on the back side of the EMC, while the other faces are subjected to convection with a heat transfer coefficient of  $h = 25 \text{ W/m}^2/\text{°C}$ , an external temperature of 25 °C, and a dissipated power applied to the transistors. The power values are illustrated in Table 6.

Dissipated power (W)	Temperature stage 2 - sensor 1	Temperature sensor 1	Average temperature stage 2 - sensor 1
	Extrapolation of infrared measurement	Electrical measurement	Thermal simulation
1.9	124 °C	122 °C	126.46 °C
2.6	141 °C	138 °C	142.58 °C

Table 6 : Comparison of measurement and simulation results from sensor 1 at reference temperature of 100 °C

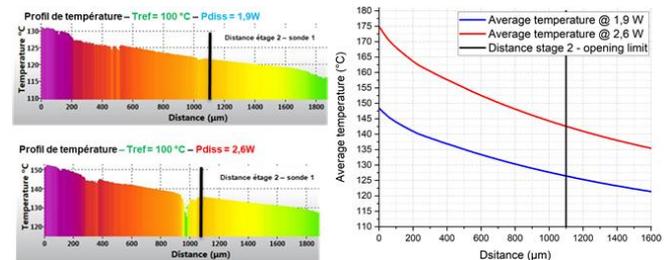


Figure 16 : Comparison of infrared results and simulation of the distance from stage 2 to the opening boundary at reference temperature of 100 °C, left/ infrared result, right/ simulation result

Figure 16 and Table 6 show a good agreement between measurement results and simulation results, thereby validating the presented findings.

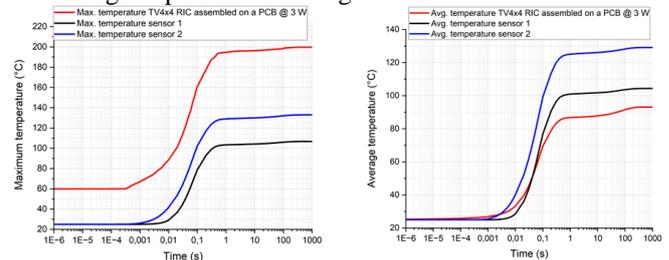


Figure 17 : Transient thermal study of the TV4x4 RIC assembly on PCB device used for thermal measurement: left/ maximum temperature values, right/ average temperature values

Under the conditions of the electrical measurement, we observe that a dissipated power of 3 W is required for the device to reach a maximum temperature of 200 °C. The reference temperature is 60 °C, with a convective coefficient of 25 W/m<sup>2</sup>/°C and an ambient temperature of 25 °C. In this context, Figure 17 shows that the device reaches its steady state at the maximum value after 120 s, while sensors 1 and 2 reach theirs after 100 s. For the average temperature, the device reaches its steady state after 290 s, sensors 1 reaches its steady state after 150 s and sensors 2 reaches its steady state after 220 s. (Explain the difference with your simulation!)

## CONCLUSION

This article presents the methodology adopted within the SMART3 project for the evaluation and development of SiPs (System in Packages). A campaign of measurements and simulations has been carried out to validate the project's

devices. For future work, despite time constraints, thermorefectance measurements will provide additional insights by comparing them with electrical, infrared measurements, and simulations results. In parallel of this work, a thermomechanical study of TV4x4 RIC will be completed. Results will be compared to measurement data obtained Topography Deformation Measurement (TDM) scans.

#### ACKNOWLEDGMENT

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