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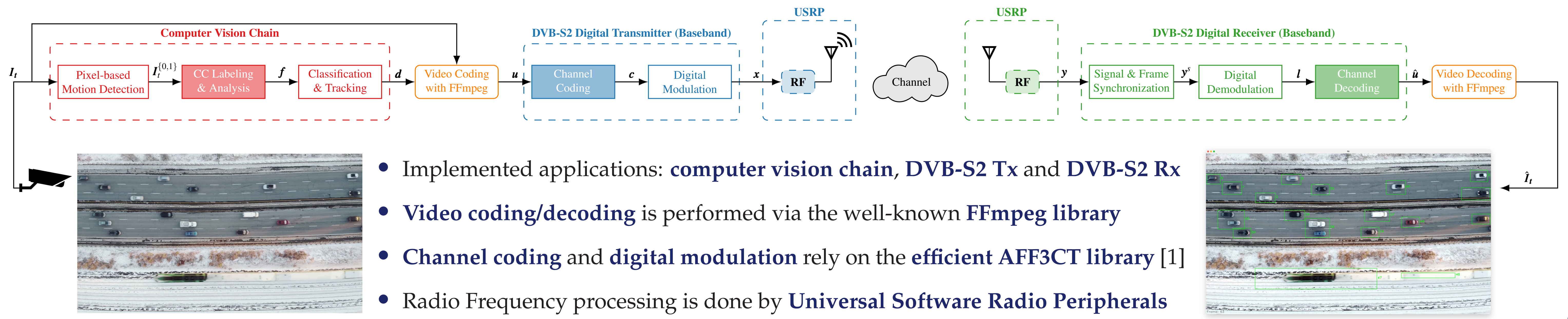


# Combined Computer Vision and SDR Transmission on Multicore CPUs

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## DEMONSTRATION OF A FULL DVB-S2 TRANSCIVER IN SOFTWARE WITH MOTION DETECTION



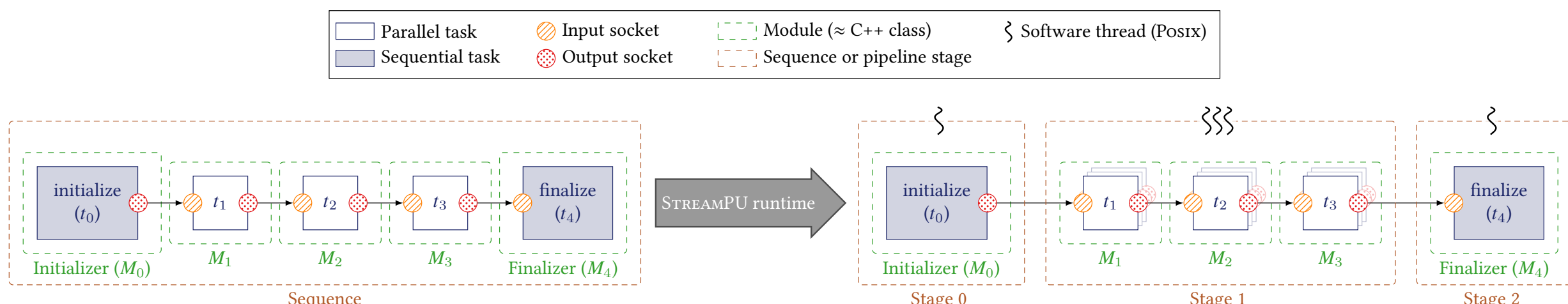
## STREAMPU LANGUAGE & RUNTIME [2]

Domain Specific Embedded Language into C++: Core of the AFF3CT library

- Dedicated to **streaming applications**: Static dataflow graph (mainly)

Multithreaded runtime based on portable C++11 threads

- Pipeline with  $1 \rightarrow n$  and  $n \rightarrow 1$  **efficient producer-consumer** implem
- **Simplified replication** of parallel stages



## HARDWARE SPECIFICATIONS



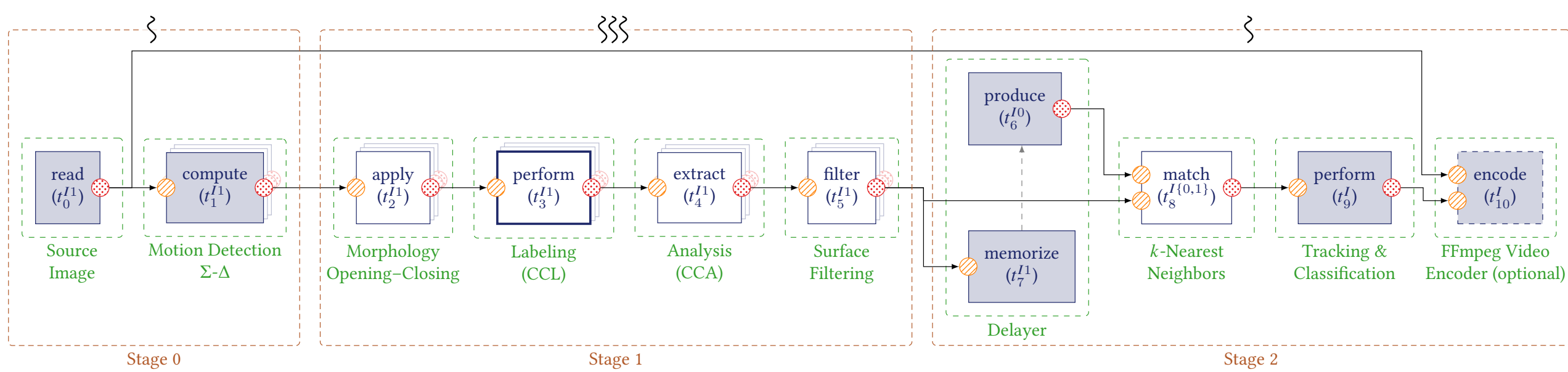
2× **Minisforum Mercury EM780**

- AMD **Ryzen 7 7840U** CPU
  - 8 × Zen 4 core @ 3.3 GHz
  - TSMC **4nm** FinFET
  - Config. **15 W** to 28 W TDP
- 32 GB of LPDDR5 RAM
- Dimensions: **80×80×43 mm**

2× **Ettus Research USRP B200mini**

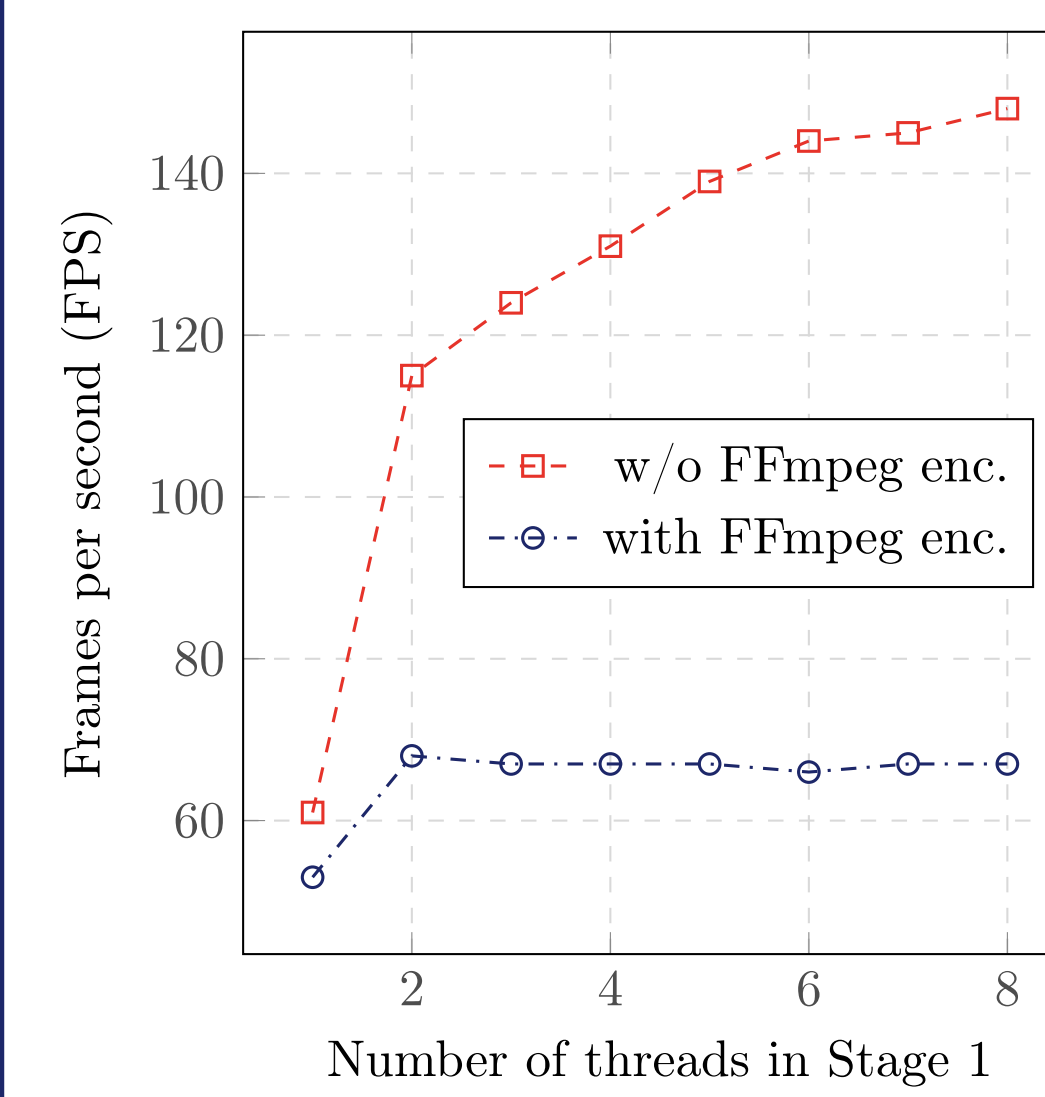
- Freq. range: **70 MHz – 6 GHz**
- Max 56 MHz instant. bandwidth
- Prog. Xilinx **Spartan-6** FPGA
- USB 3.0 data & bus-powered
- Dimensions: **83.3×50.8×8.4 mm**

## COMPUTER VISION CHAIN



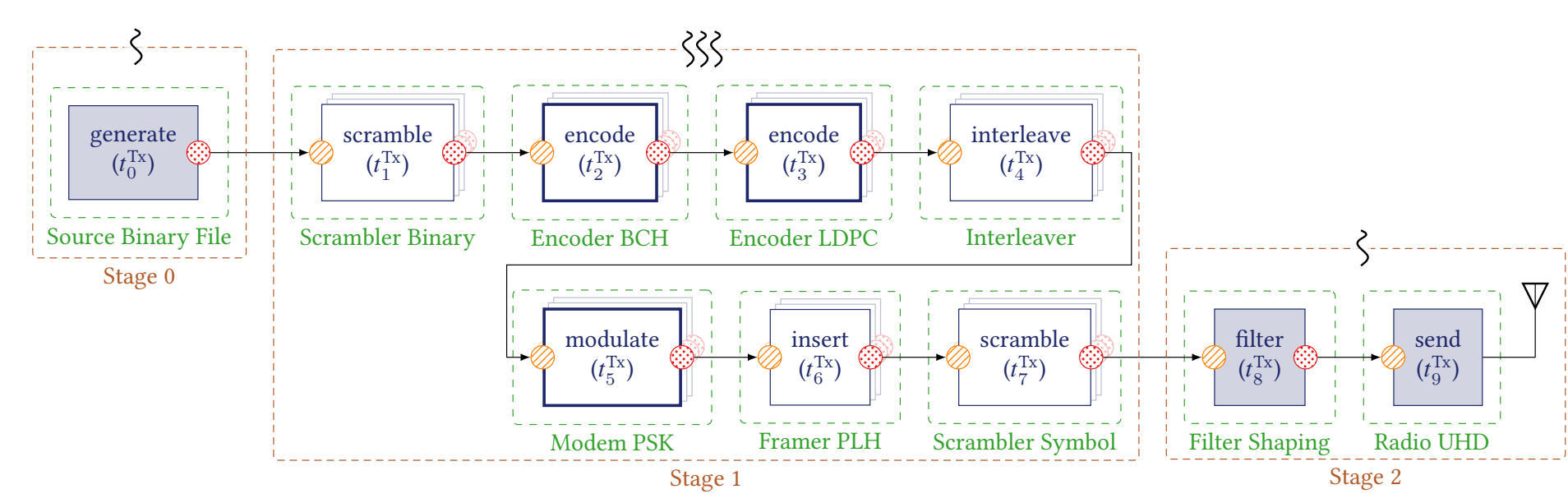
- $\Sigma$ - $\Delta$  ( $t_1^1$ ): Detects **pixels that moved between two consecutive frames**
  - Strong assumption: **Brightness is constant** and no camera movement
- **Connected-Component Labeling** ( $t_3^1$ ) is the **most time-consuming part**
  - Efficient **Light Speed Labeling (LSL)** algorithm [3] is used

## COMPUTER VISION – MEASURED PERFORMANCE



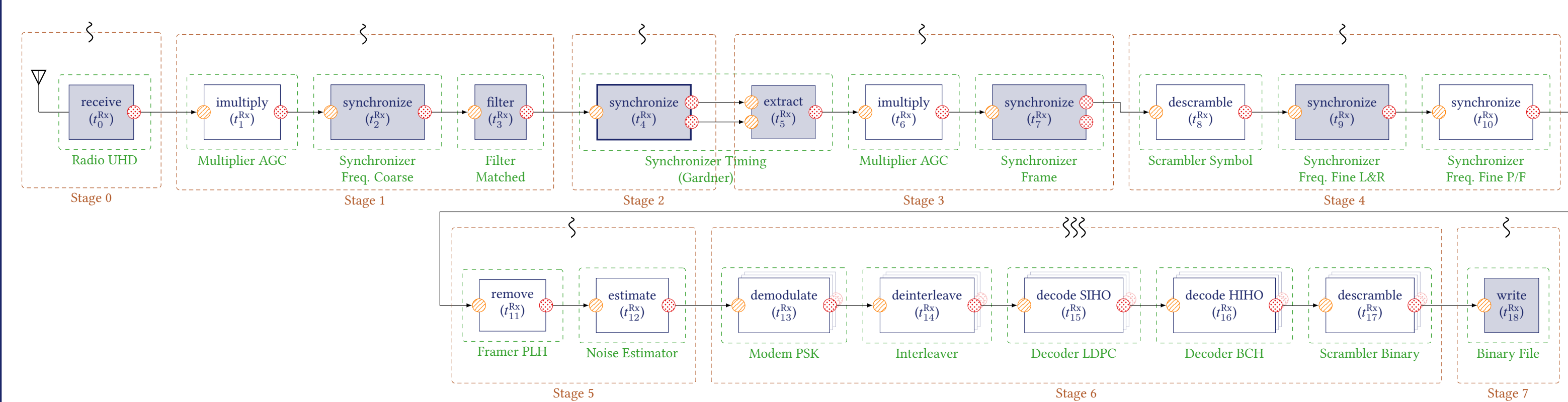
- Frame format: 1920×1080 pixels, 8-bit gray
- Running on the AMD Ryzen 7 7840U
- Motion detection & object tracking **benefit from multicore CPUs** (without  $t_{10}^1$  task)
  - Up to **148 FPS** on 8 cores
- **BUT the bottleneck is the video encoding**
  - SW enc. **limits to 67 FPS** (with  $t_{10}^1$  task)
  - Idea: Use **HW video encoder** instead

## DVB-S2 TRANSMITTER



- **DVB-S2 MODCODs** based on:
  - **BCH + LDPC** ECCs concat. ( $N = 16740$ )
  - **Phase-Shift Keying (PSK)** modulation
- Implementation over a **3-stage pipeline**
  - Vectorized with the **MIPP SIMD wrapper** [4] to guarantee **portability & efficiency**

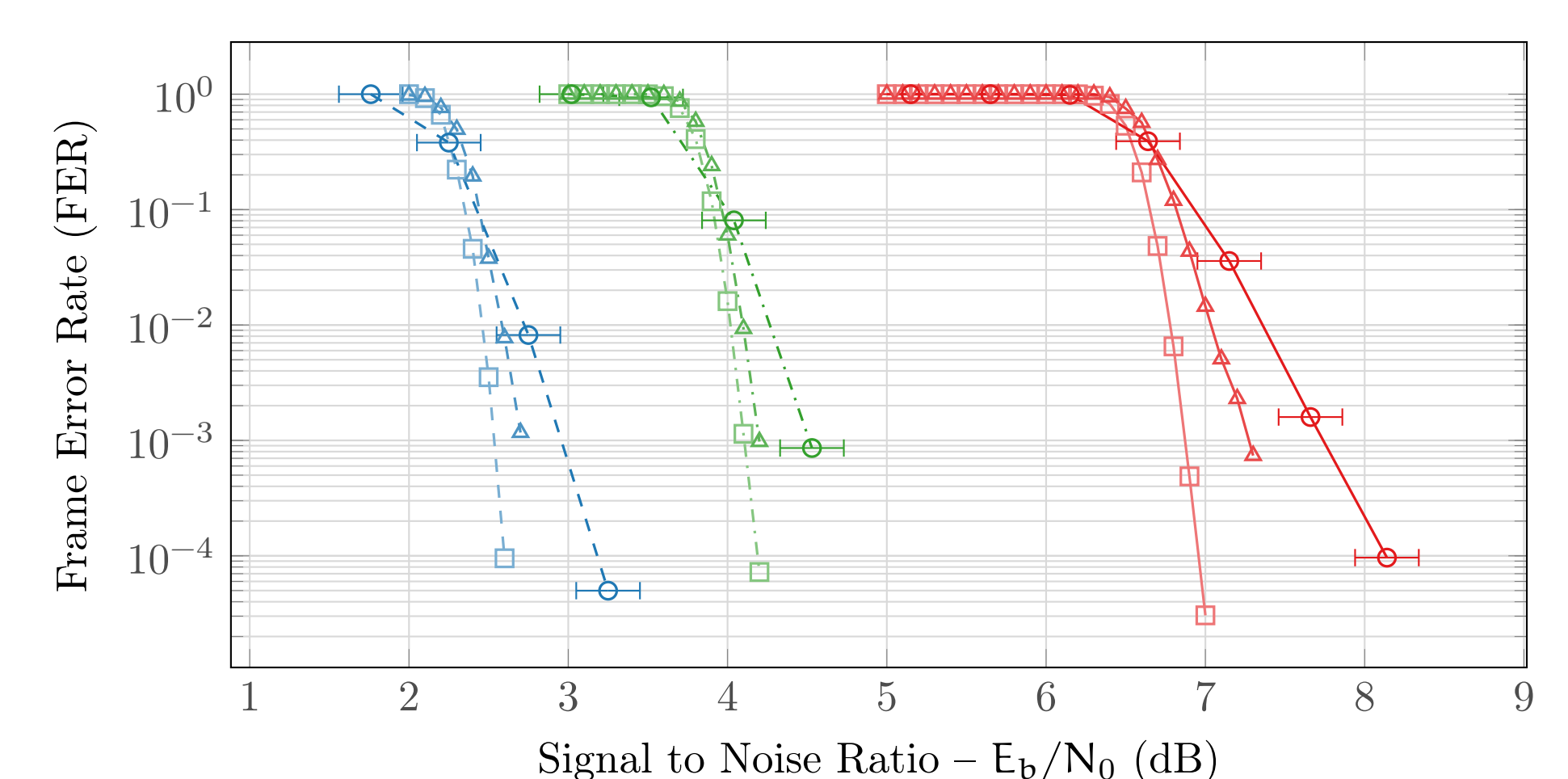
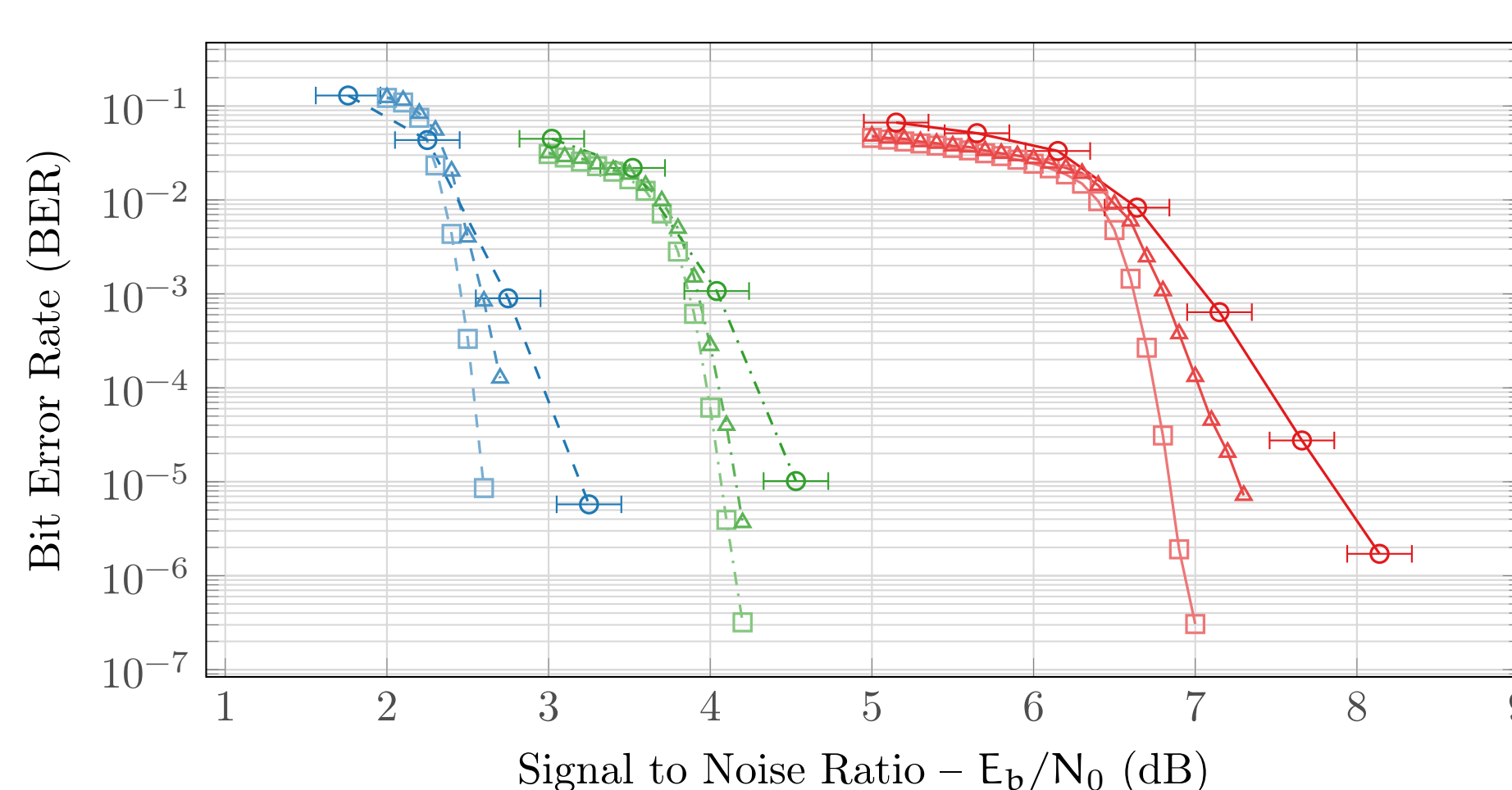
## DVB-S2 RECEIVER – TRANSMISSION PHASE



- $n$ -stage pipeline
- **Automatic scheduling with OTAC** [5]
- **Sync. timing** ( $t_4^{Rx}$ ) is the **limiting task**

## DVB-S2 RECEIVER – MEASURED PERFORMANCE

Configuration	Information Throughput (Mb/s)								Latency (ms)			
	Sequential				Parallelized with STREAMPU							
	Xeon	ThunderX2	M1 Ultra	Ryzen 7	Xeon	ThunderX2	M1 Ultra	Ryzen 7	Xeon	ThunderX2	M1 Ultra	Ryzen 7
MODCOD 1	3.4	1.0	5.9	8.5	37	19	33	37	–	37	6.3	8.8
MODCOD 2	4.1	1.4	7.0	11.6	55	28	51	55	56	41	8.0	9.6
MODCOD 3	4.0	1.1	5.6	12.0	80	42	71	71	–	51	10.1	9.3



Configuration	AWGN	AWGN+	Real
MODCOD 1, QPSK, R = 3/5	—□—	—△—	—○—
MODCOD 2, QPSK, R = 8/9	—□—	—△—	—○—
MODCOD 3, 8-PSK, R = 8/9	—□—	—△—	—○—

- **Portable implem.** on x86 & ARM CPUs
- **SDR flexibility:** Multiple MODCODs
- Up to **80 Mb/s** on Intel Xeon Platinum 8168

## REFERENCES

- [1] A. Cassagne et al. AFF3CT: A fast forward error correction toolbox! *Elsevier SoftwareX*, 10:100345, 2019.
- [2] A. Cassagne, R. Tajan, O. Aumage, D. Barthou, C. Leroux, and C. Jégo. A DSEL for high throughput and low latency software-defined radio on multicore CPUs. *Wiley CCPE*, 35(23):e7820, 2023.
- [3] L. Lacassagne and B. Zavidovique. Light Speed Labeling for RISC architectures. In *ICIP*. IEEE, 2009.
- [4] A. Cassagne, O. Aumage, D. Barthou, C. Leroux, and C. Jégo. MIPP: A portable C++ SIMD wrapper and its use for error correction coding in 5G standard. In *WPMVP*. ACM, 2018.
- [5] D. Orhan et al. OTAC: Optimal scheduling for pipelined and replicated task chains for software-defined radio. 2023.

<https://github.com/aff3ct/streampu>  
<https://github.com/aff3ct/aff3ct>  
<https://github.com/aff3ct/dvbs2>



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