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# High performance fully vertical GaN on Silicon PIN diodes for next generation power devices

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The existing Silicon- and Silicon carbide-based devices do not fulfill all the needs for next generation power generation due to physical limits and high cost of fabrication, respectively. On the other hand, Gallium nitride grown on silicon substrate offers superior physical properties and low fabrication cost. However, despite outstanding lateral GaN-on-Silicon HEMT (high electron mobility transistors) technology development within the last 20 years, the complexed heteroepitaxy, the rather large device dimensions, some remaining reliability issues partially due to the 2DEG proximity with the surface and the absence of avalanche capability still plague its market penetration for medium and high voltage applications. In this frame, vertical GaN-on-Silicon based configuration has been proposed [1]. Theoretically, this technology could show robust performances with avalanche capability and small fingerprint owing to a uniform vertical transport, which has recently been experimentally demonstrated at 800 V [2]. In many cases, pseudo vertical GaN-on-Si devices are used as a test vehicle, for which no backside processing is required. However, this device design suffers from a severe degradation of the on-state resistance ( $R_{on}$ ) increasing linearly with the anode size due to the so-called current crowding effect. Fully vertical devices can be achieved by accessing the  $n^+$  bottom layer from the backside by means of local substrate and buffer removal using DRIE and ICP, respectively. Some of the device fabrication challenges include 1) the mechanical robustness of the resulting membranes subsequent to the silicon and buffer etching, 2) both p-type and n-type high contact quality to ensure proper on-state performance, 3) the implementation of a heat sink close to the junction enabling high current spreading. At the epitaxy level, as the breakdown voltage scales with the drift layer thickness, both material quality and low bow should be maintained. In this work, we demonstrate high performance fully vertical GaN-on-Silicon PIN diodes with state-of-the-art blocking voltage above 1200 V and low  $R_{on}$  on large diodes resulting in high current spreading close to 12 A.

The growth of PIN diodes was performed by MOCVD on 6-inch Silicon substrate by using an optimized buffer as transition layers [3]. The structure contains a 500 nm thick  $N^+$ -bottom layer with a Si-doping of  $5 \times 10^{18} \text{ cm}^{-3}$ , a 7400 nm N-drift layer with a Si-doping of  $9 \times 10^{15} \text{ cm}^{-3}$  (net ionized doping) and a 700 nm of P-top layer with a Mg-doping of  $3 \times 10^{17} \text{ cm}^{-3}$  (active doping) (Fig. 1). The processing started with an optimized deep ICP mesa etching (supported by TCAD simulation), used as edge termination to reduce leakage current (Fig. 3). After mesa etching, a thick polyimide passivation is added to fill in the trenches and enhance the membrane robustness. Then, the Silicon and buffer layers are locally removed using DRIE and ICP tools. Prior to Ti/Au backside metallization, an HCl wet treatment is applied on the  $n^+$  N-face GaN layer to remove the native oxide, which is followed by a thick Copper electroplating of about 100  $\mu\text{m}$  (Fig. 2).

The fabricated diodes show a high breakdown voltage above 1200 V with indication of avalanche signature as seen from off-state temperature measurements (Fig. 4). On-state characteristics show a threshold voltage of about 4V and high current spreading with low  $R_{on}$  ( $< 0.5 \text{ m}\Omega\cdot\text{cm}^2$ ) on small diodes. On larger diodes using 1 mm anode radius, the  $R_{on}$  increased to  $1.7 \text{ m}\Omega\cdot\text{cm}^2$ , which is attributed to thermal management issues that can still be further optimized. Nevertheless, a high on-state current close to 12 A is achieved for the first time with fully vertical GaN-on-Si devices (Fig. 5 and 6). These results translate to a high Baliga figure of merit of  $3 \text{ GW}\cdot\text{cm}^{-2}$  and clearly show the potential of this technology for cost-effective high performance next-generation power devices.

## References

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- [2] Y. Hamdaoui et al, Appl. Physics Express 17, 016503 (2024)
- [3] S. Michler et al, Phys. Status Solidi B 2400019 (2024)

## Acknowledgments

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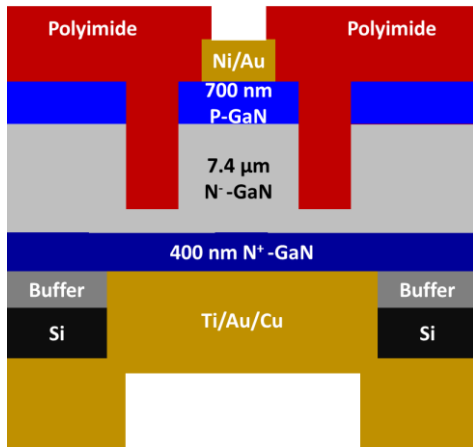


Fig. 1 Schematic cross section of the fabricated fully vertical PIN diodes

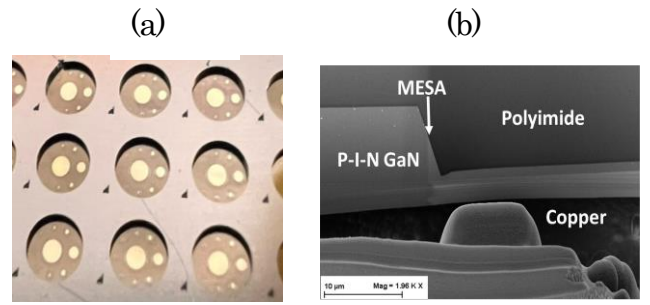


Fig. 2 (a) Backside image after local substrate and buffer removal (front side contact can be seen by transparency) (b) Focused ion beam image of a fully vertical PIN diode

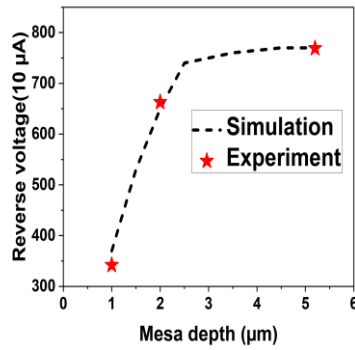
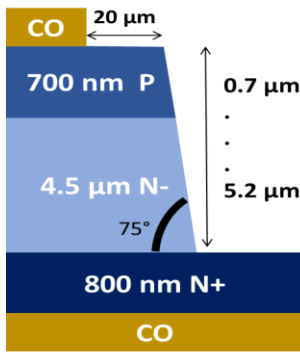


Fig. 3 Experimental and simulation reverse voltage at 10  $\mu$ A of 100  $\mu$ m anode radius PIN diodes showing the benefit of deep mesa etching

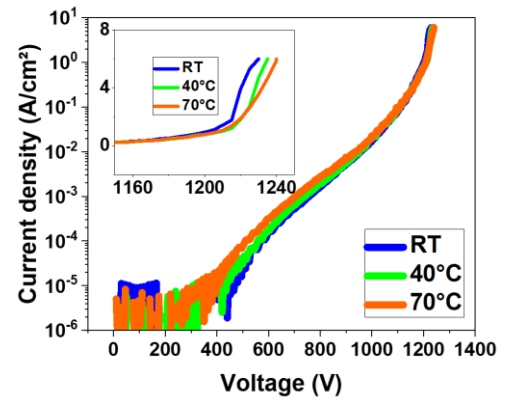


Fig. 4 Off-state measurement at various temperature of the fabricated diodes indicating avalanche signature

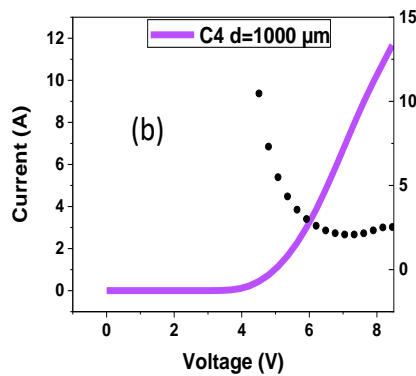
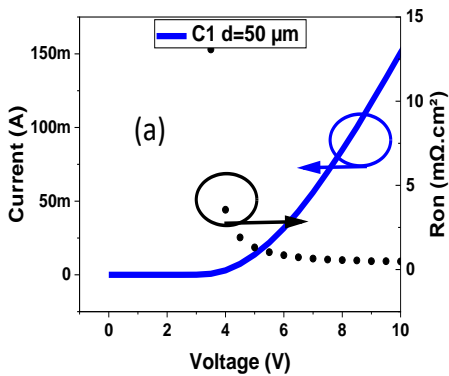


Fig. 5 On-state measurements of 50  $\mu$ m (a) and 1000  $\mu$ m (b) anode radius of the fully vertical GaN-on-Silicon PIN diodes

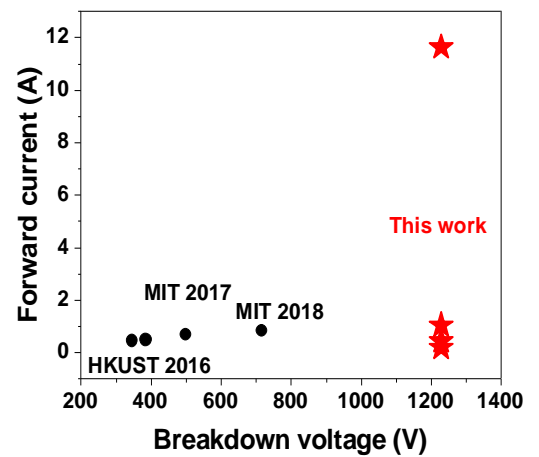


Fig. 6 Benchmark of vertical GaN-on-Silicon PIN diodes