Vertical GaN devices: Reliability challenges and lessons learned from Si and SiC

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Vertical GaN Devices: Reliability Challenges and Lessons Learned from Si and SiC

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***Abstract*—**We discuss recent advancements in the development of vertical GaN devices, and the related reliability challenges. Key results indicate that: (i) vertical GaN devices can show high performance, low background doping, and kV-range breakdown voltages; avalanche capability (a property of Si and SiC devices) is demonstrated also for vertical devices on silicon substrate, enabling reliable high-voltage operation; (ii) threshold voltage instabilities are related to the presence of interface and border traps, whose contribution can be modeled with great accuracy by prior characterization of the trap distribution profile; (iii) gate stack reliability is mainly limited by oxide breakdown; factors limiting off-state failure are discussed. Strategies for device improvement are proposed, also based on the learnings from silicon and silicon carbide technology.

I. Introduction

Wide-bandgap semiconductors are rapidly replacing silicon devices in the power conversion field. The large energy gap (3.23 eV for SiC and 3.4 eV for GaN) and the correspondingly large breakdown field make these materials ideal for developing efficient power semiconductor devices (material comparison shown in Table I). In the power semiconductors field, several device structures are currently adopted, as summarized in Fig. 1. Superjunction transistors help minimize conduction losses, for a given die size, thus constituting a reliable solution for devices on silicon; SiC transistors are based on different concepts, (either JFET, planar MOSFETs or trench MOSFETs), and can target voltages in the range of 2 kV or more. Commercially-available GaN transistors are based on the lateral HEMT (high electron mobility transistor) design, that ensures high mobility, thanks to the use of a 2-dimensional electron gas (2DEG) created via polarization doping, and low parasitics. Comparison between silicon, SiC and GaN-based commercial devices (Fig. 2) indicates that the GaN HEMT structures may have much lower gate charge, reverse recovery charge, and $R_{on} \cdot Q_G$ product, resulting in a significant minimization of resistive and switching losses in power converters. Recent innovation in the GaN field comes from the development of vertical device structures, to further increase power and current densities [1], [2] . This paper deals with the operation and reliability challenges for power GaN devices with vertical structure. We present recent and original data obtained within the YESvGaN project on: the properties of drift region grown on native and foreign substrates; the demonstration of avalanche capability in GaN-on-Si epitaxy; the physical origin of threshold voltage instabilities; the processes responsible for device breakdown and possible strategies for improvement.

II. Reliability Challenges

A. Optimizing the drift region for performance/reliability

The performance of vertical GaN devices strongly depends on the properties of the drift region. Reducing the unintentional impurity concentration can be beneficial in terms of mobility. Mobilities as low as $20\ cm^2/(Vs)$ have been extracted for high residual carbon ($[C]\sim10^{17}cm^{-3}$), whereas for higher quality material values around $960\ cm^2/(Vs)$ [3], [4] have been reported, comparable with those of silicon carbide [5], [6]. The residual conductivity of the drift region can also limit the maximum voltage that can be applied to the stack in order to prevent excessive leakage current. To investigate this issue, on a native GaN substrate, drift layers with a 10 µm thickness were grown (in pn junctions, Fig. 3) with doping levels around $8 \cdot 10^{15}cm^{-3}$; such structures could reach breakdown voltages above 1.2 kV (Fig. 4), i.e. compatible with the voltage range of SiC devices [7]. We note that growth on low-cost foreign substrates can induce larger dislocation densities $> 10^8\ cm^{-2}$, compared to vertical GaN-on-GaN ($< 10^4\ cm^{-2}$). This may result in higher leakage currents (see the data on sapphire substrate in Fig. 4): operation on foreign substrate is viable for voltages lower than 1200 V. Remarkably, we recently demonstrated near-kV avalanche capability in GaN-on-Si pseudo-vertical pn diodes (Fig. 5), a necessary property (present in Si and SiC devices) for reliable operation [7].

B. Substrate removal and vertical membrane concept

Looking at the main Si and SiC device structures in Fig. 1, it can be understood that also for GaN vertical devices, a vertical current flow is a necessary requirement, to minimize parasitics and current crowding effects. In case a native substrate is used, this can be obtained by directly depositing a metal on the bottom of the wafer. For foreign substrates, this can be achieved by removing the substrate locally, below the area of the transistor. Typical processes are etching (for Si substrates [9]) or laser lift-off (for sapphire substrate [10]). The resulting structure, along with device picture and I_D-V_D curves, is shown in Fig. 6; a Ti/Al backside contact, reinforced with a copper metallization, is used to ensure high conductivity. Best

$R_{on}A$ measured for a 0.52 mm^2 transistor is 5.2 $mOhmcm^2$ when extracted at V_D=1V, V_G=20V.

C. Charge trapping phenomena and instabilities

Silicon carbide devices may show significant threshold voltage shifts (between 0.5-1 V [12], [13], [14]) when submitted to positive gate stress. Typical processes involved are (Fig. 7) a) electron trapping at border/interface states [11], [12]; b) hole trapping due to impact ionization [15].

To investigate the physical origin of threshold instability in GaN vertical MOS structures, we carried out an extensive analysis on both quasi-vertical MOS capacitors (Fig. 8) and MOSFETs (Fig. 9), considering two different dielectrics (Al_2O_3 and SiO_2). Pulsed capacitance-voltage (C-V) analysis, carried out on MOS capacitors (Al_2O_3 dielectric), indicated the presence of positive (PBTI) and negative (NBTI) threshold instability (Fig. 10), and the presence of a characteristic "hump" in the C-V curves. Interface trap density was extrapolated experimentally by fast-CV measurements, indicating a deep-level peak centered around E_C-0.6 eV (Fig. 11). The resulting trap distribution was fed as input to TCAD simulations (Fig. 12), finding excellent agreement with the experimental data. The hump in the C-V curves was ascribed to the pinning of the Fermi-level at the energy corresponding to the peak of charge distribution. Further experiments were carried out to determine the best conditions for Al_2O_3 deposition. Results (Fig. 13) indicated that the lower CV hysteresis is obtained by thermal ALD (ThALD), compared to plasma-enhanced ALD (PEALD). However, since ThALD may suffer for limited robustness [13][13], a mixed (ThALD/PEALD) stack was found to be the most promising deposition process for Al_2O_3-vertical FETs.

With regard to charge trapping in MOSFETs (with SiO_2 dielectric), a first generation of devices was found to show a significant positive shift in threshold voltage, under positive gate stress (Fig. 14). A mathematical model can be proposed to interpret the kinetics, by considering tunneling of channel electrons towards trap states in the silicon oxide. By considering the tunneling probability (eq. (i) in Fig. 15), and calculating the integral of trapped-charge (eq. (ii) in Fig. 15), we were able to accurately reproduce the experimental data, consistently with the model in the inset of Fig. 15. TCAD simulations were also implemented, to investigate the role of border (BT) and interface (IT) traps. Trap distributions were calibrated, considering both donors in the upper half of the bandgap, and acceptors narrowly distributed near E_C. Results demonstrated that higher gate voltages result in higher electron tunneling probability from the channel to BTs, with consequent shift in threshold voltage (Fig. 16). New generations of devices (Fig. 17, Device B) showed a considerably reduced electron trapping. The significant improvement from Device A to Device B was obtained by changing the SiO_2 deposition process from low-pressure CVD (LPCVD) at 785 °C, with PDA at 800 °C, to LPCVD at 880 °C with PDA at 900 °C [18].

D. Failure processes

The reliability of GaN vertical devices was evaluated by a series of gate- and drain-step stress experiments. During a gate step-stress, on devices with a 70 nm SiO_2 gate dielectric, gate current was found to be negligible up to V_G=45 V (Fig. 18 (a)); for higher voltage levels, carrier injection through the oxide resulted in an increase in leakage current, till failure is reached at V_G=60 V. Similar experiments on SiC devices suggest a significant contribution of carrier injection from the semiconductor to the gate via Fowler-Nordheim tunneling [19], [20]; exposure to higher gate voltages may result in electron trapping in the oxide, with consequent positive shift in the threshold voltage (see Fig. 18 (b), and compare with [19], where similar failure voltages are found for SiC devices). The observed failure process is ascribed to the breakdown of the gate insulator; in vertical FETs, trench corners may represent favorable failure spots, due to the crowding of the electric field (Fig. 18 (c)). Also in a drain stress, carried out with grounded gate and high drain voltage, the electric field in the oxide can be close to the breakdown field of the dielectric. A simulation (V_G=0 V, V_D=100 V) is reported in Fig. 19 (a), indicating electric fields in excess of 6 MV/cm. Comparison with silicon carbide devices indicates that managing the electric field on the trench sides and bottom is a key step for ensuring high off-state reliability. Various solutions have been proposed, including bottom thick oxides [21], [22], [23], double trench structures, double p-base structures [24], and bottom protection p-wells [25], [26]. Such solutions are being preliminarily explored also for GaN vertical FETs (even if area-selective p-type doping of GaN is less mature than for SiC): an example is shown in Fig. 19 (b), where -similarly to what done for SiC in [27] – a p-shield has been placed on the trench bottom (marked as "p-well"), to significantly reduce the field across the dielectric in off-state conditions (compare with Fig. 19 (a)).

III. Conclusions

GaN vertical devices represent an excellent solution for next-generation power electronics. Native substrates ensure the lowest leakage current, for >1.2 kV operation, whereas foreign substrates as sapphire and silicon can be used for lower voltage operation, in presence of substrate removal. The concept of vertical membrane transistor has been proposed to obtain a low-cost GaN vertical technology. Epitaxy and process optimization allowed to reach near kV breakdown voltages, and to demonstrate avalanche capability on a silicon substrate.

The key charge trapping processes have been identified and modeled [28], [29]; solutions to minimize threshold voltage instabilities have been proposed, for both Al_2O_3 and SiO_2 dielectrics. The main failure processes of vertical GaN devices have been identified and described, for both gate and drain stress.

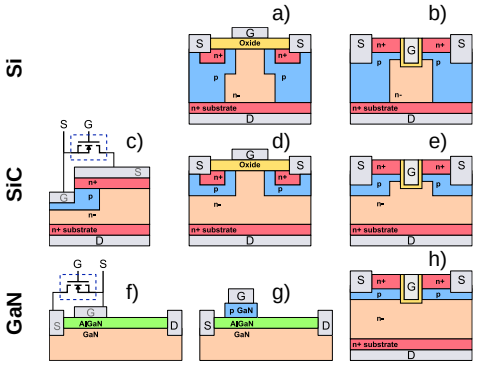


Fig. 1: schematic structure of power semiconductor devices; a) planar-gate SJ MOSFET; b) vertical SJ MOSFET; c) SiC vertical cascoded JFET; d) SiC planar-gate vertical MOSFET; e) SiC vertical trench MOSFET; f) GaN cascoded power HEMT; g) GaN power HEMT with p-GaN gate; h) GaN vertical trench-MOSFET

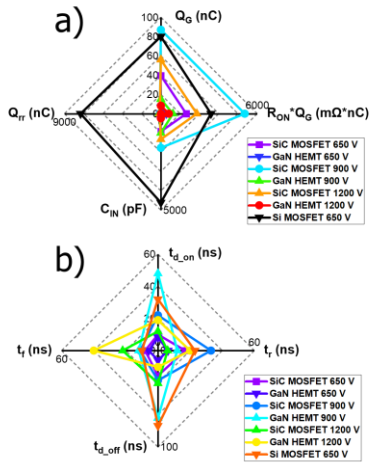


Fig 2: comparison of the dynamic properties of commercial GaN FETs, compared to SiC and Si

Material	E_G (eV)	E_{crit} (MV/cm)		μ_e (cm²/V s)	v_s (×10⁷ cm/s)
Si	1.12	0.3	1.3	1440	1
4H-SiC	3.23	2.5	3.7	950	2
GaN	3.4	3.3	2.5	1400	2.4
β-Ga_2O_3	4.9	8	0.1 - 0.3	250	1.1
Diamond	5.5	10	23	4500	2.3
AlN	6.2	15	2.85	450	1.4

Table 1: summary of the properties of wide bandgap semiconductors, compared with Si

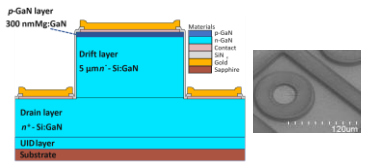


Fig. 3: (left) schematic structure of a vertical GaN PN diode; (right) SEM picture of one of the devices

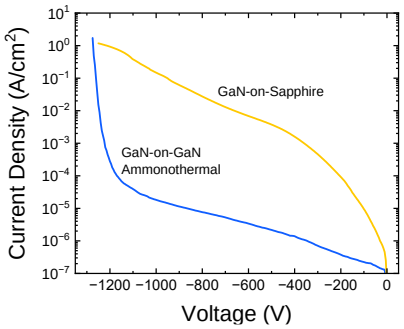


Fig. 4: I-V curves for vertical pn diodes grown on AT-GaN (dislocation density $10^4\ cm^{-2}$), and sapphire (dislocation density $5 \cdot 10^8\ cm^{-2}$)

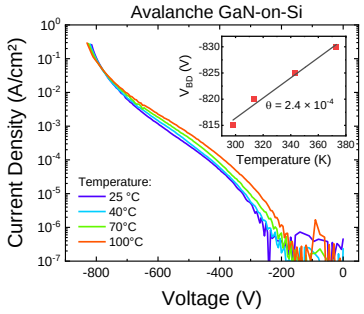
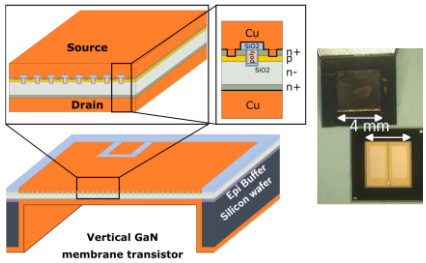


Fig. 5: avalanche characteristics of GaN-on-Si pseudo vertical diodes, and related positive temperature coefficient (net ionized doping concentration in the drift region is $9 \cdot 10^{15} cm^{-3}$)



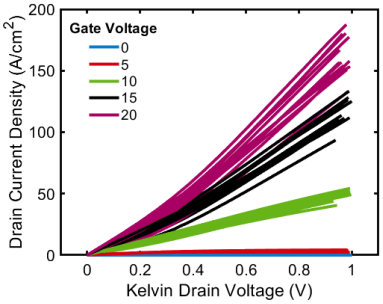


Fig. 6: (top left) schematic drawing of a vertical membrane transistor, as developed within the YESvGaN project; (top right) picture of one of the fabricated fully vertical chips; (bottom) I_D-V_D curves for one of the developed transistors

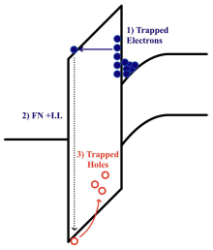


Fig. 7: schematic drawing the main processes responsible for threshold instability in SiC MOSFETs

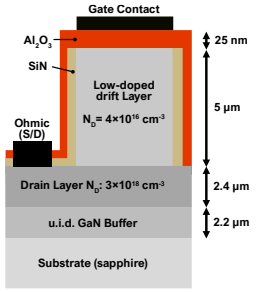


Fig. 8: structure of the investigated quasi-vertical MOS capacitors on foreign (sapphire) substrate.

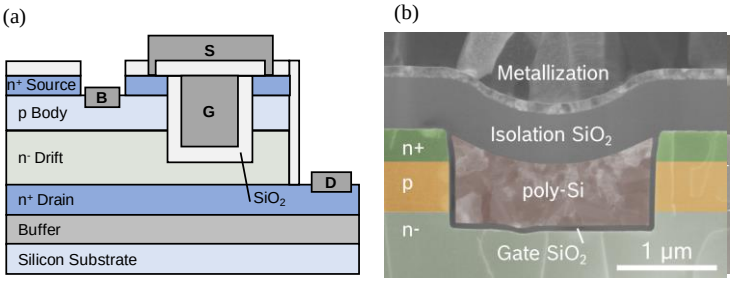


Fig. 9: (a) structure and (b) micrograph of the investigated quasi-vertical MOS transistors investigated within this work. The devices were grown on a silicon substrate

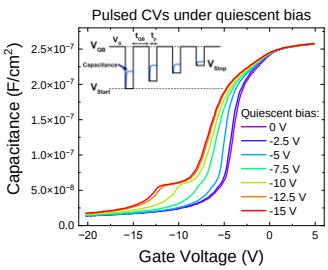


Fig. 10: impact of positive and negative gate stress on the pulsed capacitance-voltage curves of MOS capacitors; threshold voltage shift can be observed, along with a "hump" in the CV curves.

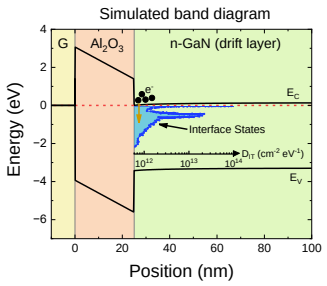


Fig. 11: interface trap density as estimated by fast-CV measurements in one of the MOSCAPs with structure in Fig. 8.

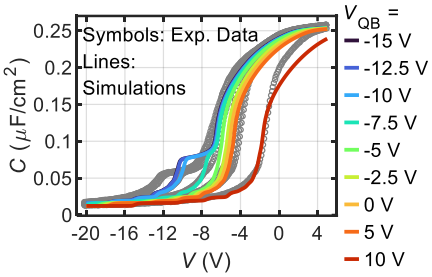


Fig. 12: simulated (colored) and experimental (gray) CV curves as obtained by TCAD simulations in GaN quasi-vertical MOSCAPs, by using the interface trap distribution extracted as in Fig. 11. Excellent agreement with the experimental data is found

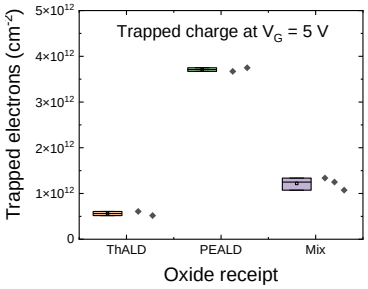


Fig. 13: comparative evaluation of the methods for depositing Al_2O_3 dielectric for the fabrication of MOS capacitors. Trapped charge is compared based on the CV hysteresis induced by positive gate stress

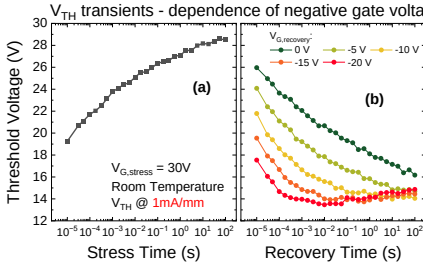


Fig. 14: threshold voltage variation under (a) positive gate stress and (b) consequent recovery phase at different voltages, for a first generation of quasi-vertical GaN MOSFETs

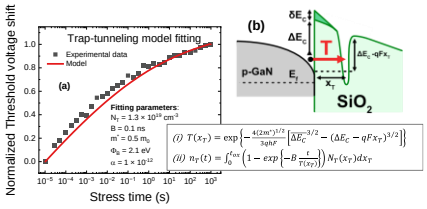
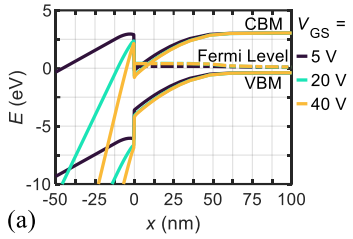


Fig. 15: experimental and modeled threshold voltage variation. Equation (i) represents the tunneling transmission coefficient, while (ii) models the total number of trapped electrons according with the tunneling model.



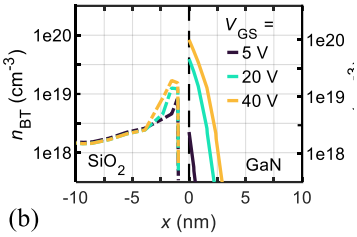


Fig. 16: simulated (a) band diagram and (b) trapped charge density, after stress at different bias levels. A significant increase in oxide field, along with increased tunneling and trapping probability, can be observed at high voltages

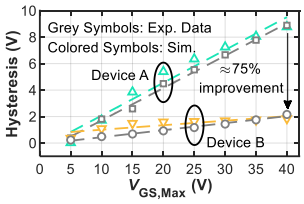


Fig. 17: simulated and measured hysteresis of I_D-V_G curves, after stress at increasing gate voltages, for two generations of quasi-vertical GaN MOSFETs (A and B)

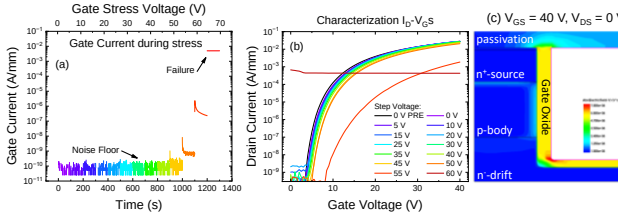


Fig. 18: (a) results of a gate step-stress, carried out on a quasi-vertical GaN MOSFET, by repeatedly increasing gate voltage until failure; (b) I_D-V_G characteristics measured after each phase of the step-stress test; (c) 2D simulation of the electric field in a vertical trench MOSFET biased at V_G=40 V.

(a) V_{GS} = 0 V, V_{DS} = 100 V (b) V_{GS} = 0 V, V_{DS} = 100 V

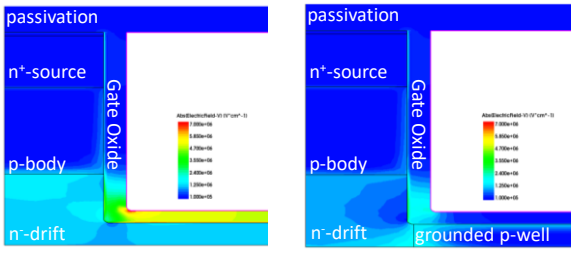


Fig. 19: simulated electric field in a quasi-vertical GaN MOSFET in off-state conditions (V_G=0 V, V_D=100 V). (a) standard structure; (b) structure with a bottom p-well (same doping as in the p-body layer)

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