



HAL
open science

High quality fully versus pseudo vertical GaN-on-Silicon pn diodes

Youssef Hamdaoui, Idriss Abid, Sondre Michler, Katir Ziouche, F Medjdoub

► **To cite this version:**

Youssef Hamdaoui, Idriss Abid, Sondre Michler, Katir Ziouche, F Medjdoub. High quality fully versus pseudo vertical GaN-on-Silicon pn diodes. GaN Marathon, Jun 2024, VERONA, Italy. hal-04762008

HAL Id: hal-04762008

<https://hal.science/hal-04762008v1>

Submitted on 31 Oct 2024

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

High quality fully versus pseudo vertical GaN-on-Silicon pn diodes

Youssef Hamdaoui, Idriss Abid, Sondre Michler, Katir Ziouche and Farid Medjdoub

Abstract— We report on high quality vertical GaN-on-silicon pn diodes. A successful scaling of the drift region thicknesses resulted in state-of-the-art breakdown voltage well above 1000 V (corresponding to a critical electric field of 2.3 MV/cm) together with low Ron ($< 0.5 \text{ m}\Omega\cdot\text{cm}^2$). Furthermore, a comparison between pseudo and fully vertical diodes fabricated on the same epi-wafer demonstrates the benefit of the fully vertical architecture when using larger device dimensions as needed to deliver high current. As a result, unprecedented low on-state resistance could be achieved in large mm-size diodes with avalanche breakdown capability.

I. INTRODUCTION

In the frame of the development of next generation low cost power devices, Gallium nitride (GaN) grown on Silicon (Si) is an undeniable technology that combines the high physical properties of GaN (large band gap, high electron mobility and high electric field) and the cost-effective Si fabrication technology. Lateral GaN-based high electron mobility transistors (HEMTs) on Si substrate are thus a promising candidate with proven high performances. However, several drawbacks slow down the industrialization of this technology for high voltage applications ($> 650 \text{ V}$) such as a destructive breakdown voltage (BV), a complex epitaxy and large device size [1]. To overcome this limitation, the junction based vertical GaN-on-Silicon technology could be an attractive alternative. Indeed, the vertical structure allows a better electric field management potentially resulting in low charge trapping issues. Moreover, the BV occurs due to impact ionization, which results in a non-destructive breakdown and thus unlock the avalanche capability. Finally, owing to the vertical transport, the device size can be smaller compared to high voltage lateral architectures.

Recently, pseudo vertical (PV) GaN-on-Si pn diodes have been developed with few attempts of fully vertical devices [2]. However, high current spreading in large devices has not been yet demonstrated, although this is a key requirement for power electronics. Current crowding effect in the case of pseudo-vertical devices is a major issue that prevents the achievement of large current (i.e. large device dimension with low on-resistance). Therefore, the development of a robust fully vertical (FV) structure with high processing and growth quality is critical to unveil the potential of this technology.

This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 101007229. The JU receives support from the European Union's Horizon 2020 research & innovation programme and Germany, France, Belgium, Austria, Sweden, Spain, Italy. This work was also supported by the French RENATECH Network.

In this work, we demonstrate a high-quality drift layer thickness scaling in fully vertical GaN-on-Si pn diodes enabling BV as high as 1135 V with low Ron and high current spreading through large anode size.

II. GROWTH AND FABRICATION

A first pn heterostructure has been grown on 6-inch silicon substrate using MOCVD. After the buffer layers, an 800 nm N^+ layer ($\text{Si}-5\times 10^{18} \text{ cm}^{-3}$) were deposited followed by 4.5 μm N^- drift region ($\text{Si}-3\times 10^{16} \text{ cm}^{-3}$, $n\approx 9\times 10^{15} \text{ cm}^{-3}$). The growth ends with 700 nm P layer ($\text{Mg}-5\times 10^{19} \text{ cm}^{-3}$, $p\approx 3\times 10^{17} \text{ cm}^{-3}$). Two additional wafers have been grown with different epitaxial parameters: a 500 nm N^+ layer, a 5.5 μm and 6.5 μm N^- drift region, a 600 nm P layer and 20 nm P^+ layer.

Processing consists in the deposition and patterning of Ti/Al/Ni/Au metal stack to contact the front-side n-type GaN layer after a mesa deep etching (down to the N^+ layer). It can be pointed out that an optimized Cl_2/Ar based ICP-recipe has been used not only to avoid sidewall damage but also to generate a beveled etching as edge termination. Then, a Ni/Au stack was deposited using evaporation on top of the P GaN layer. Both contacts were annealed at 500°C for 10 min. The P-type contacts showed ohmic behavior after annealing. The front side process was completed with 10 μm thick Polyimide layer to further prevent electrical peak induced-damage while increasing the mechanical robustness of the diodes.

The backside process comprises a Si substrate thinning from 1 mm to 400 μm , a local Si DRIE-etching followed by the buffer layer ICP-etching around the devices. Backside contacts are formed by evaporating Ti/Al on top of the N^+ GaN layer. Finally, a thick Cu-layer was electroplated on the backside both as a heat sink and to further increase the mechanical device robustness. As a result, pseudo and fully vertical (Fig. 1.a, b and c) are thus fabricated on the same wafer allowing a proper and direct comparison without any growth and processing variation.

III. DEVICE CHARACTERIZATION

The fully and pseudo vertical 4.5 μm GaN-on-Si diodes show similar high blocking capability with an average hard breakdown of 820 V (Fig. 2.a) corresponding to a critical breakdown field close to 2.3 MV/cm despite the absence of field plates. A uniform breakdown was also observed on large

Y. Hamdaoui, I. Abid K. Ziouche and F. Medjdoub are with IEMN (Institute of Electronics, Microelectronics and Nanotechnology), CNRS-IEMN, University of Lille, France. Email: youssef.hamdaoui@univ-lille.fr

S. Michler is with the Department Innovation Management, Siltronic AG, München, Germany.

diodes (anode diameter = 1 mm). The leakage current density is quite low compared to the previously reported GaN-on-Si pn diodes from the literature, which reflects the high material and processing quality such as the reduction of sidewall leakage and electrically active dislocations through the GaN drift layer. This is in line with the reported avalanche BV capability on a similar wafer [3]. Fig. 2.b shows the excellent scaling of the breakdown voltage as a function of the drift region thickness using diode diameter of 100 μm . To the best of our knowledge, this is the highest reported BV in vertical GaN on Si substrate with 1135 V, especially considering the avalanche BV capability.

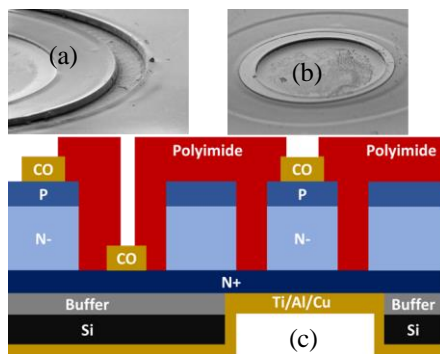


Fig. 1. SEM image of PV (a) and FV (b) GaN-on-Si pn diodes. (c) Schematic cross section of PV and FV GaN-on-Si pn diodes on the same sample

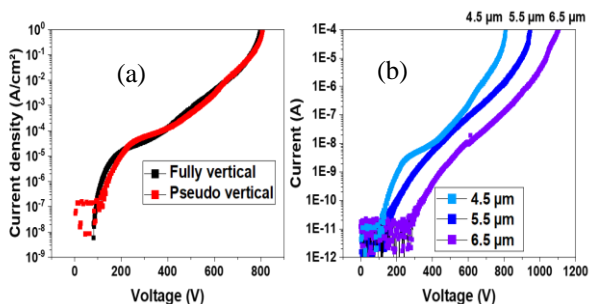


Fig. 2. (a) Reverse characteristics of fully and pseudo vertical 4.5 μm drift thickness and (b) 4.5 μm , 5.5 μm and 6.5 μm fully vertical pn diodes

The forward characteristics of the pseudo and fully vertical 4.5 μm pn diodes were evaluated using DC measurements. It is well known that current crowding effects occur in pseudo vertical configuration affecting the current spreading in large diodes as illustrated in our TCAD simulations (Fig. 4.a and b). This results in a degradation of the specific on-state resistance, which strongly increases with the diode size.

Fig. 3 shows the forward current and the corresponding differential R_{ON} of various diode sizes for both pseudo and fully vertical configurations. The devices exhibit a high current density with low differential $R_{ON} < 0.35 \text{ m}\Omega\cdot\text{cm}^2$ for the pseudo and fully vertical devices when using small device size. However, for larger diode size, R_{ON} degrades drastically in the case of pseudo vertical diodes (see Fig. 3.d) to reach for instance $10 \text{ m}\Omega\cdot\text{cm}^2$ for 200 μm diodes. Unlike pseudo vertical diodes, R_{ON} remains extremely low (around $0.25 \text{ m}\Omega\cdot\text{cm}^2$) as a function of the diode size (up to 200 μm of diameter). The low R_{ON} in the fully vertical configuration is attributed to the suppression of the current crowding effect that scales with the device dimensions. This, in turn, enables high current as seen

from the 1000 μm diode diameter delivering 7 A at 10 V with low $R_{ON} < 2 \text{ m}\Omega\cdot\text{cm}^2$ for FV compared to PV R_{ON} around $85 \text{ m}\Omega\cdot\text{cm}^2$ (Fig. 3.c and d). It can be noticed that the 1 mm fully vertical pn diodes are expected to generate even higher current level well above 10 A with a further optimized heat sink, showing the interest of this approach.

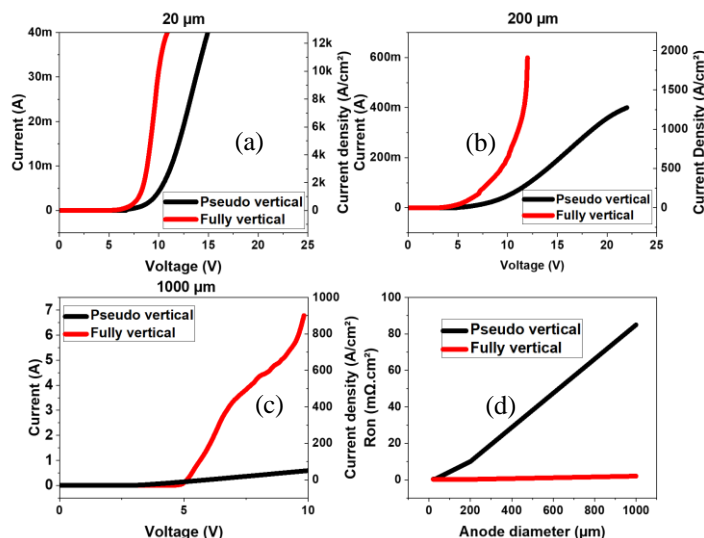


Fig. 3. (a) 20 μm , (b) 200 μm and (c) 1000 μm Forward characteristics of FV and PV 4.5 μm vertical pn diodes (c) R_{ON} dependence on anode size.

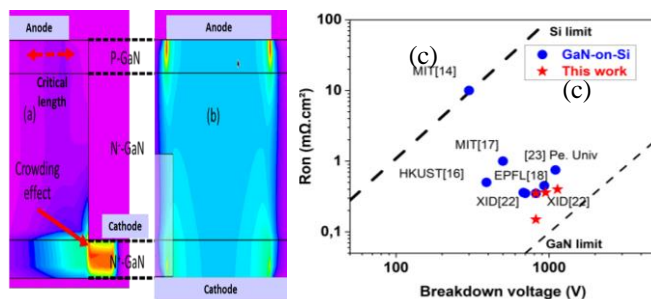


Fig. 4. TCAD current distribution at 10 V of PV (a) and FV (b) vertical pn diodes. (c) Benchmark of vertical GaN-on-silicon pn diodes

Conclusion

In this work, we investigated the potential of vertical GaN-on-Si technology. A highly scalable blocking voltage is demonstrated (820 V - 950 V - 1135 V). Furthermore, with 4.5 μm as drift thickness, fully vertical GaN-on-Si large pn diodes show high current spreading with low on-state resistance unlike pseudo-vertical diodes limited by current crowding effects. The demonstrated diodes are favorably comparable to the literature with a Baliga benchmark (Fig. 4.c) showing a BFOM $> 2 \text{ GW}/\text{cm}^2$.

REFERENCES

- [1] I. Abid, *et al.*, "Low Buffer Trapping Effects above 1200 V in Normally off GaN-on-Silicon Field Effect Transistors," *Micromachines*, 13, 1519, 2022.
- [2] Y. Zhang, *et al.*, "720-V/0.35-m $\Omega\cdot\text{cm}^2$ Fully Vertical GaN-on-Si Power Diodes by Selective Removal of Si Substrates and Buffer Layers," *IEEE Electron Device Letters*, vol. 39, No. 5, pp. 715–718, May 2018.
- [3] Y. Hamdaoui, *et al.*, "Demonstration of avalanche capability in 800 V vertical GaN-on-Silicon diodes" *Applied Phys. Express* 17, 016503, 2024.