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Localization and Physical Analysis of Defects in Degraded Power HEMT p-GaN Transistors Stressed with DC Voltage Surge and Voltage with Switching Stress

Lucien Ghizzo · Gérald Guibaud · Christophe De Nardi · François Jamin ·
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Abstract This paper presents a methodology for the physical analysis of defects on p-GaN power HEMTs that have been electrically stressed under DC surge or voltage switching stresses. The methodology includes a backside approach for sample preparation and defect localization. It is crucial to adapt the preparation process according to the position of the defect in the device structure (including metallurgy, dielectric layers, epitaxy, etc.), which depends on the type of stress applied. In our study of the reliability of the transistor under increased electrical stress in lifetime operation mode, failure analysis is used to identify the weakest areas in the design with respect to the type of stress applied. This paper presents a failure analysis consisting of techniques such as electrical characterization, photon emission microscopy and lock-in thermography for defect localization, focused ion beam slice and view, transmission electron microscopy analysis, and

frontside conductive atomic force microscopy after immersion in hydrofluoric acid.

Keywords Power transistors · HEMT GaN · Cycling · Failure analysis · Reliability

Abbreviations

GaN	Gallium nitride
HEMT	High electron mobility transistor
2DEG	Two-dimensional electron gas
PEM	Photon emission microscopy
LIT	Lock-in thermography
SEM	Scanning electron microscopy
FIB	Focused ion beam
TEM	Transmission electron microscopy
HF	Hydrofluoric acid
PQFN	Power quad flat no-lead
AFM	Atomic force microscopy
C-AFM	Conductive atomic force microscopy

List of Symbols

V_{DS}	Drain source voltage
BV	Drain breakdown voltage
DS	Drain source
GS	Gate source
I_{dss}	Drain leakage current under drain source voltage
t_0	Time before stress
$t_{0+35\text{ h}}$	Time after 35 hours of stress
FP	Field plate

Introduction

The GaN HEMT power device is emerging as a promising technology for high-frequency and medium-voltage power electronics applications. It overcomes the limitations of

silicon devices, enabling smaller and more efficient power converters. However, the reliability and failure modes of the device at maximum voltage and in switching operation near or just above its maximum ratings remain unknown. The specific physical degradation mechanisms and associated electrical signatures of GaN HEMTs require further understanding. Despite published reliability studies of power GaN HEMTs [1, 2], few resources on this technology are available to the FA community. The first part of this study describes the types of aging stresses applied. Our proposed backside sample preparation methodology must be adapted to the specific type of stress used. The second part of this paper proposes a methodology for identifying DC stress-induced defects. The third part will demonstrate the need to adapt this methodology for AC stress-induced defects. Several techniques, including IR lock-in thermography (LIT), photon emission microscopy (PEM), and Raman spectroscopy, are used for backside defect localization. Physical analysis of the defect will be performed using focused ion beam (FIB) slice and view sectioning, TEM analysis, and frontside conductive AFM measurements after hydrofluoric acid exposure treatment. The chemical etching of dislocations will be also presented. Most of these measurements methods are briefly described in [3]. The method shows how to adapt the failure analysis to the failure mechanisms that are new and proper to the GaN technology.

Electrical Stress and Characterization

Three stressed devices (#1–3) and two unstressed devices (with the same part number) were compared. All devices are commercially available and are 100 V, 90 A, 7 mΩ PQFN packaged p-GaN gate AlGaIn/GaN HEMTs (with a Si substrate). The drain voltage V_{DS} of device #1 was linearly increased in DC mode until the breakdown voltage (BV) was reached. A 1 kΩ resistor was added in series to reduce the leakage current after breakdown. The $I(V)$ curve obtained using a Keysight B1505A curve tracer during the breakdown experiment is shown in Fig. 1. Transistors #2 and #3 were subjected to voltage stress with no current in a no-load half-bridge circuit at 120 V and 2 kHz for 35 hours in AC mode. The study focuses primarily on electrical stress, and a very low switching frequency was chosen to avoid thermal overstress.

Figure 2 shows characterization curves of #2 stressed in AC mode illustrating the relationship between leakage current I_{dss} and V_{DS} , shown in blue at t_0 and in orange after stress at $t_{0+35\text{ h}}$. A sudden increase in leakage current is seen at $t_{0+35\text{ h}}$, but only above 90 V in Fig. 1a. Despite this current leakage, the transistor remains operational after aging. This current leakage is purely intermediate, as the

gate leakage current is not affected during this measurement, as can be seen in Fig. 2b. Failure analysis was performed to identify the location and nature of the defect, in both static and dynamic voltage stress.

DC Stress Defect Type: FA Methodology

The transistor technology features three metal levels for interconnecting drain, source, and gate, along with a polysilicon gate level. The epitaxy is composed of AlGaIn/GaN layers on a silicon (Si) substrate. In this configuration, backside optical defect localization is more effective [4–6].

First, the leadframe and PQFN package samples were removed by backside parallel lapping (see Fig. 3). The silicon substrate was then thinned to a thickness of 100 μm for transistor #1. We confirmed that the active region and electrical characteristics of the transistor remained consistent, allowing the performance of IR lock-in thermography to be correlated with the PEM analysis. Transistor polarization is enabled by the PQFN configuration with through-hole metal vias (Fig. 3), and probe needles are used on the underside of the thinner Si substrate. The images in Fig. 4 show upside-down views of the chip's GaN layers through the remaining silicon substrate. We observed a precise correlation between the position of the LIT hotspot and the PEM emission spot. Similar to the backside FIB editing approach, we perform backside final trenching of the remaining silicon layer over the hotspot/emission spot position using XeF₂ gas-assisted etching on a DCG Systems optiFIB IV. To achieve precise positioning of the FIB slice and view cross-sectional area, we also perform FIB marking around the spot localization.

The cross section for the FIB slice and view is 2 μm away from the hot spot (see Fig. 5a) and a small pitch of 50 nm is required to determine the defect size. A filamentary breakdown defect can be seen in only one image of the slice and view (see enlarged Fig. 5b). This defect is located in the Si_xO_y and AlGaIn layers where the electric field is highest between the 2D electron gas (2DEG) connected to the drain electrode and the corner of the drain-side field plate (FP) connected to the source, as expected. This defect appears to be a metal filament formed by the localized fusion of the FP metal with Si_xO_y and AlGaIn to connect to the 2DEG. The dimensions of this defect are extremely small (a few tens of nanometers), and the resolution of the FIB slice and view sections is insufficient. Therefore, accurate analysis of this defect type requires TEM observation.

For transistors #2 and #3, the suspected defect is in the epitaxial layers, which presents a challenge for observation. The analysis approach for this problem is discussed in the following section.

Fig. 1 (a) Electrical characterization of the breakdown voltage of transistor #1, a steep increase of the current I_D between drain and source occurs at 155 V. (b) Electrical characterization of the leakage current after the breakdown voltage experiment

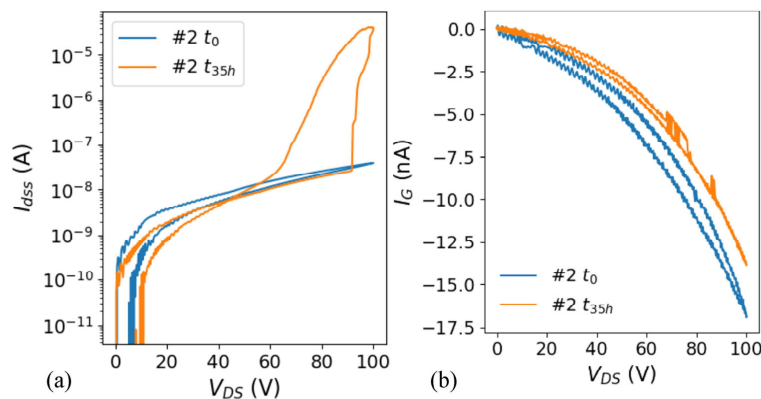
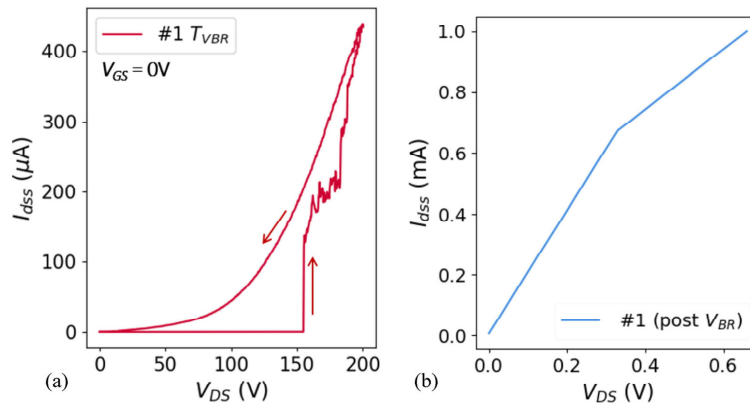


Fig. 2 Electrical characterization of the aged transistor #2 of the leakage current I_{dss} under V_{DS} at t_0 in blue and after 35 hours of electrical stress at t_{0+35h} in orange. A high leakage current appears

only after 90 V. Forward and backward sweeps are performed to account for possible hysteresis (arrows near the curves). #3 has a similar I_{dss} curve to #2

AC Switching Voltage Degradation Type FA Methodology: The Challenge of Defect Localization

The transistor #2 shows more hotspots during LIT backside analysis (Fig. 6a) after backside parallel lapping (silicon substrate thinned to 100 μm). These hotspots appear when the transistor is stressed and the electric field is above 90 V. They match the high leakage shown in Fig. 2a. PEM analysis still correlates with the observed spots, despite minor variations. The same trenching method used on transistor #1 did not find any more spots at that position with either LIT or PEM.

Hotspots and emission spots on transistor #2 are mostly near the drain edge electrode, as shown in Fig. 7b. Some spots are visible near the gate region. The spots in

transistor #3 look like those in #2. We will present the results of other measurements on transistor #3 at the end of this paper.

Removing the silicon provides an opportunity to apply another analysis method such as Raman spectroscopy, because GaN/AlGaN materials are transparent at a wavelength of 532 nm, unlike silicon. GaN/AlGaN materials are transparent at a wavelength of 532 nm, unlike silicon. Raman spectroscopy is used to analyze epitaxy layers and transistor unit cells for characteristics like structure, temperature, strains, and electric field using a frontside approach. It has not yet been used to analyze commercial device failures, let alone from the back. Figure 8 shows how the main peak of the Raman shift changed in the silicon trenching area (see Fig. 8a and b). A spot is visible

Fig. 3 (a) RX view of the PQFN package of the device (b) scheme of the parallel lapping modification from the backside before the localization of defects, the electrical polarization is still possible on both the backside and the frontside thanks to the traversing vias

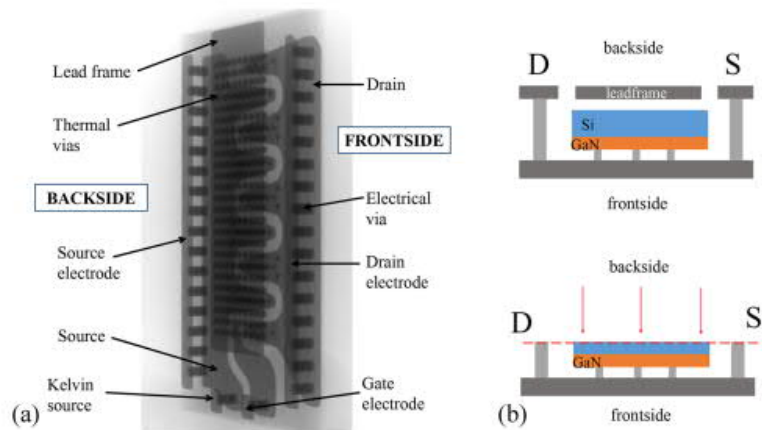


Fig. 4 (a) LIT amplitude signal of the prepared transistor #1 at $5 \times$ magnification (lock-in frequency 25 Hz), polarized at 2 V with probes landed on the electrical vias. (b) LIT at $10 \times$ magnification focused on the hot spot (c) InGaAs camera PEM image at $71 \times$ magnification focused on the emission spot (good correlation with LIT hot spot position)

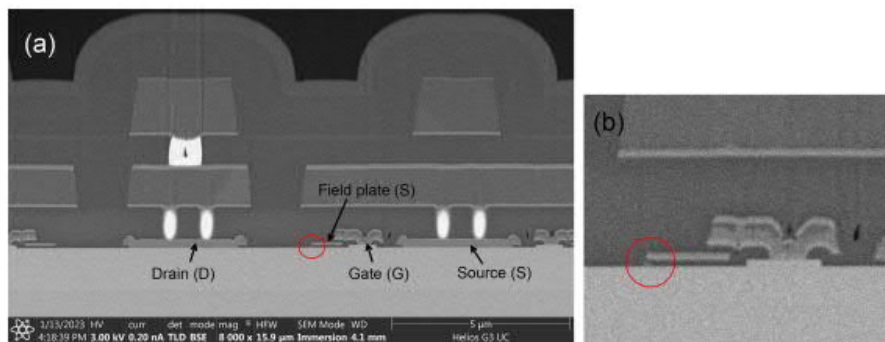
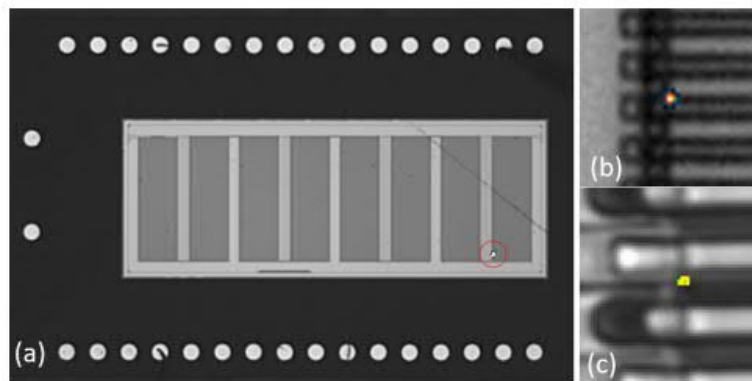


Fig. 5 (a) FIB slice and view cross section in the defect zone of transistor #1. The zoom in (b) shows at the corner of the source field plate the leakage path formed at the breakdown voltage in Fig. 1a. This is the zone where the electric field is locally most significant

above the metal lines (Drain, Source, Field Plate), where the defect was found by LIT and PEM.

Figure 8c shows a $100\times$ view of the GaN layer. It reveals dark spots that were not seen before after FIB trenching. Raman spectroscopy helped find the defect after trenching the silicon substrate. But it seems that this and the laser power made the defect worse. The hotspot that

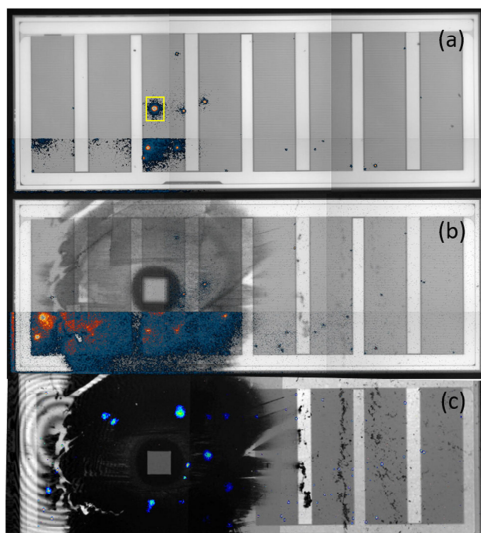
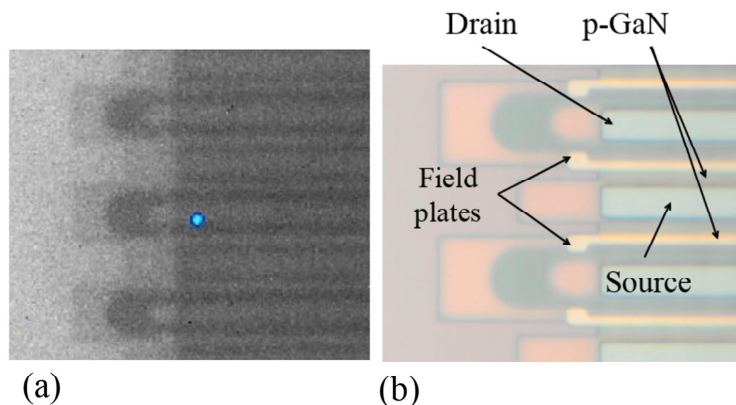


Fig. 6 (a) Superimposed LIT of #2 with polarization between 75 and 95 V, more than 20 hot spots are visible, a brighter hot spot is visible in the yellow square (b) LIT after FIB silicon trenching locally over the brightest hot spot location which has disappeared (c) InGaAs camera PEM image after FIB silicon trenching, the emission spot has also disappeared (Color figure online)

Fig. 7 (a) InGaAs camera PEM image of the emission spots. The defects are near the drain metal, which is expected to be a DS leakage through the GaN layer (transistor #2). (b) Optical zoom of the metal structure seen from the backside



disappeared after Si trenching is now visible again with LIT and PEM after Raman spectroscopy (Fig. 9a and b).

Other trials were done on the remaining spots to find the best FIB trenching depth and marking parameters. A $10\ \mu\text{m}$ silicon layer in the trench keeps the defect in focus with LIT and PEM.

A FIB marking is done in the silicon to position the TEM lamella extraction preparation as seen on the optiFIB IV ionic image and in-situ IR camera image.

TEM lamellae preparation and observation

We have all the information we need for further analysis. TEM lamellae are used to study the damage caused by AC switching stress. Three lamellae were prepared: two from transistor #2 and one from an undamaged device. The two from #2 show a DS current leakage defect (Figs 2 and 7). The lamella from the unstressed device is used as a reference. It was taken from the same region as the drain source junction of transistor #2.

In order to see all layers during the TEM wafer inspection, the silicon layer was partially removed during the FIB trench (see Fig. 10). A significant thickness was retained because the defect was believed to be under the active region in the GaN/epitaxial layers.

Figure 11 shows the TEM lamella of device #2 on a drain defect. The defect area is coated with platinum for protection. FIB boxes are carved on both sides of the mark. The unthinned lamella is then removed with a micromanipulator and positioned on a TEM grid. The final FIB thinning is performed to obtain a sample thickness of 100 nm.

Figure 12 shows that the TEM images of the same zone for an unstressed reference part (Fig. 12a) and a stressed part (Fig. 12b) clearly show that the dislocation density has

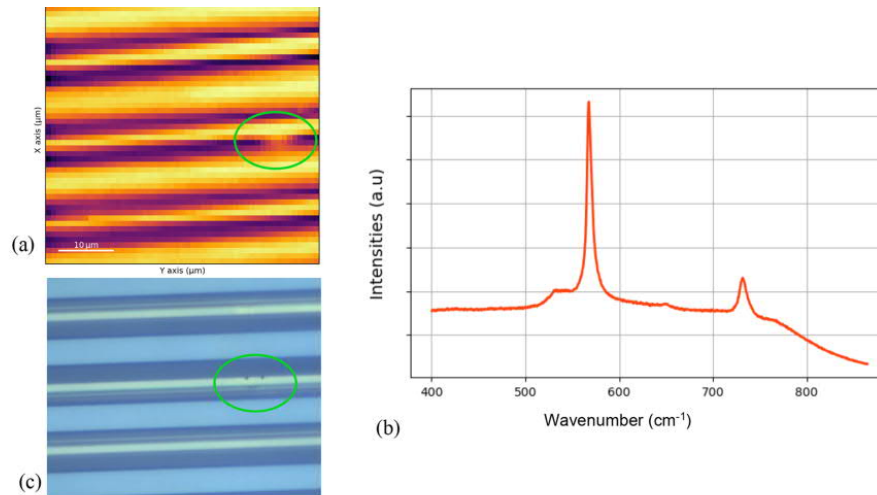


Fig. 8 Raman spectroscopy using a 532 nm laser beam with a diameter of 300 nm. (a) Mapping of the main Raman peak (1 μm scan step). (b) Long exposure Raman spectrum associated with (a, b)

acquired for one pixel. (c) Optical view of the defect at 100 \times at the coordinates given in (a)

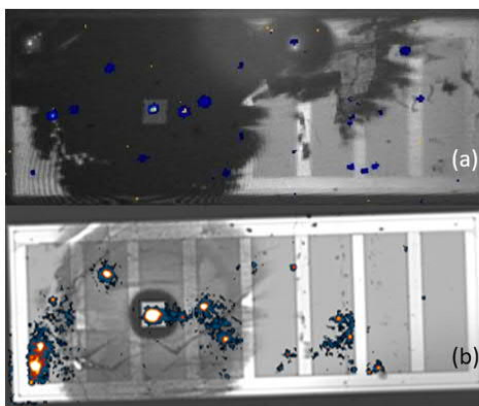


Fig. 9 (a) PEM after Raman analysis, the brightest emission spot that disappeared after trenching now has signal. (b) LIT amplitude after Raman analysis, as with PEM, the hot spot reappeared after Raman analysis

increased for the stressed transistors, especially in the gate drain region and below the drain metal where the electric field is most significant and where the spots are visible in the localization of defects. The drain region is more stressed than the gate region, for example, because the 2DEG is more depleted in the off-state for a higher V_{DS} voltage. We believe that the vertical leakage current path may be caused by changes in the quality of the GaN layer

in the buffer near the drain due to the electric field stress. Dislocations may grow or appear due to the piezoelectric effect, which creates a mechanical constraint between the layers (relative to the electric field).

In Fig. 12b, the leakage current could pass through a 2DEG at one of the AlGaIn/GaN interfaces or reach a conductive GaN layer. We think that when the silicon is removed by FIB trenching, it could change the electrostatic polarization around the leakage path. This could cause the spot in localization of defects to disappear with the same polarization parameters (in Figs. 6b and c), while the defect is still in the device.

We think that in a degraded device after stress, when the V_{DS} reaches a certain level, some of these dislocations may start to conduct or reduce the electrical insulation in the zone of higher dislocation density. The electrical resistivity of the GaN layer is reduced, and the leakage current reaches the source vertically through the epitaxy. The leakage current in the conducting dislocations could lead to recombination with trapped charges in the buffer and explain the light emission we observed with PEM at high V_{DS} .

We don't yet fully understand how dislocations cause leakage. This paper suggests some possible types of dislocations and conduction mechanisms. These dislocations are thought to be dislocations through the GaN for DS leakage. However, it is difficult to determine the type of conducting dislocation because the growth method is

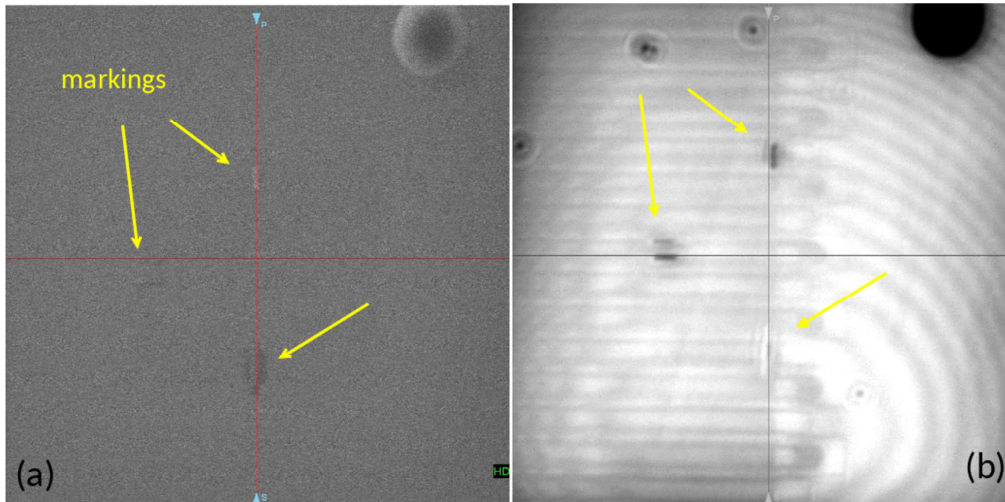


Fig. 10 (a) SEM image of the trench with 10 μm of remaining silicon and marking. (b) In-situ IR camera image through the remaining silicon and view of the etched lines marking the hot spot position for TEM lamella extraction

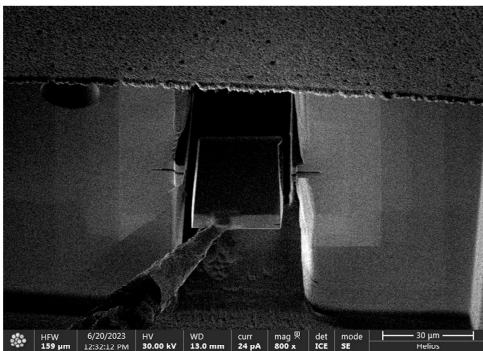


Fig. 11 TEM lamella extraction in the area bounded by the optiFIB markers after milling and side cutting

unknown. There are several possibilities. The dislocation formed/grown may be different from those at t_0 , which may be less conductive. The difference in leakage current between the unstressed and stressed device may be due to the dislocation density. Stress may make high-density dislocations areas more conductive due to the migration aluminum in the GaN layer.

The leakage current flow and/or the formation of dislocation can move aluminum from AlGaIn near the leakage path. This aluminum reduces the electrical isolation of the GaN layer, causing drain source leakage when the V_{DS} is sufficient (about 90 V in this study). Dopants in the GaN

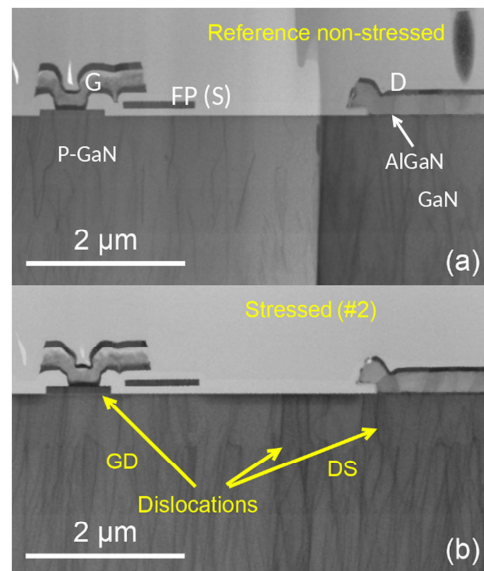


Fig. 12 (a) TEM lamella observation of our reference device that was not stressed (b) TEM of the drain region of device two #2 (stressed in AC at 120 V). The density of dislocation seems to be more significant for stressed devices compared to the pristine one

layer and impurities can also affect conduction. The electric field must be strong to activate the leakage path, even if the dislocation is similar. We don't know if the leak path

CONSISTS OF ONE OR MORE DISLOCATIONS. WE NEED TO KNOW which dislocation is causing the leakage.

More TEM investigations should be made like the one presented here to prove this hypothesis since the dislocation density is already significant for a pristine device and not homogeneously distributed over the wafer. Unfortunately, the TEM method is expensive and very time-consuming which makes us doing other experiments to have more evidence about this degradation mechanism. The conductivity of dislocations and their types was determined using electrical mode AFM/conductive atomic force microscopy (C-AFM) [7, 8] in a frontside approach.

Electrical Characterization of the Dislocations

Two samples were used to study how dislocations conduct electricity. One sample was a reference device, while the other was transistor #3, which was subjected to the same stress as transistor #2. The electrical characterization curves of the latter transistor are similar to those of transistor #2. This device was also thinned on the backside to find defects (PEM, LIT). Several spots were found like #2 in Fig. 9. We will compare how the dislocations behave in the two devices using C-AFM. We will compare the two devices in the same region and in a spot region of the stressed device.

Both devices are etched with nitric acid [4] and then hydrofluoric acid to remove layers from the front of the chip. This technique is used to prepare silicon microelectronic devices so that the active region on the front of the chip can be accessed. This study shows that HF acid does not affect AlN/AlGaIn/GaN layers. Conductivity measurements will be performed in a degraded zone where leakage is expected and an emission spot has been detected. We will use the p-GaN cap steps as markers.

Electric mode AFM will polarize some dislocations on the two devices to see if they conduct. The current will pass through the AlGaIn barrier and reach the source electrode through the 2DEG. The AFM will measure the conduction near the p-GaN cap. The area of interest is between the gate and drain. It is the expected current leakage zone and the most degraded region for the applied stress (see red square in Figs. 13 and 14). Dislocations were observed in both the AlGaIn and GaN layers.

A square area of $10\ \mu\text{m}$ is scanned to analyze the conduction behavior under electric polarization up to 10 V (limited by the conductive mode of the *Bruker Dimension Icon XR AFM* used in this study). A comparison with the reference device is performed using the same measurement protocol. Only the recorded negative currents are taken into account due to the equivalent Schottky diode contact created by the metal conducting AFM probe on the

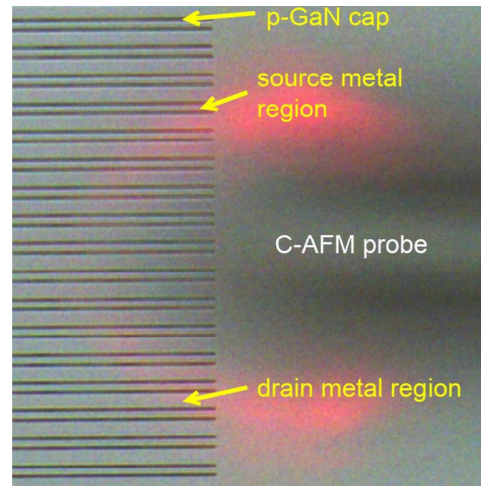


Fig. 13 Optical observation of the frontside surface after HF acid, the double line patterns observed are p-GaN caps, the rest of the observed surface is AlGaIn, except in the previous source and drain metals the two p-GaN caps and location (see Figs. 7c and 17), where the surface is the GaN layer

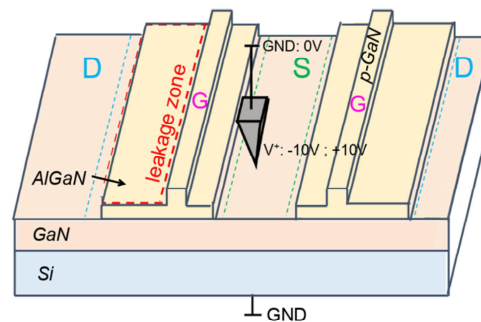


Fig. 14 Setup of a conductive AFM experiment. The probe is electrically polarized between -10 and $+10$ V. The blue squares are the previous drain metal regions and the green squares are the previous source metal regions (Color figure online)

investigated semiconductor. The differences in the leakage current paths can be observed in Fig. 15a and b.

The conductive AFM experiment is clearly not suitable for this study and for this type of device, considering the low current measured (pA) and the low polarization that can be applied compared to the threshold voltage of the leakage degradation of Fig. 2a (close to 90 V). The results obtained in [8, 9] are for experimental epitaxial structures and not for a commercial device such as ours.

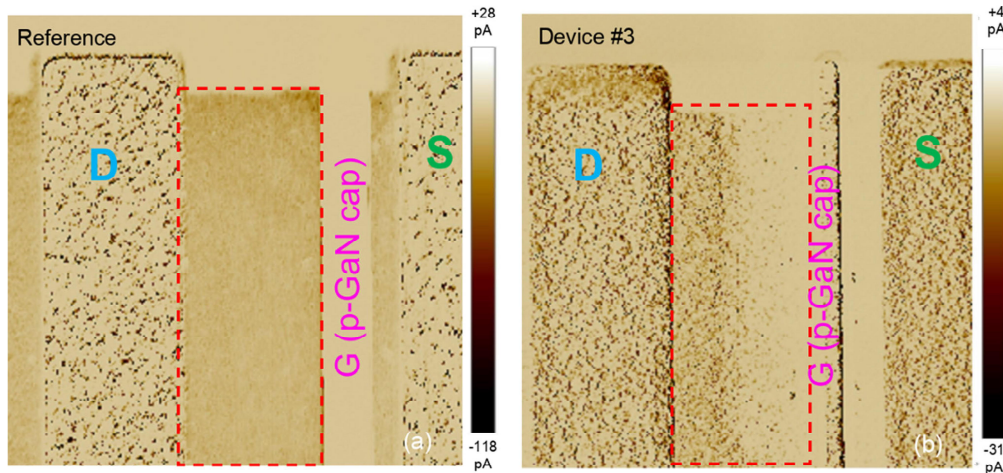


Fig. 15 Current leakage mapping obtained with conductive AFM, the black dots are the current leakage paths. The areas where the metal contacts were previously are always more conductive due to their proximity to the 2DEG, which facilitates surface leakage currents

However, although the comparison is difficult, a comprehensive analysis of the current leakage mappings reveals some differences that can be attributed to stress. First, it was observed that the leakage current in the region of interest and in the region between the p-GaN and the source metal (GS region) differs for the same device. For unstressed devices, the leakage current in both regions is remarkably similar. However, for device #3, the region bounded by the red lines in Fig. 15b appears to be more conductive than the GS region (which is not particularly stressed because the 2DEG is always in this region, reducing local hot electron effects and electric field value). In addition, the leakage current for the stressed device (#3) is less uniformly distributed over the region of interest compared to the reference device. In fact, the leakage is higher at several precise locations that form black dots in the C-AFM scan shown in Fig. 15b. Some of these dots may represent the leakage current flowing through the threading dislocations observed in the TEM lamellae.

Only degradation is observed and the transistor is still functional despite operating in a degraded mode. The functional state of the devices makes FA analysis even more difficult. Our hypothesis is that a complete failure such as a transistor breakdown could be expected to be caused by the same conductive dislocations that could induce percolation paths through the GaN layer (DS leakage current) in a real application. Further experiments will be performed on some of the stressed devices (already degraded parts like #2 and #3) in a future experiment to validate this late hypothesis on the failure mode that could follow the degradation mode presented in this paper. More

samples are needed to perform statistical studies and to draw a conclusion about this mechanism. The analysis of this degradation gives the ignition of the failure mode, which is very important to understand the full degradation/failure mode of the device. This observed degradation would have been very difficult to understand as the cause of a major failure in a barely damaged device.

A chemical etching with pure phosphoric acid could reveal the nature and number of dislocations formed during the stress compared to the reference device as in [10] and is presented in the following section.

Chemical Revelation, Observation of the Conductive Dislocations

The previous reference device and device #3 were chemically exposed with H_3PO_4 at 130 °C for 30 minutes. Some etch pits of revealed dislocations are visible on both devices (stressed and unstressed) which are less than 1 μm in diameter (Fig. 16b). On the stressed device, some zones are different from the unstressed device and lines of larger etch pits can be observed as shown in Fig. 16a and c. This pattern is expected to be related to the vertical leakage through the GaN buffer and the increased density of dislocations. The larger pits could be caused by the favored etching of the GaN in these areas due to the locally higher aluminum concentration brought about by the formation of dislocations, which reduces the electrical insulation and generates the vertical current leakage path for V_{DS} greater than 90 V [11–13].

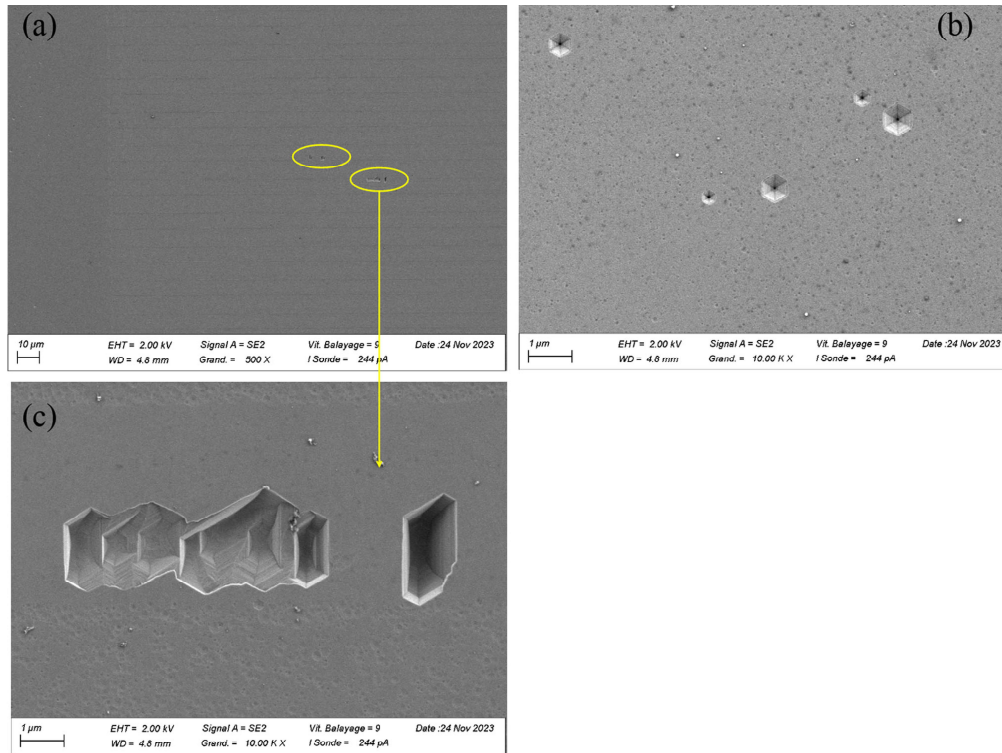


Fig. 16 Etch pits obtained by chemical exposure with H_3PO_4 from tool #3. (a) Different etch pits pattern observed on the surface. Both the reference and the #3 have the small hexagonal etch pit visible in (b), but only the #3 has the line of (c)

Conclusions

In this paper, a backside approach failure analysis methodology is proposed and applied for commercial PQFN p-GaN HEMT DC and AC switching stress-induced defect types.

The analysis performed shows that these physically induced defects can be very difficult to isolate (filament-like breakdown in DC stress). Backside ultimate FIB trenching of the silicon substrate over LIT hot spots/PEM emission spots can be a very effective way to perform the finest physical defect analysis (slice and view/TEM cross view), but it must be specifically adapted depending on the type of electrical stress inducing different defect position depths in the transistor layers. This paper also shows that the complete removal of silicon by FIB trenching could also allow the use of Raman spectroscopy as a defect localization tool. The defect is very small (a few tens of

nm) and can be missed easily in the FIB slice and view, even with much information obtained with several complementary techniques such as electrical characterization, in particular capacitance and leakage current measurements and localization such as PEM, LIT, and even Raman spectroscopy. In terms of design, this mechanism could be avoided, for example by adding a second field place to enhance the BV by reducing the peak electric field and improving its distribution [14].

For the AC stress case, the TEM observation allowed to determine the nature of the leakage current for these degraded devices, which seems to be an increase of the dislocation density. However, the high number of threading dislocations in this technology makes the interpretation of the origin of the leakage current very difficult. The TEM is still limited for this type of analysis and very time-consuming; therefore, thanks to the deep HF on GaN devices, the frontside C-AFM measurements can be another

complementary option to characterize the conduction behavior of dislocations and complete the interpretation of the TEM observations. The results obtained in this work are consistent with our hypothesis of degradation due to the applied real-life-like stress. The leakage current observed in the characterization measurements is suspected to pass through dislocations in AlGaIn and GaN. However, even if C-AFM measurements give good results of the leakage currents mapping on the surface, the measurements is limited by the maximal electric polarization of 10 V. These conductive dislocations could result from the mechanical constraints due to the piezoelectric effect generated by the electric field. The chemical etching with H₃PO₄ acid shows that the etching is favored in the defect zone attributed to a higher concentration of aluminum that have migrated to the GaN layer with the dislocation formation and/or the flowing of the leakage current and which make the layer more conductive very locally. This method gives valuable additional information but require to have several failed devices as the etching rate varies a lot from one device to another.

The application of the stress for a longer duration until the complete failure of the device will explain the complete aging process of the device from the beginning of the degradation to a non-functioning device. The likelihood of dislocations formation might be reduced by changing the buffer layer design [15] or by changing the growth method to reduce the strain between Si and GaN [16].

In conclusion, the results obtained with this methodology will provide significant information about the reliability and failure modes of power GaN HEMTs under application-like conditions.

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