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Electrical Rule Checking of Integrated Circuits using Satisfiability Modulo Theory

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Matthieu Moy*, Gabriel Radanne*, Pascal Raymond[§]

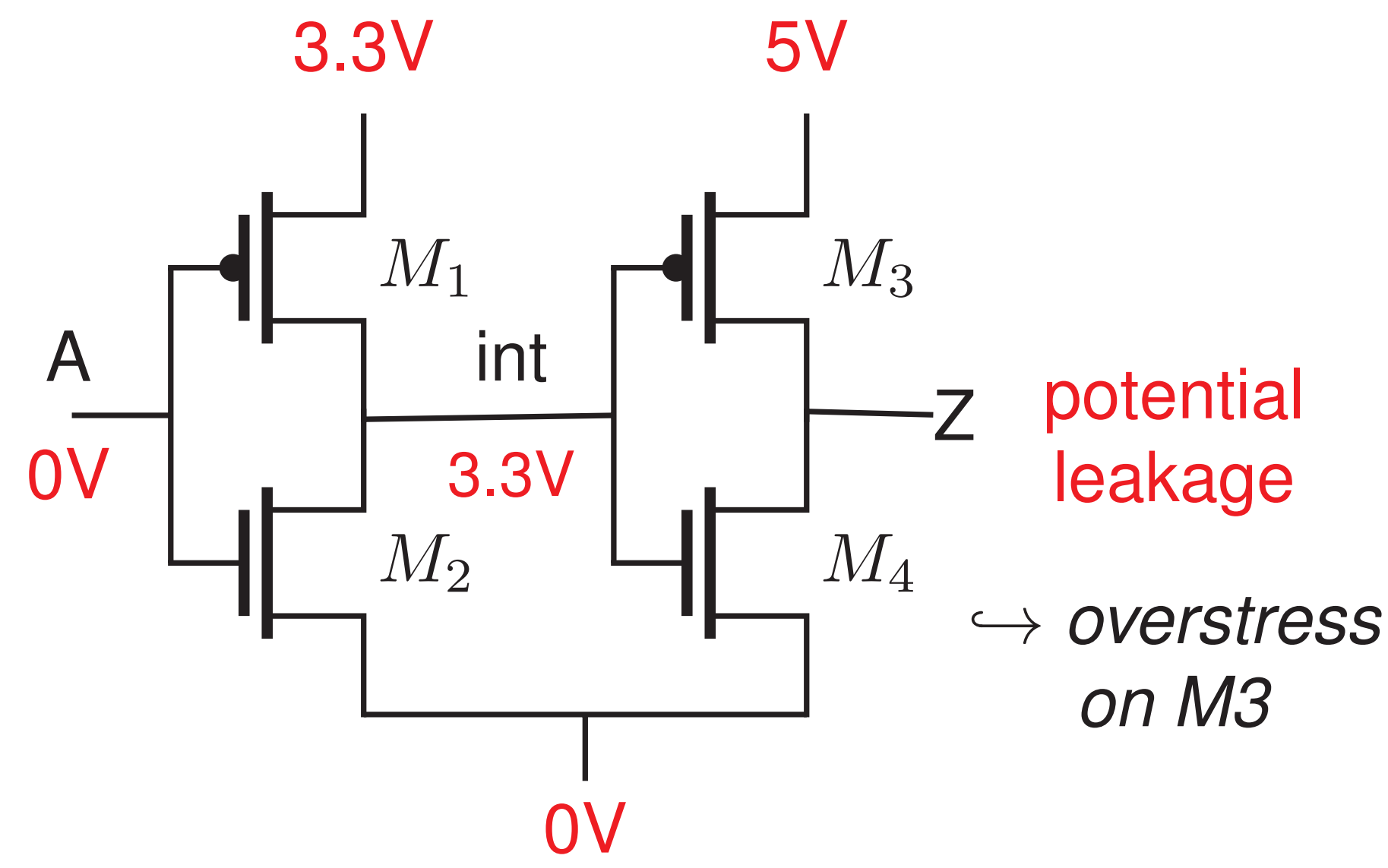
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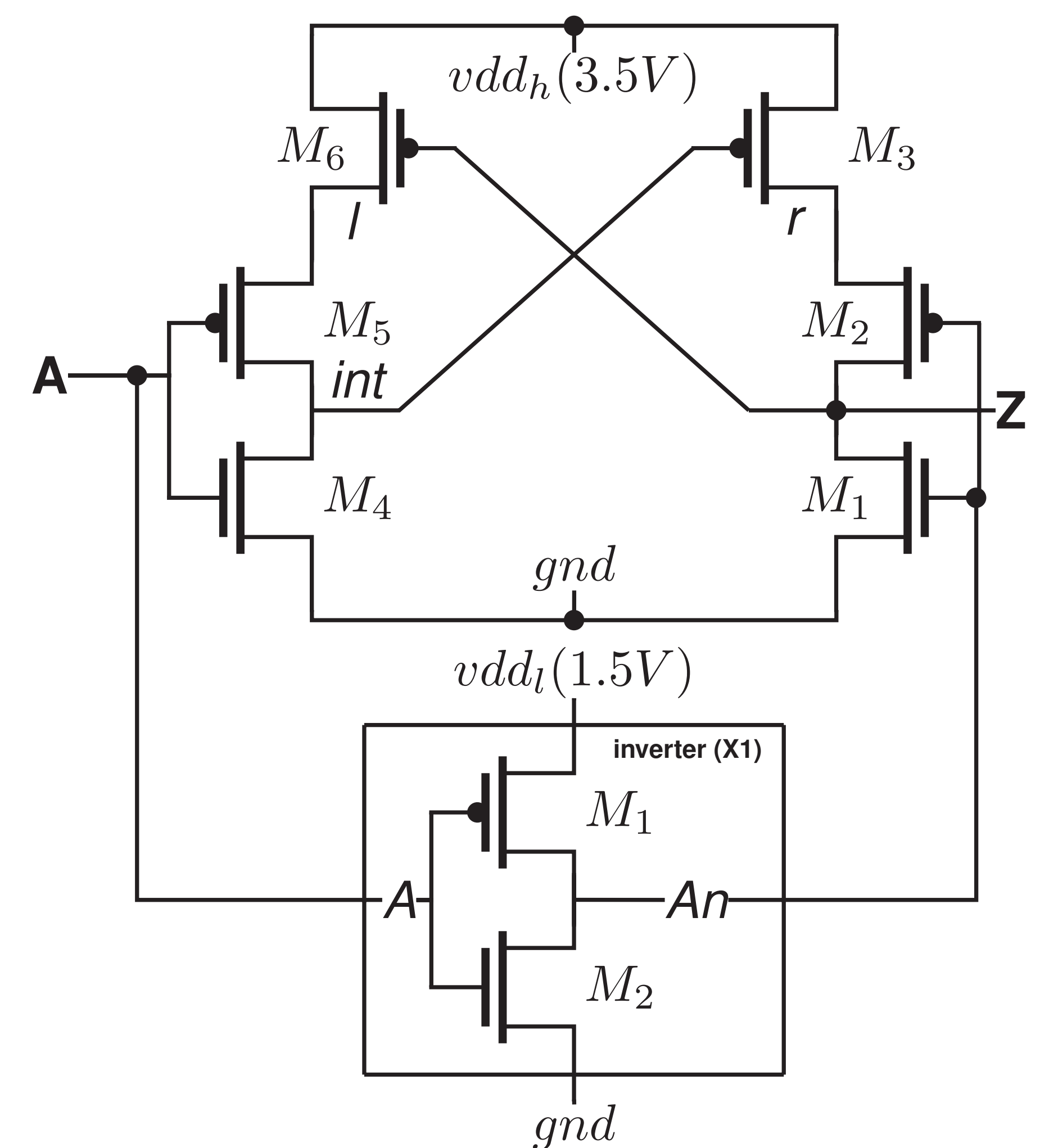
Objectives

- Formal verification techniques to improve analysis accuracy for circuit electric verification (ERC)
- Transistor-level semantics of circuits
 - encode circuits into formulas
 - check SATisfiability of errors
 - previous version introduced in [1]

Electrical Errors



Encoding a Level Shifter



Encoding the Behavior

$$\begin{aligned} \mathcal{O}_n(M_5) &\Leftrightarrow (V(A) < V(l) \vee V(A) < V(int)) \\ \wedge \mathcal{O}_n(M_4) &\Leftrightarrow (V(A) > V(gnd) \vee V(A) > V(int)) \\ (\mathcal{O}_n(M_5) \wedge \neg \mathcal{O}_n(M_4)) &\Rightarrow V(int) = V(l) \\ \wedge \neg \mathcal{O}_n(M_5) \wedge \mathcal{O}_n(M_4) &\Rightarrow V(int) = V(gnd) \\ \vee \mathcal{O}_n(M_5) \wedge \mathcal{O}_n(M_4) \wedge V(gnd) &< V(int) < V(l) \end{aligned}$$

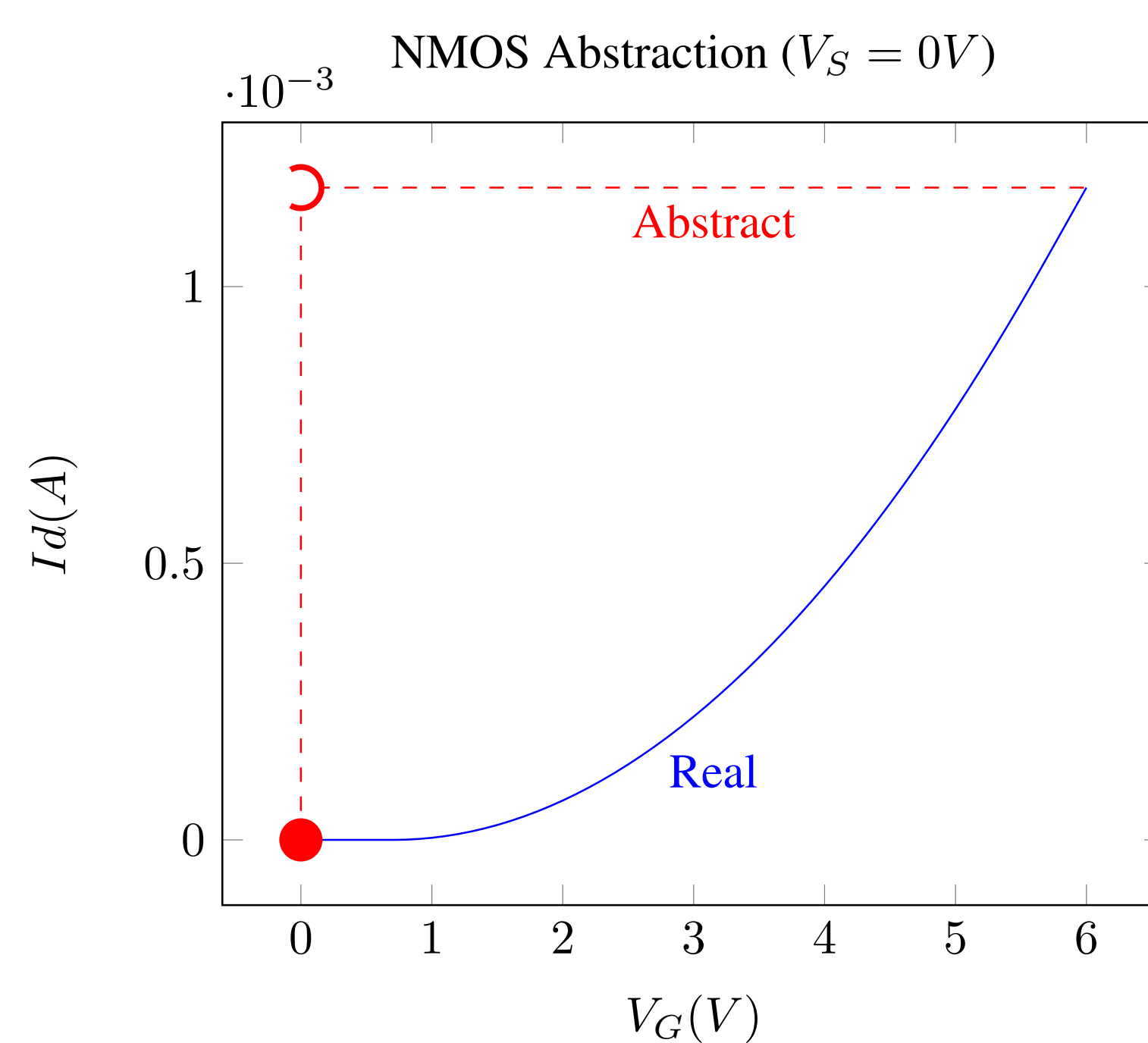
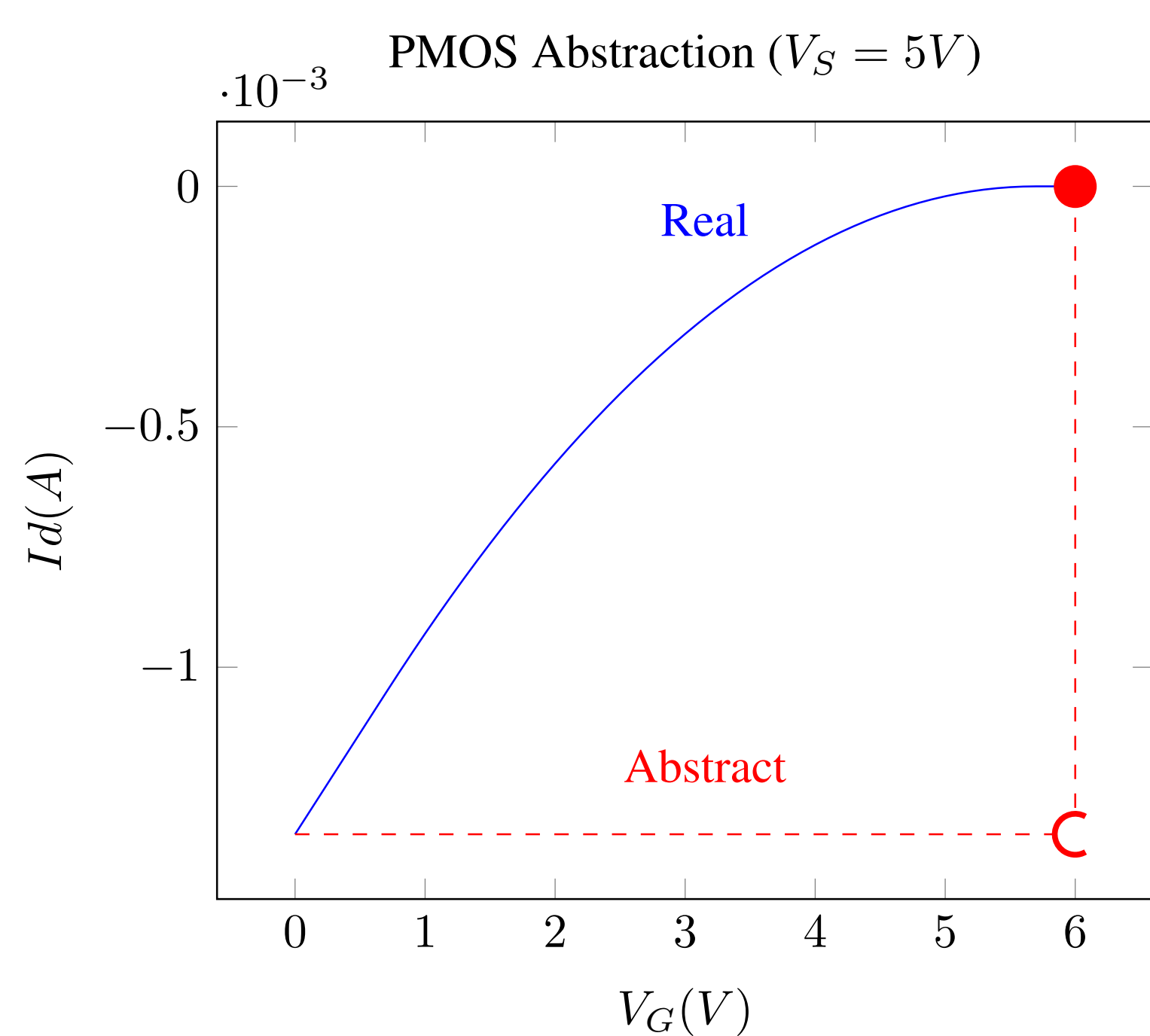
Enumerating the Solutions

V(A)	V(int)	V(Z)
0.0	3.5	0.0
[1.5, 3.5]	0.0	3.5

↪ no leakage possible

Voltage Aware Local Semantics

Abstraction of Transistors Behavior

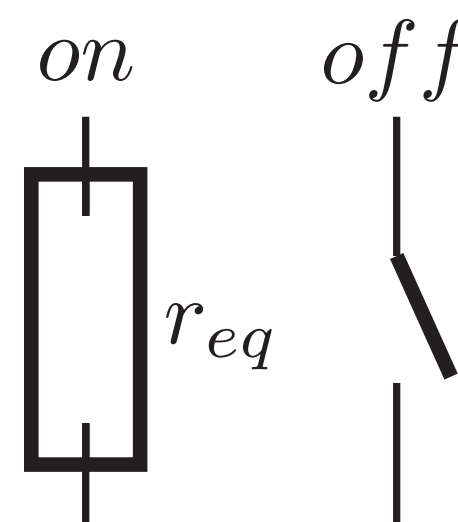


PMOS and NMOS characteristic curves $I_d = f(V_{GS})$ and abstractions.

Transistor Behavior as Logical Clauses

$$\forall Mx \in \mathcal{D}_{NMOS}, \mathcal{O}_n(Mx) \triangleq V(Mx_{GATE}) > V(Mx_{SOURCE}) \vee V(Mx_{GATE}) > V(Mx_{DRAIN})$$

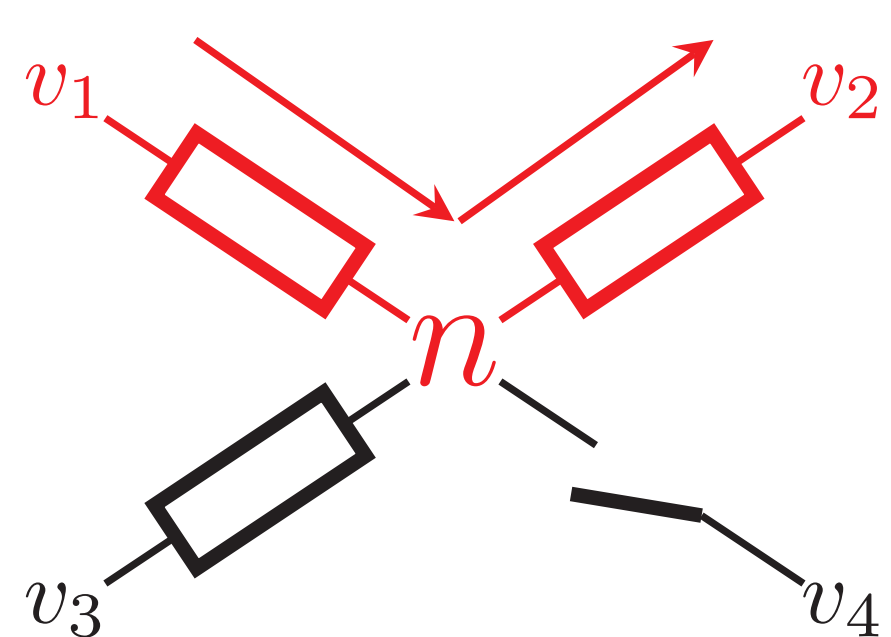
$$\forall Mx \in \mathcal{D}_{PMOS}, \mathcal{O}_n(Mx) \triangleq V(Mx_{GATE}) < V(Mx_{SOURCE}) \vee V(Mx_{GATE}) < V(Mx_{DRAIN})$$



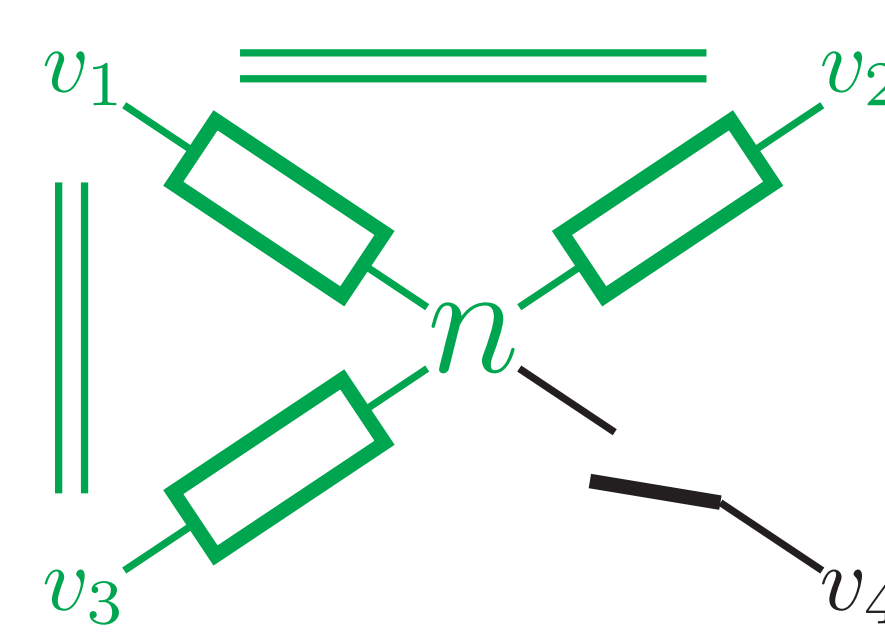
Voltage Assignment through Disjoint Clauses

$$CurrentFlows(n) \triangleq \exists i, j \in neighbours(n), \mathcal{O}_n(Mx_i) \wedge \mathcal{O}_n(Mx_j) \wedge [V(i) < V(n) < V(j)]$$

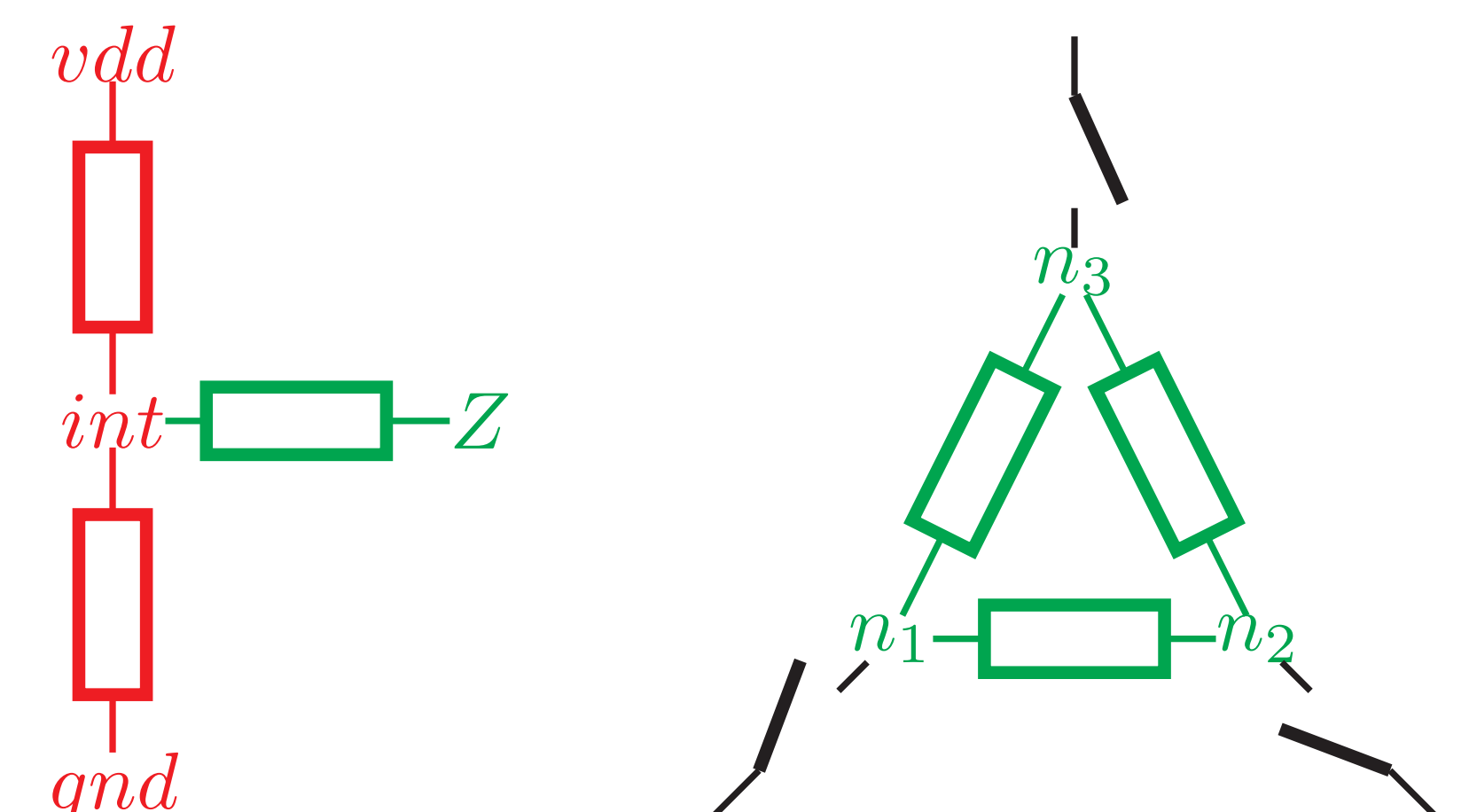
$$NoCurrentFlows(n) \triangleq \forall p \in neighbours(n), \mathcal{O}_n(Mx_p) \Rightarrow V(n) = V(p)$$



$$\forall n, CurrentFlows(n) \vee NoCurrentFlows(n)$$



Corner cases

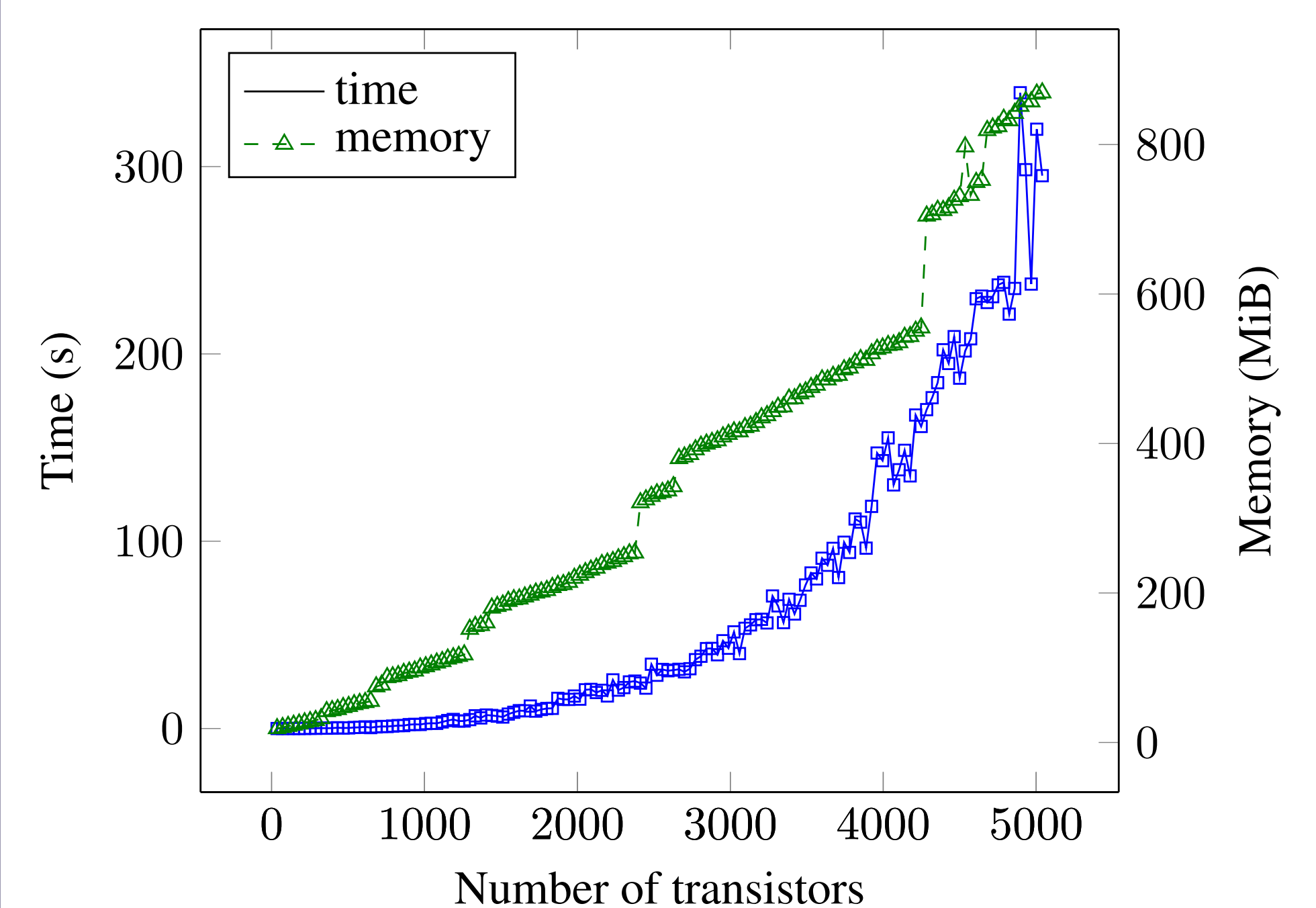


Results (Industrial Usecase)

True errors	False alarms
55 (15%)	314 (85%)

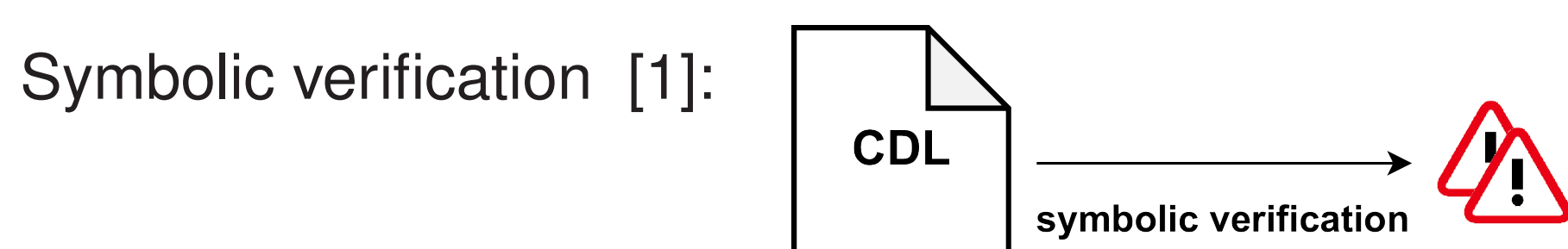
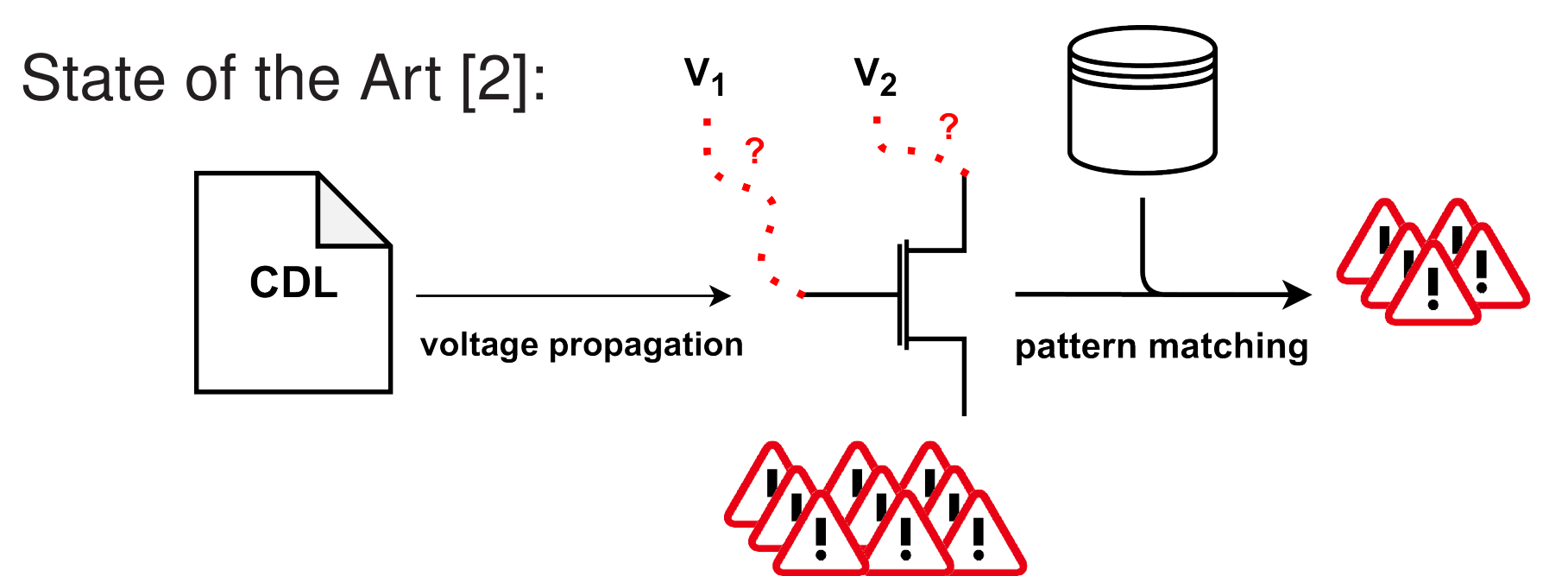
Error refinement on 369 warnings

Z3 Check-SAT time and memory consumption

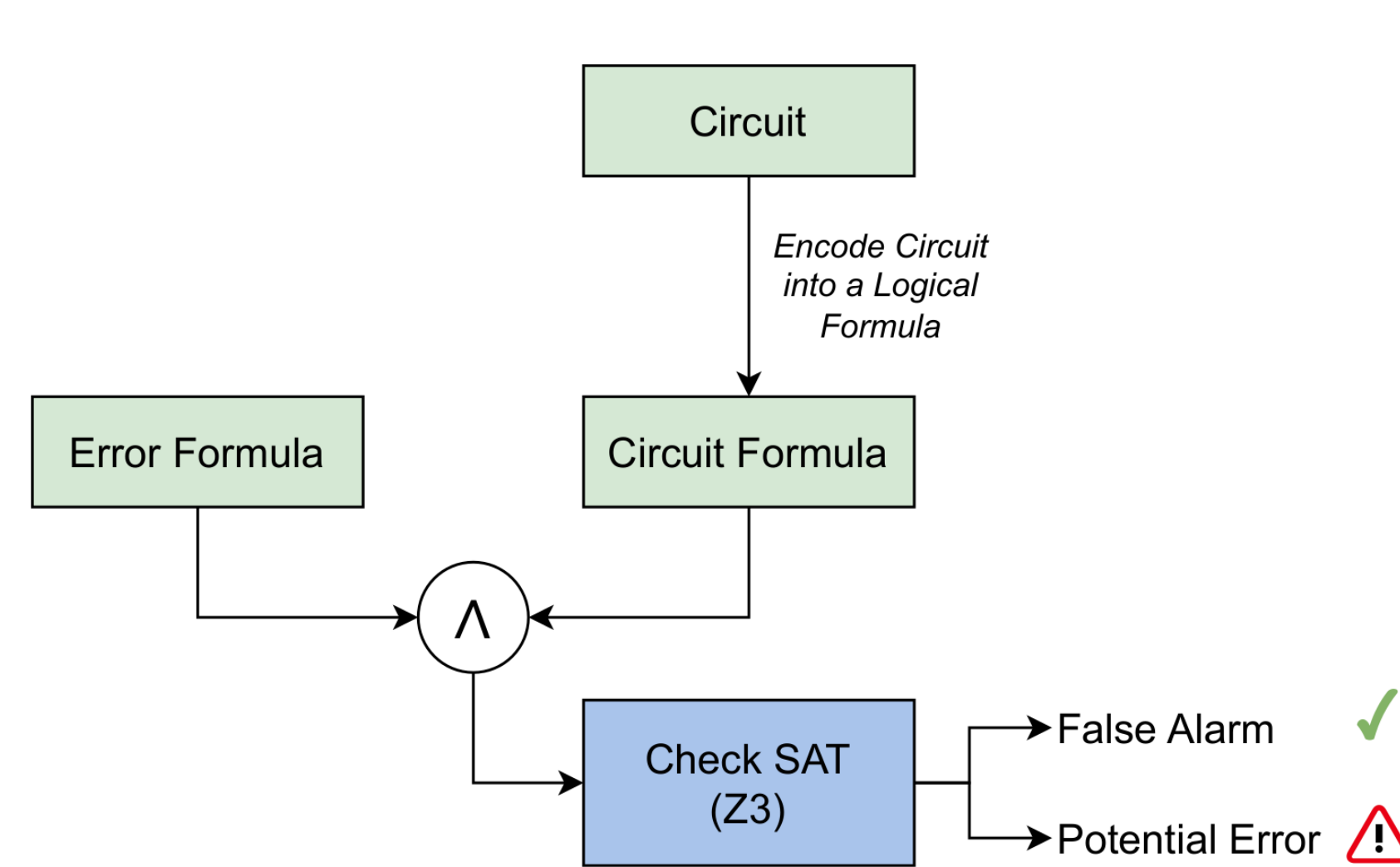


Analysis performances on full-adders

Case Study: Missing Level-Shifter



Verification Process



References

- B. Ferres, O. Oulkaid, L. Henrio, M. Khosravian, M. Moy, G. Radanne, P. Raymond "Electrical Rule Checking of Integrated Circuits using Satisfiability Modulo Theory" In DATE'23, 2023.
- J. Lescot, V. Bligny, D. Medhat, D. Chollat-Namy, Z. Lu, S. Billy, M. Hofmann "Static Low Power Verification at Transistor Level for SoC Design" In ISLPED'12, 2012.