MIETR Automated Deployment of Radio Astronomy Pipeline on CPU-GPU Processing Systems: DiFX as a Case Study

E. Michel¹, O. Renaud¹, K. Desnos¹, A. Deller², C. Phillips³, J.-F. Nezan¹

¹Univ Rennes, INSA Rennes, CNRS, IETR - <u>surname.name@insa-rennes.fr</u> ²CAS, Swinburne University of Technology, Hawthorn, Australia - <u>adeller@swin.edu.au</u> ³CSIRO, Space and Astronomy, PO Box 76, Epping, NSW 1710, Australia - Chris.Phillips@csiro.au

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The Square Kilometre Array (SKA)

System-level architecture modeling for

exascale radio telescope



- The Science Data Processor (SDP) will process data at terabyte rates with a 1 MW, 250 Pflops budget and use modern HPC system.
- Resource allocation for complex algorithms and systems is NP-complete problems.

DiFX correlator dataflow model

Voltage to binary file	-	Data Acquisition	-	Floating point conversion	-	Fringe Rotation	FFT	-	×	Accumulation	-	Visibility

CPU-GPU architecture



GPU-oriented System-Level Architecture Model (GSLA): Λ = ⟨ P, C, L, ĉ, λ ⟩

where P is the set of Processing Elements (PEs), C is the set of Communication Nodes (CNs), L is a set of undirected links connecting PEs and CNs, \hat{c} is a property function associating a cost to different elements in the model, and λ is a Lagrangian coefficient setting the cost of a single communication quantum relative to the cost of a single processing quantum.

Allow system level and internal parallelism description

Dataflow resource allocation for CPU-GPU systems

Clustering SCAPE — Extraction — Mapping — Scheduling — Timing — Translation —

• Six Steps of the DiFX Correlator:

- 1. Data Acquisition: Extracts sampled/quantized voltage from input (antenna data).
- 2. Floating Point Conversion: Converts integers to complex numbers (sample + phase shift).
- 3. Fringe Rotation: Corrects Doppler shifts caused by Earth's rotation.
- 4. FFT (Fast Fourier Transform): Separates signal frequencies (noise vs. useful data).
- 5. Cross-correlation (X): Multiplies frequency data from each telescope pair.
- 6. Accumulation: Connects samples to form final visibility products.

• Dataflow Model:

 $G = \langle A, F \rangle$

where A is the set of actors (computations) and F is the set of FIFO buffers.

 Offers a structured approach to manage parallelism and hardware deployment.



GPU-friendly computation extraction based on pattern matching
Mapping considering offloading gains:

 $p = \begin{cases} CPU, & \text{if } Tim_{CPU}(sub) > Tim_{GPU}(sub) \\ &+ \sum_{\tau \in F_{sub}} \alpha_{n_{CPU}} \cdot \text{size}(\tau) + \beta_{n_{CPU}} \\ GPU, & \text{otherwise} \end{cases}$

• Code translation based on target (CPU \rightarrow C, NVIDIA GPU \rightarrow CUDA)

Result SrDAG Allocation GPU - Manual gcorr Manual fxcorr GPU - Dataflow Manual C 58088 STD(1c) / M(1c, 1g)93.67 CPU - Dataflow STD(8c) / M(1c, 1g)93.67 230509 SCAPE(1c) / M(1c,1g)2.55 13.83 5.64 38.00 SCAPE(8c) / M(1c, 1g)

Summary conclusion

- Achievement:
- Automated dataflow resource allocation method and code generation for heterogeneous CPU-GPU systems.
- ✓ Fast mapping based on computation behavior.

Average reduction factor: the existing methods(STD) over the proposed method (M).1c:1core,1g:1core,the larger, the better.

Significant reduction by
 clustering, reflected in the
 acceleration of the resource
 allocation process.

Speedup resource allocation by a factor of **13** compared to the standard methods.



Execution time by DiFX implementation. The lower, the better.

Optimized dataflow
 implementations compete
 with manual ones.

Implemented into **PREESM** and available on **Github**.

- Future work:
- Scale it up on multi-node modern HPC systems.
- Reorganize scheduling based on component cache (CPU-GPU) integrating polyhedral optimization.













