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Aging impact of the SiC Mosfet gate dielectric

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Abstract

SiC Mosfet is a technology in development for power electronics and especially for automotive applications. Aging of the gate oxide with HTGB stress on a commercial device permits a better understanding of the failure mechanism occurring on the device. Electrical characterization, Raman extraction, Atomic Force Microscope associated with a “resiscope” and XPS-Auger analyses help us to understand the composition of the oxide design and how we can proceed for obtaining a better reliability. An electrical modification related to an atomic variation is detected through the oxidation. Further analyses will be carried out on other devices for comparison.

1. Introduction

In this paper, a commercial SCTW4N120G2VAG SiC MOSFET is studied after High-Temperature Gate Biased (HTGB) stress [1]. This latter is performed until observation of a preponderant modification of the electrical characteristics. We propose a deep study of this failure mechanism in order to delay or prevent such behavior, decreasing the device's performance. Through electrical characterization, a physical failure is observed although the integrity of the device is visually preserved. A first analysis is carried out using micro-Raman characterization and confirms an atomic difference between both devices. Analysis is then performed with the AFM-resiscope and the atomic difference can be traduced into a modification of the electrical behavior. To complete, XPS will be applied to determine the atomic origin of the mutation after aging.

SiC Mosfet was developed for twenty years and reached a level of maturity high enough to be incorporated into several current devices such as the electrical vehicle [2]. Primary failure mechanism and intrinsic impurities density have been corrected for a new generation of power transistors and industrials propose currently the last one as the 4th generation. These devices are destined for power applications, specifically embedded power electronics such as car vehicles. Reliability is therefore a key parameter for avoiding any problems with the electronic design. Although critical failures are avoided with an intelligent design, a slight modification of the electrical behavior can drastically increase the losses, reduce the efficiency, and diminish the autonomy and lifetime of the system. This modification should be evaluated accurately and all improvements into the

technology is welcomed to ensure the longest utilization possible.

2. Stress test and electrical measurements

A current method for aging actively the SiC Mosfet is to vary both temperature and power applied to the component. In our experiment, we focus on the defect created in the gate dielectric after stress. This failure was created after a Gate Switching Stress (GSS) corresponding to a dynamical HTGB with Drain-Source short-circuited. The values of the stress applied during 1000h, for 9e11 number of cycles, on the gate are sorted into Table 1.

A drift voltage is observed in comparison of the pristine device after enough stress when we compare the I_{ds} - V_{gs} characteristic (Fig.1). This characteristic is reproducible and decreases the Mosfet efficiency. Even if the I_{ds} - V_{ds} resistance looks identical, the voltage threshold derives and is increased, leading to a R_{dson} increase for a certain Gate-Source voltage as was already demonstrated in [3] and [4]. Besides, as viewed in Fig.2, I_{gs} becomes proportional to V_{gs} , traducing a failure apparition in the device, as if there was no more a capacitive with few current leakage but a resistive behavior.

Table 1: GSS stress applied to our SiC MOSFET

SN	V_{gs-}	V_{gs+}	Frequency	Tcase	Drift Vth after 1000h
92	-15V	+30V	250kHz	200°C	46.2%

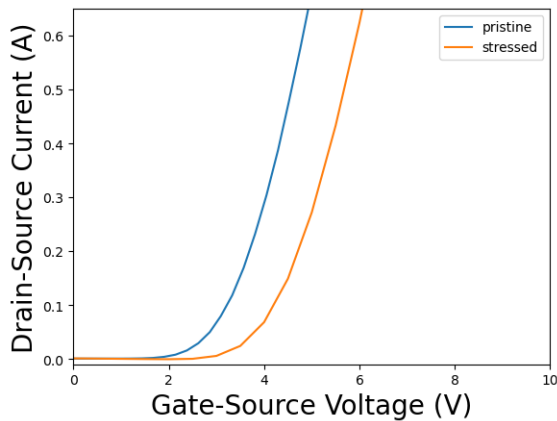


Fig. 1. I_{ds} - V_{gs}

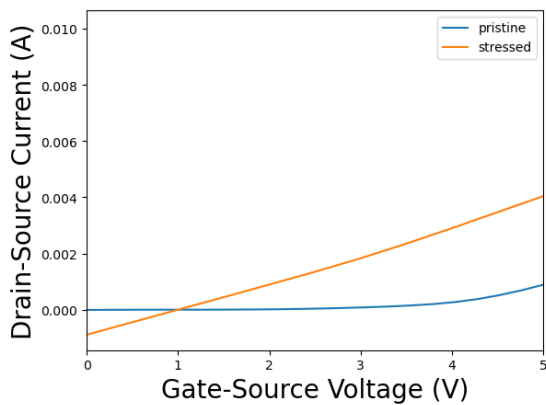


Fig. 2. I_{ds} - V_{ds}

It is fundamental to understand the origin of the electrical modification related to its physical behavior to avoid this kind of failure. That's why we tried to use some specific tools after obtaining a cross-section without any package as spectroscopies tools such as Raman or Atomic Force Microscopy associated with a resiscope for determining the failure mechanism.

3. Micro-Raman analysis

First of all, the commercial device, in a T0247 packaged, is prepared for analysis. Thanks to a specific cut with 30 to 0.01 μm diamond grinding and a flexible 0.01 μm colloidal silicon polishing, a cross-section is obtained. The DUT is then cleaned after a rinse with water DI and alcohol ISO and after drying at 80°C for 60 minutes to take out residual humidity. The AFM technique requires indeed a plane surface with low ruggedness. The result is obtained as shown in Figure 3 where we can observe the cooper platform linked to the Drain, and the SiC semiconductor. On the top, after focusing, we observe centered the gate contact encircled by the Source electrode, overhead

by the package (Figure 3). The gate looks to be made of several pieces, with specific reproducible constraints noted in blue and SiO_2 localized between the blue area and the SiC materials size 400nm.

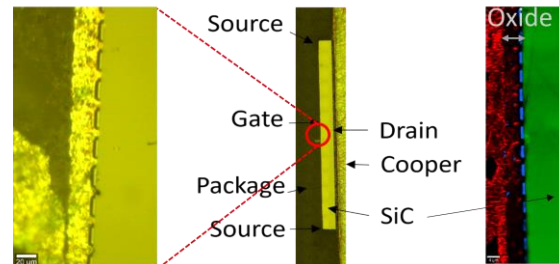


Fig. 3. cross section of the SiC Mosfet

For both samples, a surface Raman mapping of $25 \times 80 \mu\text{m}$ has been performed with 50×800 points. The piezoelectric stage moves from point to point, and for each step, a Raman spectrum is collected. Each single spectrum is recorded through a 100x objective during 0.2s. The 532nm laser power is about 0.5mW on a 1 μm diameter laser spot. The laser critical power threshold has been studied previously. From each spectrum of the recorded data object, we calculate the integrated intensity below the compound Raman signature peak (521 cm^{-1} for Si and 783+799 cm^{-1} for SiC). The surrounding compound has no Raman signature as expected but a phononic background signal. The resulting map (figure 7) is the result of the combination of the Si/SiO₂, of the SiC, and for the compound or other metal signature). These Raman mappings and numerical treatments have been applied for the pristine and the aged samples. From these points, there is no significant difference regarding these integrated intensity maps. For further analysis, we created local individual masks to isolate the Raman data contained in each Si/SiO₂ cluster of the gate region. For each mask, Raman data contained in this Boolean region has been averaged, giving a single Raman spectrum per individual cluster. For a better analysis, we represent in Fig. 4 the averaged Raman signal of Si/SiO₂ for the pristine and the aged samples. For a better visualization, data is normalized by the peak maximum. On the pristine sample, there is no shift evidence but a certain asymmetry of the Raman peak at the low vibration frequencies. This could be due to a local change in bonding length or crystallinity of the Silicon gate. On the aged sample, a vibrational frequency downshift is observed for two of the Si-masked regions. This shift is attributed to a compressive stress in Raman spectroscopy. These two regions also show an asymmetry in the low-frequency region

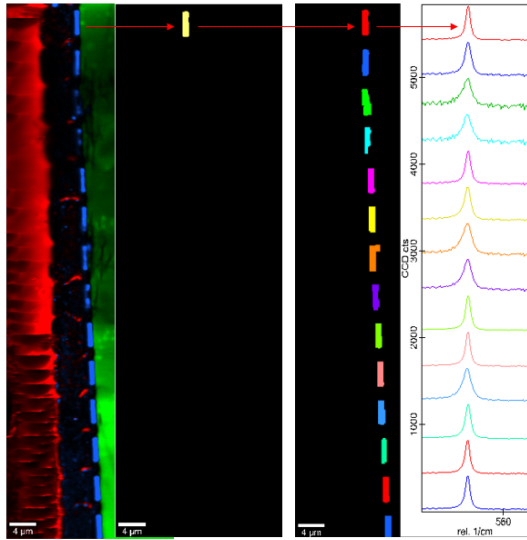


Fig. 4. Individual Gate subregion mask procedure for Raman averaging

The frequency downshift is about 1.5 cm^{-1} , and this could be attributed to a local strain caused by the aging. The Micro-Raman study spectroscopy is applied locally to the SiO_2 -SiC interface. SiC response is similar for the pristine and the aged devices (Fig. 5). On the contrary, a slight shift is observed for the Si/SiO₂ analysis (Fig. 6). A shift is observed traducing a difference of atomic composition only into the Si/SiO₂. Out of the subregion, the signal is as unexploited as it should be in SiO₂. It means that probably an interfacial layer of Si was added to improve the oxide reliability. Nevertheless, if other dielectrics were used, better reliability could be obtained as was demonstrated in [5] even if SiO₂ is one of the most adapted dielectrics [6] for SiC MOSFET.

4. AFM Resiscope

A deeper study has to be carried out in order to determine the atomic nature of the electrical derived observed. To achieve this, a measuring device called "Resiscope" is used in conjunction with an AFM microscope to realize electrical resistance mapping in parallel with a topographic map. Electrical mapping is carried out by polarizing the gate-drain at 10V the sample under test and measuring the local electrical resistance at each point on the surface scanned by a conductive AFM tip. Each electrical image is created pixel by pixel, with a dynamic range of ten decades of resistance (102 Ohms to 1012 Ohms).

After investigation, we can detect higher leakages into the device 92. That means that something was created and impact the capacity behavior of the oxide. It corresponds to traps proposing some interstitial Fermi layers facilitating the current flow.

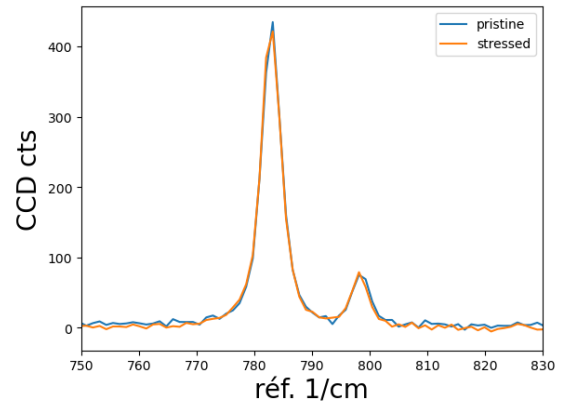


Fig. 5. Micro-Raman SiC comparison between the pristine device and the aged device

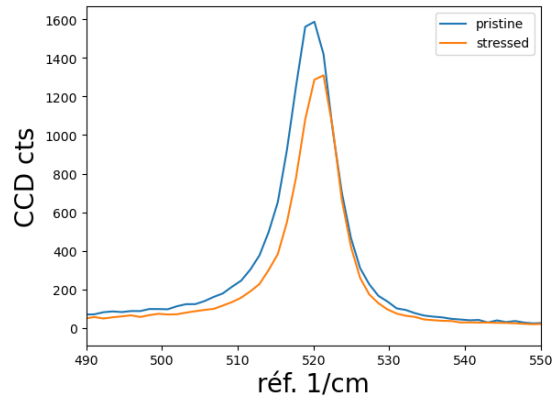


Fig. 6. Micro-Raman SiO₂ comparison between the pristine device and the aged device

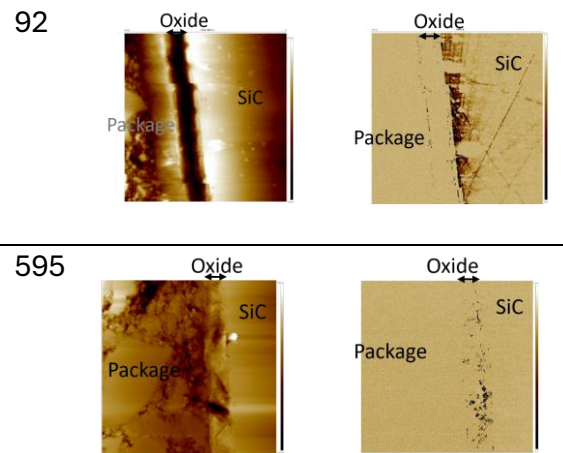


Fig. 2. AFM Resiscope representation of the pristine and the aged device

5. Discussion

The intricacy of the SiO_2 /SiC interface, in comparison to the Si-based structure, causes severe problems even though the mobility is reduced by 5% of the theoretical value. It was demonstrated by surface

potential analysis [7] the existence of high potential fluctuations, which can have a significant impact on the carrier transport at the SiO₂/SiC interface of SiC metal-oxide-semiconductor field effect transistors. Similarly, hall effect measurements justify the presence of traps at the interface [8]. In particular, these measurements give information on the density (~10¹¹ cm⁻²) of near interface oxide traps (NIOTs) present inside the SiO₂ layer and their position with respect to the interface with SiC (at about 1–2 nm) with capacitive measurements and trap characterization [9]. The results demonstrate the existence of an active defect in the gate oxide, located very close to the SiC surface, with localized energy levels between 0.13 eV and 0.23 eV above the bottom of the conduction band. The observed spatial and energy localizations indicate that this is a well-defined defect [10] allowing an electrical model [11]. Finally, it will be shown that a comparison of the electrical data with advanced structural and chemical characterization methods makes it possible to ascribe the NIOTs to the presence of a sub-stoichiometric SiO_x layer at the interface [12]. The 4H-SiC inversion layers are found to have very poor conductance which is caused by severe trapping of electrons at the Si/SiO₂ interface. The trapping causes reduced conductance through a reduction in the number of free electrons in the inversion layer, and also because of a drop in the mobility due to increased Coulombic scattering [13]. The TEM measurement shows the 4H-SiC/SiO₂ interface modification is due to variations in nitric oxide annealing and aluminum implantation [14]. It reveals the presence of distinct layers, several nanometers thick, on each side of the interface. Additionally, partial amorphization of the top SiC surface was observed. These interfacial layers were attributed to the formation of a ternary Si-C-O phase during thermal oxidation.[15]. It was demonstrated the best oxide quality is obtained by means of a dry oxidation process performed at temperatures more than 1100 °C leading to better reliability [6] [8].

7. Conclusion

Through the analysis of a commercial SiC MOSFET, we investigate the SiO₂/SiC interface after aging with an HTGB test. The results demonstrate the presence of Si at the interface between SiO₂ and SiC. A physical degradation of the interfacial layers is observed by the AFM resiscope traducing probably the increase of NIOT density, generating a mobility variation, and increasing the internal resistance of the device. A higher threshold voltage becomes in this case necessary for triggering the transistor. Other devices will be studied in order to understand with

accuracy the oxide inhomogeneity and the relation between the failure and the process of design.

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