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Aging impact of the 4H-SiC MOSFET SiO₂ gate dielectric

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Abstract

Silicon Carbide (SiC) devices are a technology used for power electronics and especially for automotive applications. For MOSFET devices, an aging of the Gate oxide with dynamical HTGB stress called GSS on a commercial device permits a better understanding of the failure mechanism occurring on the device during use. Electrical static characterization Ids-Vds and Ids-Vgs, Raman spectroscopy, Atomic Force Microscope associated with a “resiscope” and Transmission Electronic Microscopy analyses are used to determine the composition of the oxide design and the origin of the failure mechanism. An electrical modification related to a nanometer scale material variation with platelet apparition is detected through the oxidation.

1. Introduction

Silicon Carbide SiC MOSFET is developed for 15 years in replacement of traditional Silicon device with lower internal resistance, lower switching losses and better thermal dissipation [1]. The SiC MOSFET reached a level of maturity high enough to be incorporated into several current devices such as the electrical vehicle [2]. Primary failure mechanism and intrinsic impurities density have been corrected and reduced for a new generation of power transistors and industrials propose currently on the market the 4th generation of transistors. These devices are destined for power applications, specifically embedded power electronics such as automotive vehicles. Reliability is therefore a key parameter for avoiding any problems with the electronic design, as we know that semiconductors are with the capacity the more frequent common failure in power converters. Although critical failures are avoided with an intelligent design, a slight modification of the electrical behavior can drastically increase the losses, reduce the efficiency, and diminish the autonomy and lifetime of the system. This modification should be evaluated accurately and all improvements into the technology is welcomed

In this paper, a component COTS (Component Off The Shelf) SiC MOSFET 1200V-36A is studied after High-Temperature Gate Biased (HTGB) stress [3]. This latter is performed until observation of a preponderant modification of the electrical characteristics. We propose a deep study of this

failure mechanism with some tool’s evaluation for a better understanding of its aging and the consequently decrease of the device’s performance. Through electrical characterization, a physical failure is observed although the integrity of the device is visually preserved. A first analysis is carried out using scanning electron microscopy (SEM), Energy Dispersive Spectroscopy (EPS) and micro-Raman characterization and confirms an atomic variation between a Pristine and a Stressed device. Analysis is then performed with the AFM-resiscope and the atomic difference can be traduced into a modification of the internal resistance at the junction SiO₂/SiC.

2. Stress test and electrical measurements

A current method for aging actively the SiC MOSFET is to vary both temperature and power applied to the component. In our experiment, we focus on the defect created in the Gate dielectric after stress. This failure was created after a Gate Switching Stress (GSS) corresponding to a dynamical HTGB with Drain-Source short-circuited. The values of the stress applied between the Gate and the Source (Vgs) switch from -15V to +30V at 200 °C during 1000 h with a switching frequency of 250 kHz, for 9e11 number of cycles.

A drift threshold voltage is observed in comparison of the Pristine device after stress when we compare the Drain-Source current in function of the Gate-Source voltage, Ids-Vgs characteristic (Fig.1). This characteristic is reproducible and decreases the

MOSFET efficiency. Whereas the variation of the current, hence of the internal resistance $R_{ds_{on}}$, looks identical, the voltage threshold derives and is increased from 46.2%, leading to a $R_{ds_{on}}$ increase for a certain Gate-Source voltage as was already demonstrated in [4] and [5]. Besides, as viewed in Fig.2, the Gate-Source current I_{gs} becomes proportional to the Gate-Source voltage V_{gs} , traducing a failure apparition in the device, as if there was no more a capacitive behavior with few current leakages but a resistive behavior.

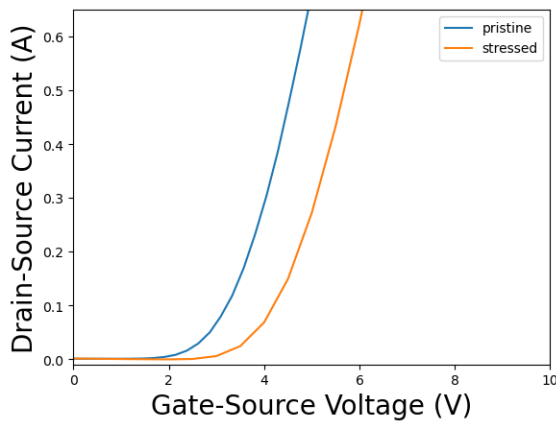


Fig. 1. I_{ds} - V_{gs}

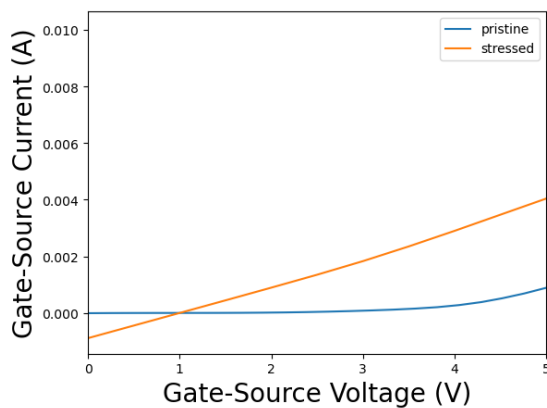


Fig. 2. I_{ds} - V_{ds}

It is fundamental to understand the origin of the electrical modification related to its physical behavior to avoid this kind of failure. That's why we used specific microscopy tools for investigation such as Raman for detecting an atomic variation below the Gate oxide, Atomic Force Microscopy (AFM) associated to a resiscope for detecting a resistance variation related to the failure and Transmission Electronic Microscopy (TEM) for a more accurate failure detection. However, these tools are requiring a

specific preparation for obtaining an unpackaged surface for scanning.

3. Micro-Raman analysis

First of all, the commercial device, in a T0247 packaged, is prepared for analysis. Thanks to a specific cut with 30 to 0.01 μm diamond grinding and a flexible 0.01 μm colloidal silicon polishing, a cross-section is obtained. The DUT is then cleaned after a rinse with deionized water and alcohol isopropyl and dried at 80°C for 60 minutes to take out residual humidity. The DUT can be then observed in Fig 3.



Fig. 3. Physical preparation of the DUT

For both samples, a surface Raman mapping of 25x80 μm has been performed with 50x800 points for compound signature analysis. The piezoelectric stage moves from point to point, and for each step, a Raman spectrum is collected. Each single spectrum is recorded through a 100x objective during 0.2 s (Fig. 5). The 532 nm laser power is about 0.5 mW on a 1 μm diameter laser spot. The laser critical power threshold has been studied previously. From each spectrum of the recorded data object, we calculate the integrated intensity below the compound Raman signature peak (521 cm^{-1} for Si and 783+799 cm^{-1} for SiC). The surrounding compound has no Raman signature as expected but a phononic background signal. The resulting map (Fig. 4) is the result of the combination of the Si/SiO₂, of the SiC, and for the compound or other metal signature). These Raman mappings and numerical treatments have been applied for the Pristine and the Stressed samples. From these points, there is no significant difference regarding these integrated intensity maps. For further analysis, we created local individual masks to isolate the Raman data contained in each Si/SiO₂ cluster of the Gate region. For each mask, Raman data contained has been averaged, giving a single Raman spectrum per individual cluster. For a statistical analysis, we averaged each Raman cluster signature for SiC and Si/SiO₂ for both samples. Data is represented in Fig. 5 and 6 for SiC and Si/SiO₂ respectively, for the Pristine and the Stressed sample. For a better visualization, data is normalized by the peak maximum. For SiC signature, there is no shift evidence nor asymmetry on the Raman signature between Pristine and Stressed sample. However, on the Si/SiO₂ regions, a certain asymmetry and

downshift of the Raman peak is clearly appearing. This could be due to a local change in bonding length or crystallinity of the Silicon Gate and could be attributed to a local strain caused by the aging. On the Stressed sample, the frequency downshift is about 1.5 cm^{-1} , and the FWHM 1.2 cm^{-1} bigger than the Pristine sample. This shift is attributed to a compressive stress in Raman spectroscopy.

Out of the subregion, the signal is as unexploited as it should be in SiO_2 . It means that probably an interfacial layer of Si was added to improve the oxide reliability. Nevertheless, the Raman imaging system spatial resolution is not accurate enough to observe the atomic variation due to this failure. That's why another tool is required for understanding the voltage threshold modification.

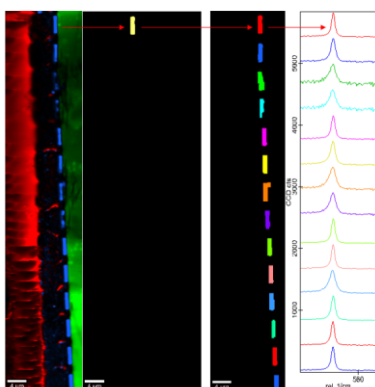


Fig. 4. Individual Gate subregion mask procedure for Raman averaging

4. AFM resiscope investigations

A deeper study has to be carried out in order to determine the atomic nature of the electrical derived observed. To achieve this, an additional technique called “resiscope” based on AFM microscope is used to require electrical resistance mapping simultaneously to a topographic map [6]. This method consists in the application of a voltage and implies a current circulation for observing a local resistance variation permits a more accurate image of the samples and of the defects below the Gate.

Electrical mapping is carried out by polarizing the AFM tip-sample at 1V of both sample and by measuring the local electrical resistance at each point on the surface scanned by a conductive AFM tip. This polarization and this configuration are the ones presenting the best contrast for the image quality and are referred in Table 1. Each electrical image is created pixel by pixel, with a dynamic range of ten decades of resistance (102 Ohms to 1012 Ohms). The structure of the SiC MOSFET is revealed and a thickness of the EPI layer of $14 \mu\text{m}$ is determined device (Fig. 7) in pink traducing such a resistance

whereas the substrate is in yellow. Topography and Deflection error are displayed in addition of the resiscope of the device located below the Gate electrode and unfortunately, it wasn't possible to determine more deeply the failure mechanism thanks to this method because the current value wasn't measured, and the difference of resistance couldn't be interpreted as a structural modification.

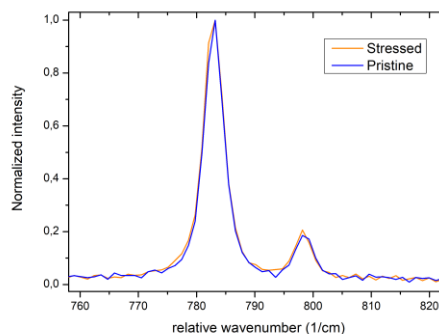


Fig. 5 Micro-Raman average spectra of SiC/SiO_2 regions between the Pristine device and the Stressed device

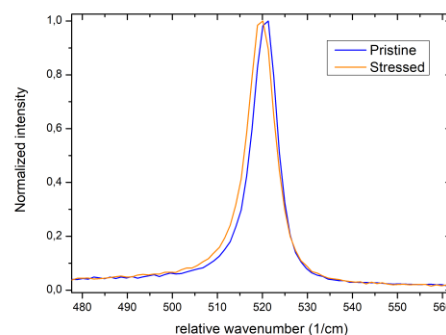


Fig. 6. Micro-Raman average spectra of Si/SiO_2 regions between the Pristine device and the Stressed device

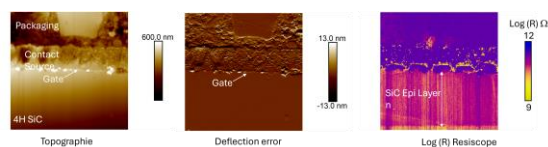


Fig. 7. AFM Topography, deflection error and resiscope of the stressed device.

Scan size	50 μm
Scan rate	0.498 Hz
Samples	256
Aspect ratio	1.00
Capture Direction	Down
Amplitude setpoint	357.79mV
Drive Amplitude	100mV

Table 1. Datas of the resiscope parameters

5. TEM observations

As the previous investigation wasn't relevant for our failure characterization, we reduce the resolution of the analysis by using the Titan microscopy, a TEM able to reach a resolution of 0.08 nm. A sample of both device is taken off via a Focus Ion Beam (FIB) and an EDS is realized for atomic identification (Fig. 8). We can observe in the top the image the presence of Resin in the Aluminum. It corresponds in reality to the failure observed previously with the resiscope analyze. Probably that during the sample preparation, a piece of Aluminum moved and altered locally the internal resistance. We can then separate the different layers with Titanium, a sandwich of SiO₂ over a polysilicon and the SiC substrate.

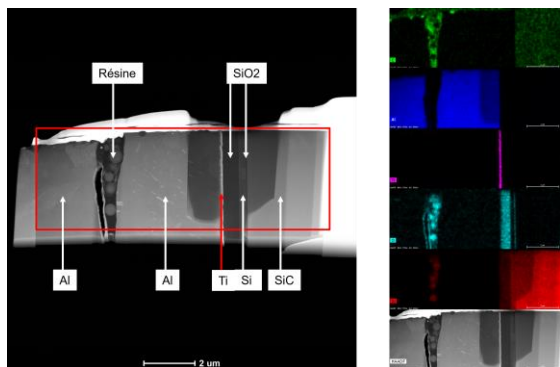


Fig. 8. Sample characterization for HAADF STEM via EDS representation of the stressed device.

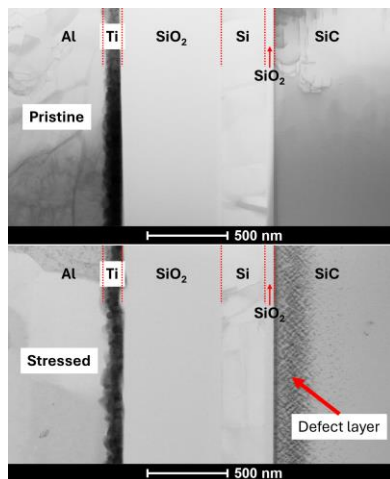


Fig. 9. Bright Field STEM image of the Pristine (top) and the Stressed device (bottom).

This structure is relevant with the literature for a SiC MOSFET trench, as described in [7]. The Bright Field STEM representation displays different result between the Stressed device and the Pristine (Fig. 9).

Apparition of small black points is particularly noticed and could be related to the failure. It corresponds to kind of platelets as described in [8]. A

focused is done on these black points located in the first SiC 200nm.

7. Conclusion

Through the analysis of a commercial SiC MOSFET, we investigate microscopically the SiO₂/SiC interface after aging with a Gate Switching Stress test. The results demonstrate the presence of platelets at the interface between SiO₂ and SiC. A physical degradation due to thermal stress of the interfacial layers is observed by the TEM imagery traducing probably the increase of dislocations, generating a mobility variation, and increasing the internal resistance of the device. A higher threshold voltage becomes in this case necessary for triggering the transistor. Other similar and different devices will be studied in order to confirm this hypothesis due to the thermal degradation at the interface.

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