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Applicability of the Carrier Number Fluctuations Model for Random Telegraph Noise of Nanoscale MOSFETs Operating in Saturation

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Abstract—Random Telegraph Noise (RTN) amplitudes are analyzed for different drain-source voltage biases in bulk MOSFETs issued from a CMOS 40 nm technology. The study highlights the modulation of RTN amplitudes due to the responsible trap’s position along the channel from source to drain. We show that the carrier number fluctuation (CNF) model can still be very accurate for traps located around the middle of the channel, but either underestimates or overestimates the resulting current shift, when applied to traps near the drain or source regions.

Keywords—*Random Telegraph Noise, Carrier Number Fluctuations, MOSFET, Short channel effects, Electrical characterization*

I. INTRODUCTION

Random Telegraph Noise (RTN) acts as an important contributor to the limitation of performances in nanoscale devices and circuits [1] due to its significant amplitude in downscaled MOSFETs. Its parameters can however provide valuable information about the nature of the RTN-inducing traps, as well as their position in the oxide, which is important to enable a robust modeling of its impact on the device’s electrical characteristics and reliability. Previous works [2-6] have shown that the trap’s position along the channel can also modulate the RTN amplitude when the channel is not uniform and impacted by pinch-off effect, as schematized in Fig. 1. We propose to deepen the studies on RTN amplitudes by probing different cases of traps thanks to statistical noise measurements conducted for various drain voltage (V_d) and source voltage (V_s) biases. Firstly, two cases of amplitude profiles are characterized, showing either a symmetrical or an asymmetrical amplitude variation with V_d and V_s . Secondly, we examine the validity of the carrier number fluctuations (CNF) model for traps located around the center or at the edges of the channel.

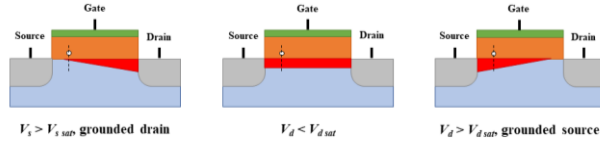


Fig. 1. Representation of the studied devices with a trap located near the source region in the oxide. Three cases are discussed: for source voltage biased in saturation (left), drain voltage biased in linear regime (center) and drain voltage biased in saturation (right).

II. MEASURED DEVICES AND EXPERIMENTAL SET-UP

Silicon bulk nMOSFETs issued from a CMOS 40 nm technology with width $W = 0.3 \mu\text{m}$ and length $L = 40 \text{ nm}$ were selected as a test vehicle for this work. Minimal channel length devices are taken to ensure a channel length modulation effect in saturation. Time domain drain current noise measurements are performed using the NOISYS7 equipment by Synergie Concept. Measurements are undertaken by sweeping the drain/source voltage from linear regime ($V_{ds} = 40 \text{ mV}$) to saturation ($V_{ds} = 1.1 \text{ V}$) by either forcing V_d bias with grounded source or V_s bias with grounded drain. RTN signals are measured each time for a selected gate voltage bias (V_g), and the transconductance ($g_m = \partial I_d / \partial V_g$) is obtained for each V_d (or V_s) by measuring a complementary I_d - V_d curve at a near gate voltage bias $V_g + dV_g$ ($dV_g = 20 \text{ mV}$).

III. RESULTS AND DISCUSSION

Examples of time domain drain current noise measurements are represented Fig. 2 for a device showing RTN in linear and saturation regimes for both V_d and V_s biasing. The amplitude DI_d corresponds to the drain current shift between the two discrete states of the RTN signal.

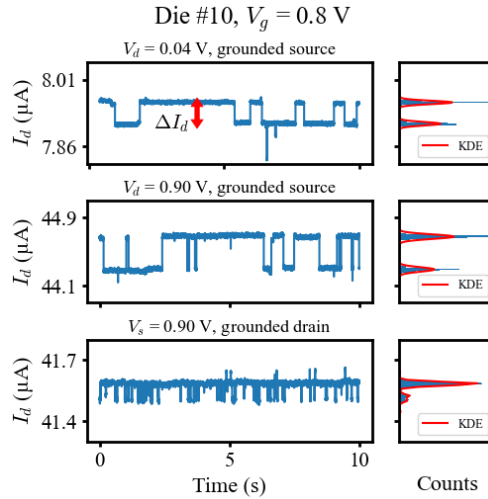


Fig. 2. Example of RTN signals measured in the time domain drain current noise in linear regime (top), saturation with V_d bias (middle) and saturation with V_s bias (bottom), for device #10 at $V_g = 0.8 \text{ V}$.

A. Symmetrical and asymmetrical amplitude profiles

The selected RTN amplitudes DI_d are represented in Fig. 3 and 4, with Fig. 3 showing symmetrical modulations by V_d and V_s , and Fig. 4 showing asymmetrical ones with an attenuation observed for increasing V_s . The case in Fig. 3 can be associated with a trap located around the middle of the channel, whereas the case in Fig. 4 can be associated with a trap located near the source region of the channel, as the charge sensitivity to local potential variations is much smaller in the pinched-off region.

B. CNF model description of the observed amplitudes

While similar observations were also made in [2-5] and while the CNF model should be valid in saturation [7], an experimental proof of the model description for the drain and source voltage dependence of the RTN amplitudes seems to have never been clearly shown. The CNF model reflects the proportionality of DI_d with the transconductance, g_m , and is expressed by $DI_d = DV_{fb} \times g_m$ [7] where DV_{fb} is the equivalent flatband voltage shift. We show through Fig. 3 that the CNF model correctly predicts the amplitude increase as V_d or V_s increases, in a continuous way from linear to saturation region, without adding other parameters. The CNF model is thus valid

for the cases of traps located around the middle of the channel. However, Fig. 4 shows that the CNF model fails to accurately describe the amplitude variations above linear regime when the trap, here located near the source region, sees a higher concentration of charge carriers compared to the channel center. It can also not explain the decrease in amplitude when the trap is above the pinched region of the channel. Therefore, if the CNF model is used to describe the variations in an asymmetrical profile, it ends up overestimating or underestimating D/I_d in saturation region

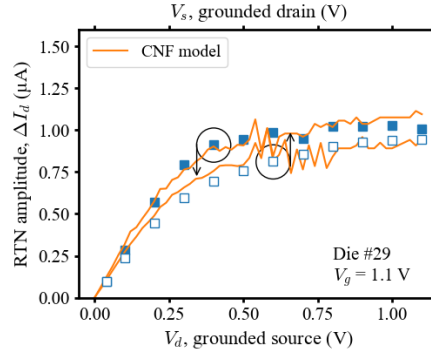


Fig. 3. Amplitude ΔI_d as a function of V_d (closed symbols) and V_s (open symbols), with their respective CNF model fits (lines), for device #29. The profiles are symmetrical.

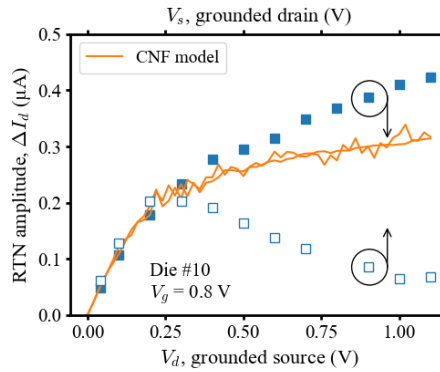


Fig. 4. Same as Fig. 3 for device #10. The profiles are asymmetrical, and the CNF model fails to properly describe the variations.

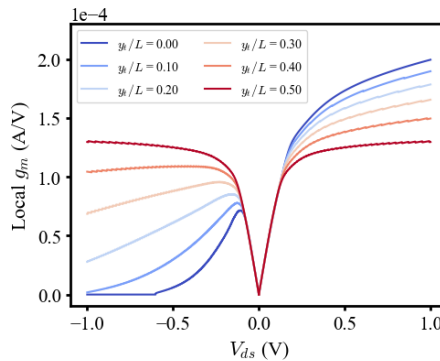


Fig. 5. Lambert W calculated local transconductance as seen by the trap, for various relative channel positions y_t/L .

Nevertheless, our results allow to localize the trap in one of the two sides of the channel (source or drain), depending on which bias mode results in a D/I_d that is higher or lower than $DV_{fb} \times g_m$. To further illustrate how the CNF model could be eventually modified (not shown here) to account for the trap position across the channel, we calculated the local transconductance in various channel positions versus V_d and V_s , using a Lambert W-based MOSFET model. The results shown in Fig. 5 resemble a lot the data trends of Fig. 3 for $y_t/L = 0.5$ and Fig. 4 for $y_t/L = 0.1$ (trap near source).

IV. CONCLUSION

RTN amplitude has been analyzed versus drain and source voltage to assess the trap's location impact. Symmetrical and asymmetrical amplitude profiles have been characterized, providing information on the trap's position along the channel. Finally, we show that the CNF model can accurately describe the amplitude variations for traps located in the middle of the channel, whereas for traps near source or drain regions, it leads to an under- or overestimation of the RTN amplitude, respectively.

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