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Undoped junctionless EZ-FET: model and measurements

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1. Abstract

The junctionless EZ-FET is a device with simplified architecture and processing. With only two lithography levels and using regular process steps, it enables fast electrical characterization of semiconductor films on insulators (SOI) with undoped source and drain. An electrical model reproducing the peculiar transfer characteristics of a junctionless EZ-FET is presented in this work. Based on this model, a simplified parameter extraction methodology is proposed and used to access the electrical properties of SOI structures (i.e. threshold voltage, mobility).

2. Introduction

The EZ-FET is a simple FDSOI-like test vehicle that allows, with only two lithographic levels, an efficient electrical characterization of SOI substrates and gate stacks. Indeed, this device is intermediate between a pseudo-MOSFET [1] used for electrical characterization at the SOI wafer level and a fully processed FDSOI transistor. While the pseudo-MOSFET is quickly fabricated, it only allows back-channel characterization. Alternatively, an FDSOI transistor allows front and back-channel characterization, but is lengthy and costly to fabricate. The EZ-FET combines therefore the fast processing of a pseudo-MOSFET and the complete electrical characterization obtained by an FDSOI transistor. Thus, a quick and reliable feedback on the technological splits of CMOS modules can be obtained using it, and without the need for a fully processed transistor. In the specific context of 3D sequential integration, the top tier, including the top SOI substrate transfer must be processed with a limited thermal budget to avoid degradation of the bottom layers [2,3]. We demonstrated in [4] an EZ-FET with undoped source and drain, fully eliminating dopant activation thermal limitations. This junctionless EZ-FET allows therefore a fast and effective electrical characterization of low temperature SOI substrates. In this work, we propose a model able to correctly reproduce the experimental current-voltage characteristics of a junctionless EZ-FET and a parameter extraction methodology giving access to the film properties and the impact of front and back interfaces.

3. Experiments

Figure 1 shows a schematic of a junctionless EZ-FET fabricated on an FD-SOI wafer with a 12-nm-thick Si film and a 145-nm-thick buried oxide (BOX).
The active layer is defined by mesa etching (1x1,5 mm²). The gate stack is made of a 6 nm thick SiO_2 layer capped by a 50 nm thick TiN layer formed by physical vapor deposition (PVD). Subsequent lithography and etching define a gate stack on top of the silicon slab.
The carrier's distribution in the active film of the EZ-FET can be controlled through the coupling effect [5] by the front gate V_{FG} and back gate V_{BG} that work in tandem. However, the source and drain regions are governed by the back gate exclusively. Moreover, since these regions are undoped, there are no free carriers reservoirs that allow a current flow in the front and/or back channels. The back-gate is mandatory to induce

an “electrostatic doping” of the source and drain regions by providing free charge carriers and therefore enabling a current flow in the film, closer to front or back interface, depending on the V_{FG} bias.
In order to ensure an ohmic contact in the source and drain regions we use a semi-automatic measurement station with manual probes.

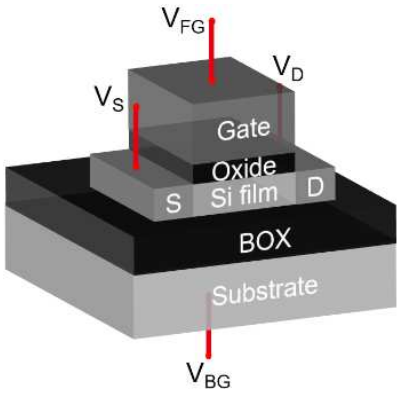

Figure 1: Schematic of an EZ-FET device with probes directly placed on the gate, source and drain regions.

Figure 2 (a) shows the experimental back-gate transfer characteristics I_D-V_{BG} for various V_{FG}. The curves present three important features:
- The shape of the curves is similar to the ones obtained for pseudo-MOSFETs [5], since the junctionless EZ-FET enables either electrons or holes conduction in the channel, according to the polarity of the back gate voltage: the electron channel obtained for positive V_{BG} is replaced by a hole channel when V_{BG} becomes negative.
- The curves are horizontally shifted by changing the front-gate voltage V_{FG}, reflecting the classical coupling effect in FD-SOI MOSFETs [6].
- With decreasing V_{FG} the absolute value of the back hole channel threshold voltage $V_{T,BG}$ is lowered until it reaches saturation and all subsequent curves tend to merge. Such saturation occurs when the resistance of the channel region becomes small enough thanks to V_{FG} and the total current is limited by the conductance in the S/D terminals (that are only controlled by V_{BG}). The reciprocal effect is observed for the electron channel, under high positive V_{FG}.

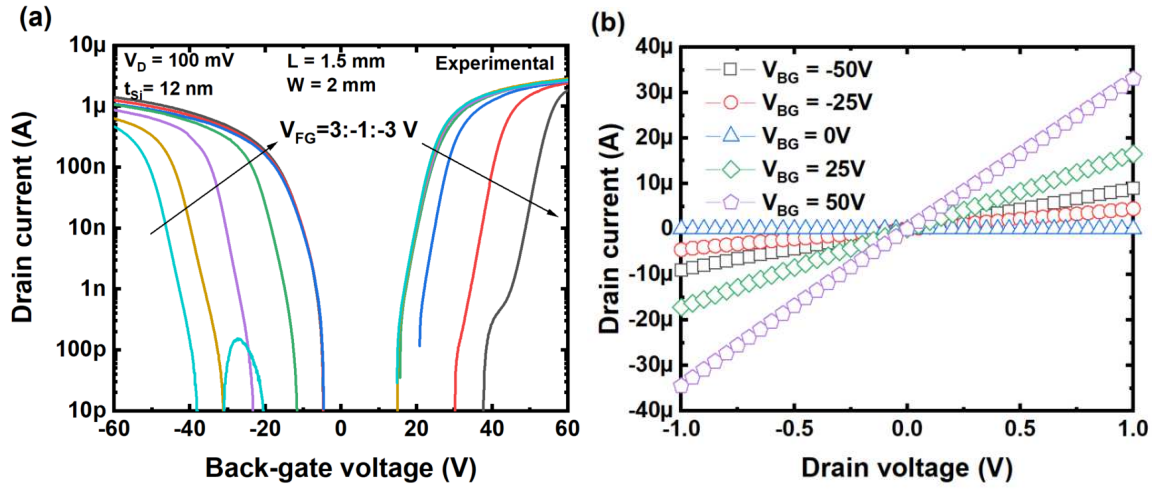

Figure 2: (a) Experimental I_D-V_{BG} curves for V_{FG} varying from 3V to -3V with a -1V step, (b) Experimental I_D-V_D curves for V_{BG} varying from -50V to 50V with a 25V step.

Figure 2 (b) displays the I_D-V_G curves that show a linear behavior for various back-gate voltages. This confirms the ohmic conduction for both holes (negative V_{BG}) and electrons (positive V_{FG}).

The $I_D(V_{FG})$ characteristics measured by sweeping V_{FG} for different V_{BG} voltages are displayed in Figure 3. Although these curves contain useful information about the quality of the front interface and gate stack

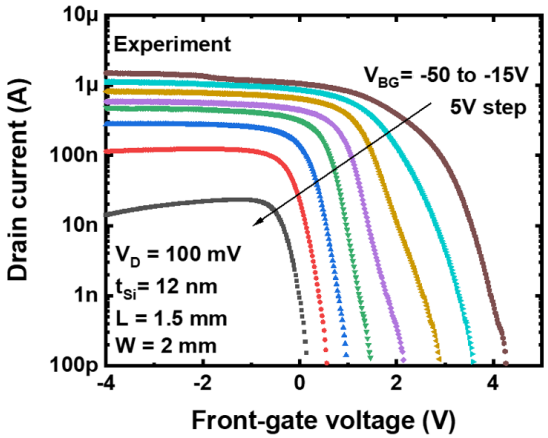

Figure 3: Experimental I_D-V_{FG} curves of the hole channel for V_{BG} varying from -50 to -15V with a 5V step.

through μ_0 and V_T for instance, care is needed to select the region for parameter extraction. Indeed, lowering the back-gate voltage value results in a shift to the right (higher front-gate threshold voltage V_{TF}) which is again the classical coupling effect ΔV_{TF} / ΔV_{BG} [6]. However, the massive current drop observed for low V_{BG} is less expected. This peculiar effect can be explained by the drastic increase of the series resistance in the S/D regions, where the low free carriers density limits the transport across the device. Therefore, accurate front-channel parameters should be extracted from the drain current obtained at back-gate voltages high enough so that the series resistance is not a limiting factor. The next section describes the model proposed to reproduce these experimental results.

4. Model

Our model is based on the equivalent circuit of an EZ-FET operated in an ohmic regime (Figure 4): the series resistance R_S is in series with the parallel association of the front-channel resistance R_{FG} and the back-channel resistance R_{BG}.

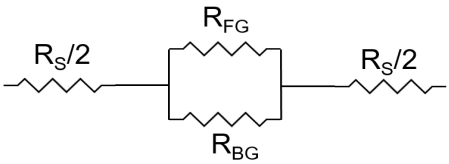

Figure 4: Equivalent circuit of the junctionless EZ-FET operated in ohmic regime.

The resistances and charge expressions for each of the elements of Figure 4 are given below using Ohm's law and Lambert function expression of the inversion charge [6].

$$R_S(V_{BG}) = \frac{1}{\frac{W}{L_D - L}\frac{\mu_{0_{BG}}}{1+\frac{\theta_{BG}Q_{i_S}}{C_{box}}}Q_{i_S}} \qquad Q_{i_S}(V_{BG}) = C_{box}n_S\frac{kT}{q}LW\left(e^{q\frac{V_{BG}-V_{T_{BG}}}{n_S kT}}\right) \quad (1)$$

$$R_{FG}(V_{FG}) = \frac{1}{\frac{W}{L}\frac{\mu_{0_{FG}}}{1+\frac{\theta_{FG}Q_{i_{FG}}}{C_{ox}}}Q_{i_{FG}}} \qquad Q_{i_{FG}}(V_{FG}) = C_{ox}n_{FG}\frac{kT}{q}LW\left(e^{q\frac{V_{FG}-V_{T_{FG}}}{n_{FG}kT}}\right) \quad (2)$$

$$R_{BG}(V_{BG},V_{FG}) = \frac{1}{\frac{W}{L}\frac{\mu_{0_{BG}}}{1+\frac{\theta_{BG}Q_{i_{BG}}}{C_{box}}}Q_{i_{BG}}} \qquad Q_{i_{BG}}(V_{BG},V_{FG}) = C_{box}n_{BG}\frac{kT}{q}LW\left(e^{q\frac{V_{BG}-(V_{T_{BG}}-\alpha_{FG}V_{FG})}{n_{FG}kT}}\right) (3)$$

W is the gate width, L_D is the device length, L is the gate length, μ_0 is the low-field mobility, θ is the attenuation factor, Q_i is the inversion charge, C_{box} is the BOX capacitance, C_{ox} is the front-gate oxide capacitance, n is the ideality factor, $\frac{kT}{q}$ is the thermal voltage at 300K and LW refers to the Lambert function [7].

Starting from these simple equations, a resistance ratio R_S/R_{gate} can be calculated. R_{gate} is given by the parallel association of R_{FG} and R_{BG}. Figure 5 shows this ratio for holes transport. At negative V_{FG} values, the channel resistance is very small. Therefore the S/D resistance is dominant with respect to the channel one, which results in the V_T saturation observed experimentally in Figure 2.

The total current I_D of the structure can be calculated as:

$$I_D(V_{BG},V_{FG}) = \frac{V_D}{R_S(V_{BG}) + \frac{R_{FG}R_{BG}}{R_{FG}+R_{BG}}(V_{FG},V_{BG})} \quad (4)$$

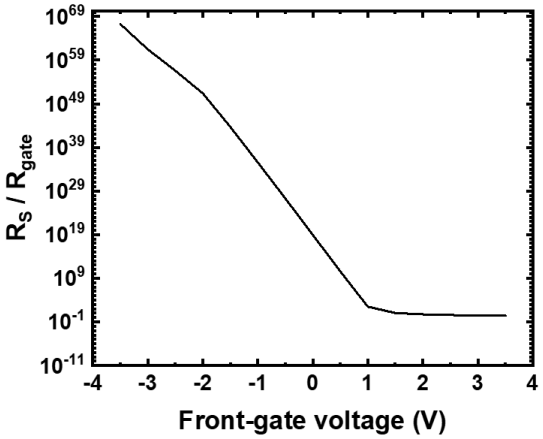

Figure 5: Modeled series and gate resistances ratio at various V_{FG}.

Using this equation and reference key parameters (μ_0, V_T) consistent with a standard EZ-FET with doped S/D [4], we reproduce the measured $I_D(V_{FG},V_{BG})$ behavior, with V_T saturation in I_D-V_{BG} plot (Figure 6) and current drop at low V_{BG} in I_D-V_{FG} plot (Figure 7) for holes. The inset in Figure 6 shows an example of an I_D-V_{BG} plot for electrons.

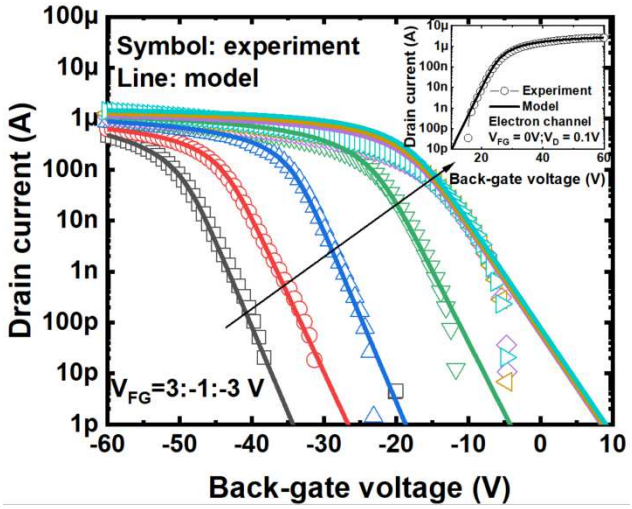

Figure 7: Experimental (symbols) and modeled (lines) I_D-V_{BG} curves at various V_{FG} for a hole channel. For example, the fit of the left curve (V_{FG}=3V) is obtained using μ_0 = 27cm²/Vs, V_T = -54V, and θ = 0.05 /V. Inset graph shows an example of experimental and modeled I_D-V_{BG} curves for an electron channel.

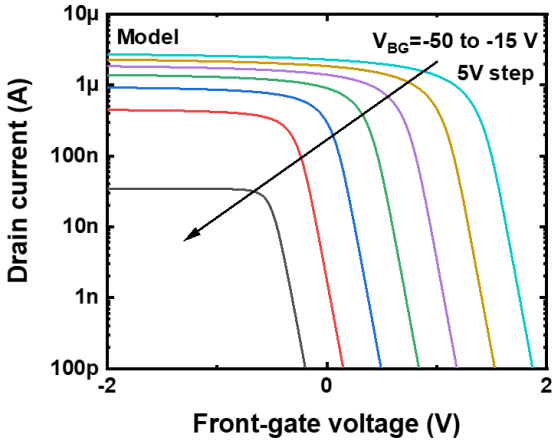

Figure 6: Modeled I_D-V_{FG} curves at various V_{BG}.

Using a simplified version of this model, an extraction methodology is proposed in the next section.

5. Parameters extraction

Since Equation (4) includes 8 fitting parameters (n_{FG}, V_{TFG}, μ_{0FG}, θ_{FG}, n_{BG}, V_{TBG}, μ_{0BG}, θ_{BG}), a direct fit of current curves would be complicated. Therefore, the extraction methodology is based on specific cases and voltage ranges enabling the determination of back-gate and front-gate parameters thanks to curve fittings. Three steps are needed for complete parameters extraction: first, an open front-gate I_D-V_{BG} measurement to extract R_S, then an I_D-V_{BG} measurement at various V_{FG} to extract back-gate parameters, and finally an I_D-V_{FG} measurement at a specific V_{BG} to extract front-channel parameters.

Step 1: Series resistance

The front-gate is floating, the EZ-FET is then equivalent to a pseudo-MOSFET [6]. The open front-gate experimental current is fitted with the following model:

$$I_{D_{open}}(V_{BG}) = \frac{V_D}{R_{S_{open}}(V_{BG}) + R_{BG_{open}}(V_{BG})} \quad (5)$$

This fit provides the open front-gate parameters n*, V_T*, μ_0*, θ* and therefore the series resistance:

$$R_S(V_{BG}) = \frac{V_D}{\frac{W}{L_D - L}\frac{\mu_0^*}{1 + \frac{\theta^* Q_i^*}{C_{box}}} Q_i^* V_D} \qquad Q_i^*(V_{BG}) = C_{box} n^* \frac{kT}{q} LW \left(e^{q\frac{V_{BG} - V_T^*}{n^* kT}} \right) \qquad (6)$$

Step 2: Back-channel properties

For simplicity, we limit the extractions to the region where the front-channel is off (positive V_{FG} and high R_{FG}) by neglecting the front-gate resistance in Equation (4). $R_S(V_{BG})$ is then replaced by its extracted value in step 1, leaving only the back-gate parameters unknown. A fit of this new current expression for every V_{FG} value is performed in order to extract the back-gate parameters for each V_{FG}. Figure 8 presents the extracted threshold voltage for different V_{FG} values. The graph clearly reproduces the V_T saturation for high negative V_{FG} values as explained in part 3. To overcome this saturation, and given the linear coupling relationship [5],

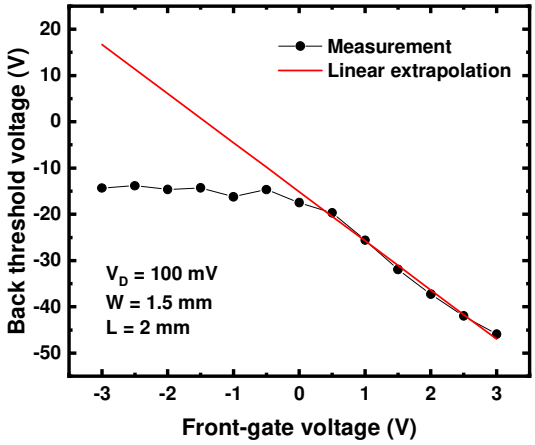

Figure 8: Extracted V_T values at various V_{FG} biases.

a linear extrapolation from the positive V_{FG} range yields the threshold voltage at negative V_{FG}.

Figure 9 shows the extracted μ_0 for different V_{FG} values. The graph evidences the gate coupling in this device, through the decrease of the mobility at positive V_{FG} values. Indeed, for holes transport, a positive V_{FG} bias increases the vertical field repelling the holes in the film towards the Si / BOX interface, which degrades the mobility due to interface effects (roughness, interface states density …). Moreover, the extracted values are comparable to those in a sample with doped source and drains with the same gate stack [4].

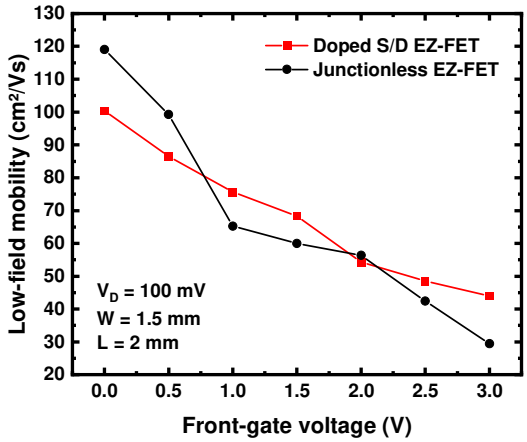

Figure 9: Extracted hole mobility μ_{0BG} values at various V_{FG} biases.

Step 3: Front-channel properties

The threshold voltage and carrier mobility of the front-channel are determined by maintaining the back channel in strong inversion to limit the series resistance R_S. Only the strong inversion regime of the front channel is of interest. This means that V_{TBG}, R_{BG} and R_S are constant, leaving only R_{FG} as unknown in equation (4).

The conductance varies linearly with V_{FG}

$$G_{FG} = \frac{1}{R_{FG}} = \frac{1}{\frac{V_D}{I_D} - R_{S_{BI}}} - \frac{1}{R_{BG_{BI}}} = \frac{\mu_{O_{FG}} C_{ox} W}{L}\left(V_{FG} - V_{T_{FG}}\right) \quad (7)$$

where the index BI refers to a chosen value corresponding to the Back-channel Inversion. This linear fit allows the extraction of $\mu_{O_{FG}} = 76\ cm^2/Vs$ and $V_{T_{FG}} = 1.2\ V$ from the slope and intercept.

Experimental results confirm that this methodology can be used to determine key parameters not only in the back channel, as with a pseudo-MOSFET [1], but also in the front-channel.

6. Conclusions

The junctionless EZ-FET is a simple test device with a peculiar behavior: the back-gate is mandatory to electrostatically induce free carriers in the source and drain regions. Additionally, the channel region can be controlled by both the front and the back gates, eventually its resistance becomes lower than the S/D one. This results in a V_T saturation in I_D-V_{BG} characteristic and a massive current drop in I_D-V_{FG} curves for low V_{BG}. The proposed model effectively reproduces both effects. Using a simplified version of this model and a three-step methodology, key film parameters were extracted and were consistent with that in a doped S/D EZ-FET reference. Therefore, the junctionless EZ-FET enables electrical characterization of semiconductor films without junctions doping and activation, making it most interesting for 3D sequential integration applications. This methodology could also be adopted for characterization of two-dimensional semiconductor channels, even for materials that cannot be doped, since the typical doping techniques used for Si devices destruct the crystalline lattice of 2D materials. A junctionless EZ-FET would therefore eliminate the implantation step, and allow an electrical evaluation of devices with 2D materials channels.

Acknowledgements

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