Small-Signal Characterization and Modelling of a Back Bias Reconfigurable Field Effect Transistor

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Bruno Neckel Wesling*†, Marina Deng†, Talha Chohan‡, Violetta Sessi‡, Steffen Lehmann‡, Maximilian Drescher‡, Chhandak Mukherjee†, Stefan Slesazeck*, Thomas Mikolajick*§, Cristell Maneux†, and Jens Trommer*
*NaMLab gGmbH, Nöthnitzer Str. 64 a, 01187 Dresden, Germany
†IMS, 351 Cours de la Libération, Talence Cedex, 33045, France
‡Global Foundries Fab1, 01109 Dresden, Germany
§Chair for Nanoelectronics, TU Dresden, 01187 Dresden, Germany

Email: bruno.neckel-wesling@u-bordeaux.fr

***Abstract*—In this work, we present the first small signal characterization of a reconfigurable field effect transistor. The device under test is a back-bias RFET integrated into an industrial 22nm FDSOI platform. These devices are particularly interesting for CMOS co-design as they enable a frequency doubling functionality using a single transistor, without the need for inductive elements. Extraction of figures of merit and a comprehensive small signal analysis are performed. It is demonstrated that an ambipolar back-bias reconfigurable field-effect transistor can be modelled using a conventional small-signal equivalent circuit. This shows promise for modelling engineers and circuit designers to explore innovative applications of this new emerging technology.**

***Index Terms*—silicon-on-insulator, emerging devices, reconfigurable field effect transistor, small signal equivalent circuit, RF characterization**

I. Introduction

Continuous downscaling of silicon devices has pushed them to their physical limits in the recent decades [1]. Despite the fact that the scaling roadmap has presumably reached its so-called end multiple times, integration of new features has kept it as one of the most advanced technological elements for a multitude of applications [2]. Therefore, new technological solutions to increase system functionality, without scaling down the individual feature size, have become of increasing interest.

One such solution, that can be integrated in a fully depleted silicon-on-insulator (FDSOI) platform is the reconfigurable field effect transistor (RFET). RFETs have been proposed for a series of digital applications due to their capability to operate as an N-type or a P-type transistor [3]–[5]. The realization of back-bias RFETs (BB-RFET) in a 22 nm fully-depleted silicon-on-insulator (FDSOI) technology platform has been already demonstrated [6], [7]. The BB-RFET devices use the voltage applied at the back-gate, which is inherently present in FDSOI transistors, to define the device‘s operation mode.

These devices are especially interesting for low-frequency analog applications as they enable a frequency doubling operation using a single transistor, without the need for inductive elements [7]. Application scenarios of adaptive tunable frequency mixers and rectifiers based on RFETs have been recently proposed [7], [8]. Being a rather new technology with non-conventional transport physics [3], there is a lack of accurate models for RFETs. A first table model capable of capturing the frequency doubling behavior was recently reported [8]. However, analog circuit design typically requires a more accurate and detailed representation of the small signal behavior of the circuit elements.

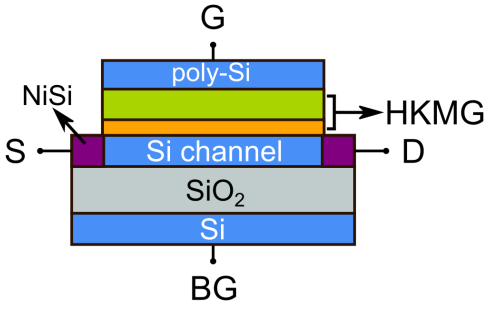


Fig. 1. Schematic of a back bias reconfigurable field effect transistor.

In this work, we performed S-parameter characterization of an industrially fabricated BB-RFETs, for the first time, providing an analyse of the RF operation followed by an extraction of a small-signal equivalent circuit. Our results can potentially help with future model building for these emerging devices.

II. Process Integration of BB-RFETs

The experimental Back-Bias Reconfigurable Field Effect Transistors, presented in this work, have been processed on the 22FDX® technology platform offered by Global Foundries [9]. The devices are built on a thin, virtually doping-free, SOI substrate with 20 nm thick buried oxide [7]. The RFET integration flow shares most of the modules with that of n-FET core-devices, such as shallow-trench isolation (STI), gate-first high-k metal gate (HKMG) integration, and spacer deposition. Modified source and drain terminals are applied to allow for a sufficient nickel-silicide (NiSi) intrusion into the channel in order to create silicide-to-semiconductor junctions that reach below the gate level (see Fig. 1). A post-STI hybrid etching process is used to form a contact on the doped silicon back-

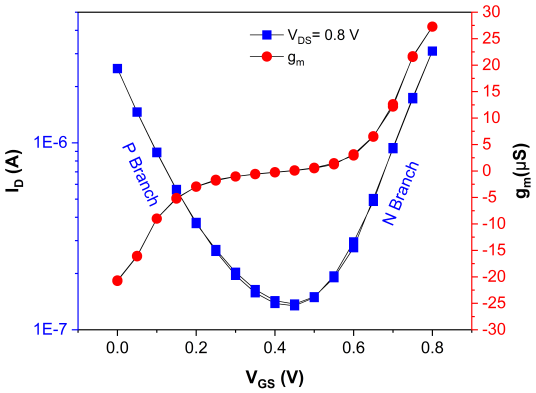


Fig. 2. Typical transfer characteristics and transconductance as a function of the gate voltage for an ambipolar BB-RFET.

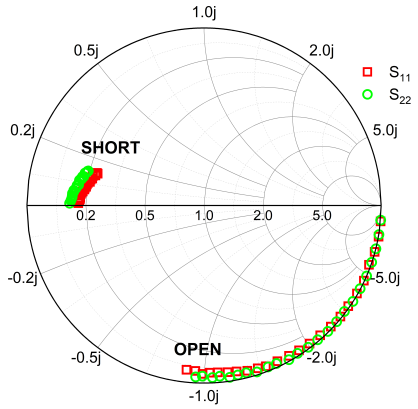


Fig. 3. S_{xx} parameters from the open and short structures.

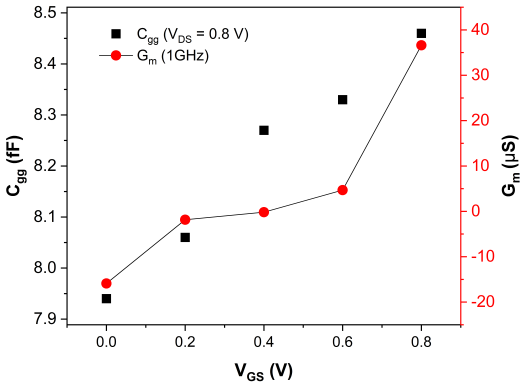


Fig. 4. Variation of the total input gate capacitance C_{gg} and transconductance G_m extracted at 1 GHz versus the gate voltage (V_{DS} = 0.8 V).

gate [9]. Finally, the back-end-of-line (BEOL) is processed to form ground-signal-ground (GSG) test structures compatible for small-signal RF characterization. The transistor analyzed in this work consists of 16 parallel fingers each having a gate length (L_g) of 20 nm and a width (W_f) of 1 μm.

III. DC AND RF CHARACTERIZATION UP TO 24 GHZ

DC measurements were performed with a Keithley 4200A-SCS Parameter Analyzer. On wafer S-parameter measurements have been performed in the frequency range of 1 GHz up to 24 GHz, using a vector network analyser (Rohde & Schwarz ZVA24) and |Z| Probe® RF probes with a 100 μm pitch. Two DC probes were connected to the back gate and source pads allowing the possibility of applying different potentials. In the context of this work, the DC probes were kept grounded, meaning that the BB-RFET was operated in ambipolar mode for all characterizations performed in this study. Corresponding open and short structures were available for the de-embedding of the devices under test. Additionally, a Short-Open-Load-Thru (SOLT) calibration was performed on a CSR-8 calibration substrate, paired with the probes, prior to the on-wafer S-parameter measurements.

A. DC Characterization

The typical ambipolar transfer curves I_D-V_G for a BB-RFET are presented in Fig.2. The drain-current curve has a nearly parabolic shape with distinct N- and P-branches. Near-symmetric operation was thus achieved. The slight offset between the maximum currents for the P- and N-branches can be attributed to the difference in initial band bending induced by the combination of the silicide and the gate materials. This difference results in a higher absolute value of transconductance for the N-branch.

B. RF Characterization

The analysis of the de-embedding structures is crucial in order to ensure that most of the external parasitics are removed from the device under test. The S-parameters obtained from the open and short structures are presented in Fig. 3. The open structure exhibits a near-pure capacitive behaviour, while the short structure exhibits a standard inductive-resistive behaviour. The quality of the de-embedding process could be further improved by using a distributed approach that involves fabricating more dummy structures. However, this would require additional silicon area [10], [11].

After de-embedding, a deeper investigation of the RF properties of the intrinsic device was performed. The total input gate capacitance C_{gg} was obtained from the de-embedded Y-parameters using $C_{gg} = Im(Y_{11})/\omega$. The value of C_{gg} incorporates the intrinsic as well the fringing capacitances. The extrinsic transconductance G_m was obtained from $G_m = real(Y_{21})$. The variation of C_{gg} over gate voltage and the G_m extracted at 1 GHz are presented in Fig 4. From these parameters, the cut-off frequency f_t can be extracted by $f_t = |(G_m/2\pi C_{gg})|$ and plotted as a function of the gate voltage as shown in Fig. 5. It is evident, that F_t has a stronger dependence on the transconductance than on C_{gg}, which exhibits only a 0.5 fF increase when V_{GS} is swept from 0 to 0.8 V. Within the given operating range, the highest f_t values are obtained at V_{GS} = 0.8 V and 0 V meaning on the top of the N-branch and the P-branch of the ambipolar curve, respectively. These values give a first insight into the achievable frequency

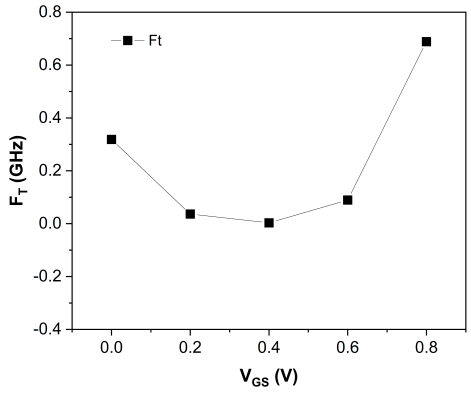


Fig. 5. Estimated current gain cut-off frequency versus gate voltage (V_{DS} = 0.8 V).

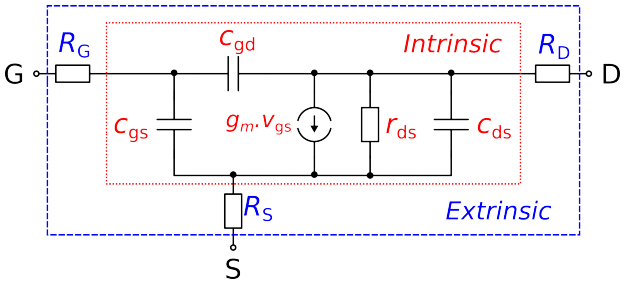


Fig. 6. Small-signal equivalent circuit model in the strong inversion.

doubling performance. It should be noted that rather low F_t values are observed for the particular operating point around V_{min} at 0.4 V where G_m is naturally zero. However, even more important insights on the intrinsic device characteristics can be gained from the small signal model presented in the next section.

IV. BB-RFET Small Signal Modelling

A conventional small-signal equivalent circuit (SSEC) proposed for the ambipolar BB-RFET and is presented in Fig.6. The SSEC model parameters were extracted for the two highest polarization points, one for the P-Type (V_{GS} = 0 V) and the other for the N-Type (V_{GS} = 0.8 V) for a fixed V_{DS} = 0.8 V.

Assuming that the current injection through the Schottky Barriers (SB) can be modeled by a single resistance, the extractions of the extrinsic parameters R_D and R_S were performed based on a demonstrated method utilized for SB-MOSFET. This technology also uses SB at the source and the drain sides, as in the BB-RFET [12]. Equations 1 and 2 were used to estimate the resistances near the highest measured frequency points. This method takes into account the bias dependence of the access resistances.

$$R_D = Re(Z_{22} - Z_{12}) \tag{1}$$

$$R_S = Re(Z_{12}) \tag{2}$$

The gate resistance, R_G, is expected to be in the order of a few Ohms, as already demonstrated for similar devices fabricated on the same platform [10]. In the RFETs of this work, R_G has its value overshadowed by noise and the high R_S and R_D values, making it impossible to extract a physically valid value. For the small-signal simulations in this work, the resistance R_G was thus considered to be zero. The source and drain resistances for the P-branch were 801 and 300 ohms, respectively (V_{GS} = 0.0 V), while for the N branch they were 965 ohms and 347 ohms, respectively (V_{GS} = 0.8 V).

The removal of the extrinsic elements were done by subtracting the Z parameters of the extrinsic parasitic network from the Z parameters of the device under test. The resulting values were then transformed into Y parameters, and the intrinsic elements were calculated using the following equations:

$$c_{gs} = Im(Y_{11} - Y_{12})/\omega \tag{3}$$

$$c_{gd} = -Im(Y_{21})/\omega \tag{4}$$

$$c_{ds} = Im(Y_{22} + Y_{12})/\omega \tag{5}$$

$$r_{ds} = 1/Re(Y_{22} + Y_{12}) \tag{6}$$

$$g_m = Re(Y_{21}) \tag{7}$$

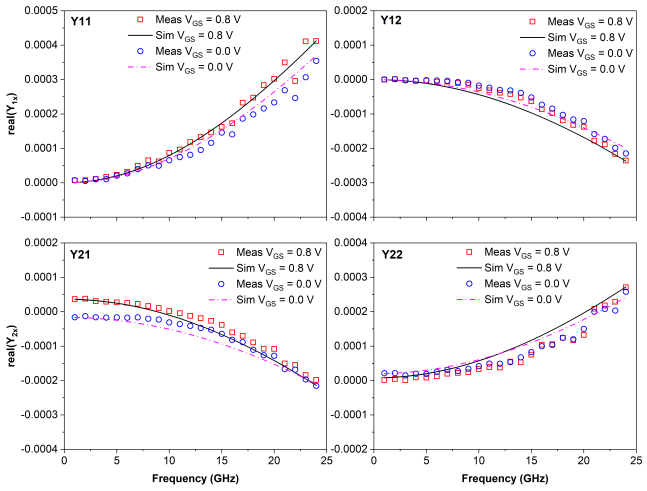
The use of S-parameter characterizations enable precise determination of the intrinsic parameters of the short-channel devices. This approach overcomes the limitations of conventional capacitance-voltage (C-V) measurement techniques, which rely on large C-V test structures and are inadequate for capturing the capacitance behavior in such scaled devices. Table I presents the intrinsic parameters obtained, along with the extrinsic resistance values.

TABLE I
VALUES OF THE EXTRACTED PARAMETERS UTILIZED FOR THE SIMULATION OF THE EQUIVALENT CIRCUIT (V_{DS} = 0.8 V).

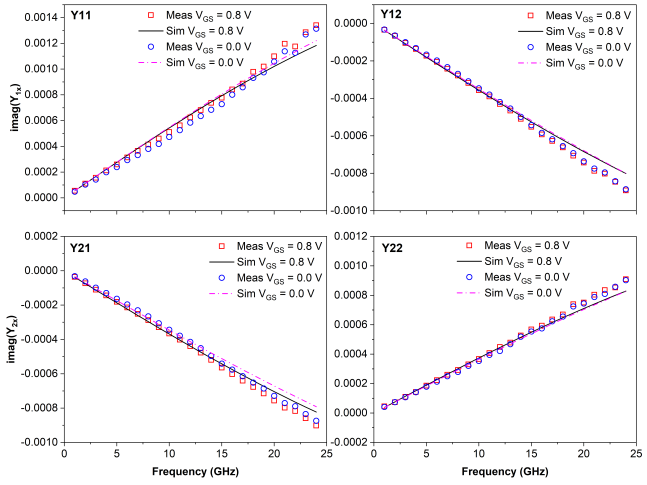
Parameter	P (V_{GS} = 0.0 V)	N (V_{GS} = 0.8 V)
R_S (Ω)	801	965
R_D (Ω)	300	347
c_{gs} (fF)	3.27	3.13
c_{gd} (fF)	5.60	5.75
c_{ds} (fF)	0.36	0.36
g_m (μS)	-16	38.5
r_{ds} (Ω)	50000	127000

The simulated Y-parameters from the SSEC were compared with the measured values and the results are illustrated in Fig. 7. An evaluation of the accuracy of the obtained equivalent circuit was performed by applying an error-check function defined through the equation (8).

$$\varepsilon_{\text{tot}(Y)} = 100 * \frac{1}{4} \sum_{ij} \left\{ \sum_{\text{freq}} \frac{|\text{meas}\,(Y_{ij}) - \text{sim}\,(Y_{ij})|^2}{|\text{meas}\,(Y_{ij})|^2} \right\} \frac{1}{N_{\text{freq}}} \tag{8}$$



(a)



(b)

Fig. 7. Real (a) and Imaginary (b) part of the Y parameters from measurement and simulation at V_{GS} = 0.0 V and 0.8 V (V_{DS} = 0.8 V).

The errors between measured and simulated Y parameters for a BB-RFET polarized with V_{GS} 0.0 V and V_{GS} 0.8 V are 0.80 % and 0.51 %, respectively. The results validate the use of a conventional SSEC for the ambipolar BB-RFET, justifying the overshadowed value of the gate resistance.

V. Conclusion

In this work, direct extraction of the small signal equivalent circuit parameters of an ambipolar 20 nm BB-RFET has been demonstrated for the first time. The extraction and validation of the SSEC was performed up to 24 GHz. These results can be further used for the validation of compact models that can be subsequently incorporated into commercial simulators, making the technology available to circuit designers.

VI. Acknowledgment

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