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***Abstract*—In this paper, we present the fabrication, characterization, and electromagnetic simulation of open pad test structures on silicon-on-insulator substrates, with an emphasis on the impact of the substrate properties on RF performance. Targeting the design of optimal RF test structures for emerging technologies, we demonstrated that a high-resistivity substrate is essential to minimize losses and parasitic capacitances in RF measurements for technologies using silicon-on-insulator wafers.**

I. Introduction

In the era of advanced neural networks permeating daily life [1], compute-in-memory is emerging as a solution to the memory access bottlenecks inherent in traditional architectures [2]. This paradigm shift towards novel architectures has prompted a reevaluation of the fundamental blocks that constitute these systems [3]. In this context, emerging devices such as the reconfigurable field effect transistors (RFETs) have shown promising potential as a future contender for the basic circuit building block development [4].

Academic research environments often serve as testing grounds for emerging device concepts, using technologies such as silicon-on-insulator (SOI) wafers to showcase innovations like RFETs and junctionless transistors [5], [6]. However, unlike industrial processes, academic level fabrication lacks the complete back end-of-line process. As a result, metal contact pads for electrical test structures are often placed directly on top of the buried oxide (BOX). For DC measurements, the BOX functions as a good insulator between adjacent devices and enables the use of the substrate as a back gate [7]. However, for analog design or even RF measurements, the substrate can lead to significant losses.

In this study, we will examine how these constraints may impact the RF performance of open test-structures utilised for de-embedding. Getting access to both extrinsic and intrinsic elements of the device, including resistances, inductances and capacitances of the small-signal equivalent circuit associated with these emerging technologies, can be quite challenging if the devices are fabricated through a non-optimised process.

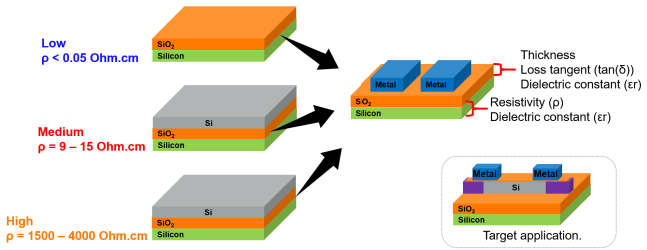


Fig. 1. Wafers having different levels of substrate resistivity used for the fabrication of the open pad structures (left) and a schematic drawing of the test structure (top right) including the necessary material properties to be defined for the EM simulations on ADS. On the bottom right a schematic of an RFET as a target application is shown [5].

To explore the frequency response of these emerging devices fabricated on SOI wafers, it is therefore necessary to first determine the structures that one requires to fabricate, in order to enable electrical contacts, such as pads and metal lines. In this context, electro-magnetic (EM) simulations can be explored as a tool to understand the effects of different wafer substrates and thus to provide predictive results on the operation of the high frequency dummies required to de-embed active devices [8], [9], [10].

II. Methodology

In this work, open pad structures were fabricated on different SOI substrate resistivity and the S-parameters were measured up to 24 GHz using $|Z|-$Probe® RF probes with 100 µm pitch. The measurement data was then used as calibration inputs for the EM simulation (see Figure1). Finally, an equivalent circuit is proposed for the wafers that are most suitable and optimised for the fabrication of active devices.

A. Test Structure Fabrication

The fabrication steps for the RF pad structures are presented in Figure 2. The medium resistivity wafer corresponds to a SOI wafer with a 100 nm BOX and a substrate resistivity

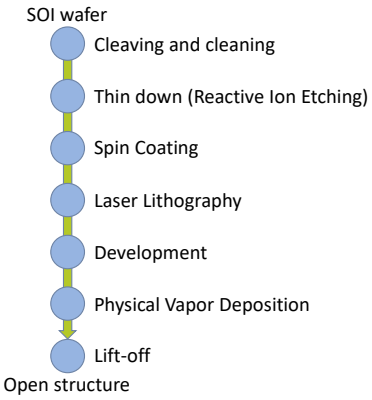


Fig. 2. Fabrication steps of an open pad structure. The thin-down step is skipped for the low resistivity wafer.

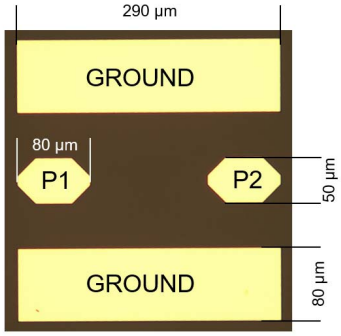


Fig. 3. Optical image of the fabricated open pad structure. The symmetry implies that $S_{11} = S_{22}$ and $S_{12} = S_{21}$.

between 9-18 Ohm·cm. The low resistivity wafer presents a 100 nm SiO_2 on top of the Si with a resistance lower than 0.05 Ohm·cm. For the high resistivity wafer, a 1000 nm BOX with a substrate resistance between 1500-4000 Ohm·cm was chosen. All the wafers used in this study are commercially available. To grow the structures directly on top of the BOX for the standard and high resistivity wafers, the silicon on top is first removed using reactive ion etching. The design of the open structure is transferred using laser direct write lithography using a positive resist.

After the exposure, the resist is developed, and a metal layer is deposited using ion beam sputtering. The metal layer consists of 90 nm of Ni and 10 nm of Pt. A lift-off process is the last step followed where the undesired metal areas are removed together with the underlying resist, leaving the designed structures on top of the SiO_2. The final structure with its associated dimensions can be seen in Figure 3.

B. Test Structure Electromagnetic Simulation

The EM simulations were performed using the Momentum simulator from PathWave Advanced Design System (ADS). The layout of the open pad was first imported into ADS using the same GDSII file that was used for the fabrication steps.

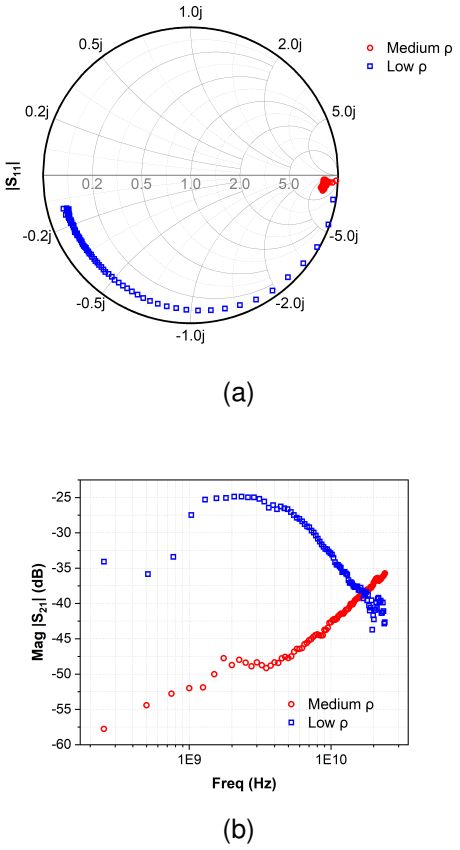


Fig. 4. Measured S-parameters for the medium (red circle symbol) and the low (blue square symbol) resistivity wafers with 100 nm SiO_2 layer. (a) Reflection coefficients S_{11}. (b) Magnitude of the transmission parameter S_{21}.

The electrical properties of the substrates were then specified based on the data-sheet of the selected wafer.

III. Results

A. Electrical Characterization versus EM Simulation of the Open Pad Test Structure

The measured reflection coefficient of the open pad on the medium-resistivity SOI wafer, shown in Figure 4a, indicates a coupling between the ports resulting in a deviation from the purely capacitive behaviour, due to the poor isolation provided by the substrate. The low resistivity wafer yields a high capacitance due to the thin BOX. Figure 4b displays a significant reduction in cross-talk from the low to the medium resistivity substrate, even though further improvement can still be achieved [11].

Figures 5 depict results obtained from the EM simulations with similar characteristics as the measured ones. Based on the EM simulation outcomes, the high resistivity wafer was deemed a reasonable solution for minimising possible cross talk at frequencies below 10 GHz and achieving small pad capacitances.

The results obtained from the high resistivity wafer are presented in Figure 6. At 1 GHz, the high resistivity wafer recorded a 12-dB reduction in cross-talk compared to the

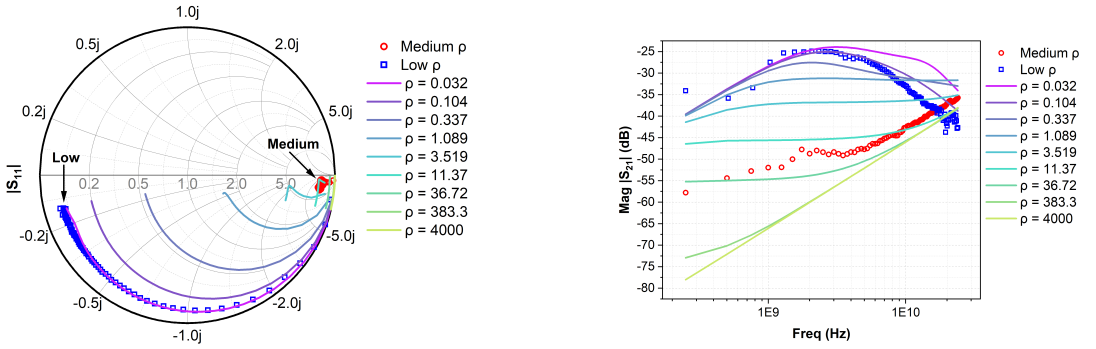


Fig. 5. S-parameters from measurements (symbols) and simulations (lines) for different resistivities ρ (Ohm·cm) with a 100 nm BOX. (a) Reflection coefficients S_{11}. (b) Magnitude of the transmission parameter S_{21}. EM simulation with a ρ of around 0.032-0.104 Ohm·cm captures the behaviour of the low resistivity wafer quite well, similar results were obtained for a ρ = 11.37-36.72 for the medium resistivity wafer.

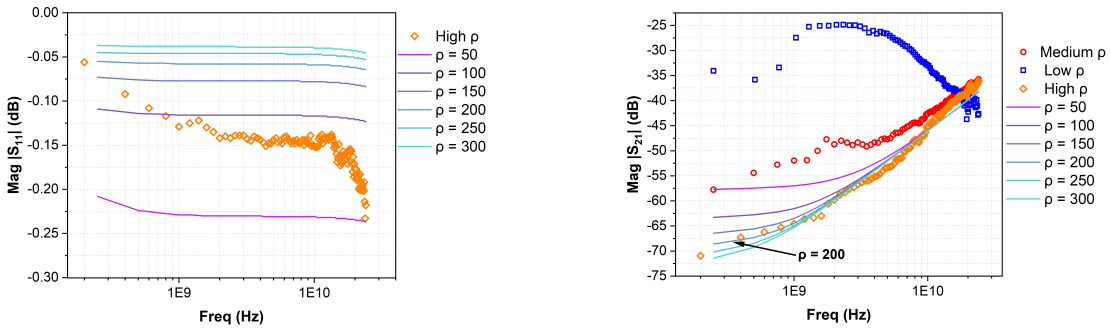


Fig. 6. S-parameters from measurements (symbols) and simulations (lines) for different resistivities ρ (Ohm·cm): (a) Magnitude of the reflection coefficients S_{11} and (b) Magnitude of the transmission coefficients S_{21}, for the high resistivity SOI wafer with a 1000 nm BOX. EM simulation results for different resistivity values obtained for a 1000 nm BOX are also compared with the results from the measured low and medium resistivity wafers with 100 nm BOX. EM simulation for the resistivity of approximately 200 Ohm·cm captures the behaviour of the high-resistivity wafer correctly.

medium-resistivity one. The measurements on the high resistivity substrate demonstrate that the expected values obtained from the EM simulation are distinctly different from that of the experimental observations, due to the presence of parasitic surface conduction at the interface of the BOX and the substrate. It has been previously demonstrated that the effective substrate resistivity at the interface is in fact lower than the one that is obtained deep within the substrate [11]. It can be observed that the measurements from the high resistivity substrate are comparable with the electromagnetic (EM) simulation results when the resistance of the substrate is approximately 200 Ohm·cm (see Figure 6b). This value is one order of magnitude lower than the intrinsic value of 1500-4000 Ohm·cm specified in the wafer data-sheet. Hence, as an additional outcome, the EM simulation can also be utilised to determine the equivalent resistivity of the substrate.

B. Equivalent Circuit of the Open Pad

An equivalent circuit and its extraction from measurements is proposed for the open structures on the medium and high resistivity wafers and is presented in Figure 7. The circuit is based on the standard π network of an open circuit consisting of three impedances Z_i, Z_t and Z_o. For the entire analyses $Z_i = Z_0$ is considered, due to the symmetry of the structure.

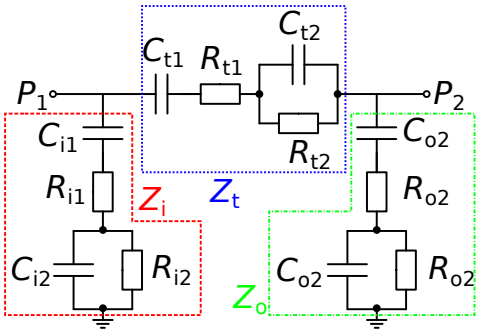


Fig. 7. Proposed equivalent circuit for the open pad structure.

Non idealities of the substrate, such as the effects of the

TABLE I
VALUES OF THE PARAMETERS UTILISED FOR THE SIMULATION OF THE EQUIVALENT CIRCUIT.

Parameters	High	Medium	Parameters	High	Medium
C_{i1}	56.5 fF	210 fF	C_{t1}	2.1 fF	7.7 fF
R_{i1}	5 Ω	5 Ω	R_{t1}	600 Ω	3k Ω
C_{i2}	6.1 fF	5.3 fF	C_{t2}	1 fF	1.8 fF
R_{i2}	4895 Ω	1 kΩ	R_{t2}	13.2 kΩ	32 kΩ

BOX, are included in the equivalent circuit, represented by a capacitor with a series resistance (C_{i1} and R_{i1}) and the substrate is represented by a resistance in parallel to a capacitor (R_{i2} and C_{i2}). The capacitance C_{i1} is first roughly estimated at low frequencies from the converted measurements using (1). From the same equation, C_{i2} is obtained, however at medium frequencies, where its value becomes frequency independent. The resistance R_{i2} is estimated from the highest point of (2) over frequency while R_{i1} is expected to have a small value that can just be determined directly at very high frequencies. C_{t1} and C_{t2} are obtained from (3) using the same methodology as C_{i1} and C_{i2} while the resistances R_{t2} and R_{t1} are determined from (4) when its value is maximum and from its value at high frequencies, respectively. With these estimated values the equivalent circuit is then simulated using ADS.

$$C_i = imag(Y_{11} + Y_{21})/\omega \tag{1}$$

$$R_i = real((Y_{11} + Y_{21})^{-1}) \tag{2}$$

$$C_t = imag(-Y_{21})/\omega \tag{3}$$

$$R_t = real((-Y_{21})^{-1}) \tag{4}$$

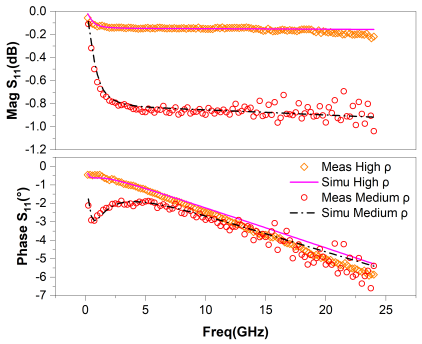
The Table I presents the extracted values of the capacitances and resistances, optimised from the equivalent circuit simulation through fitting.

The S parameters from the simulation of the final equivalent circuit and the measurements are compared in Figure 8, showcasing a good agreement between the simulation and measurement, and equation 5 was used to quantify the model accuracy. An error of 1.5 % was obtained for the medium ρ wafer while a 3.86 % error was observed for the high ρ wafer.

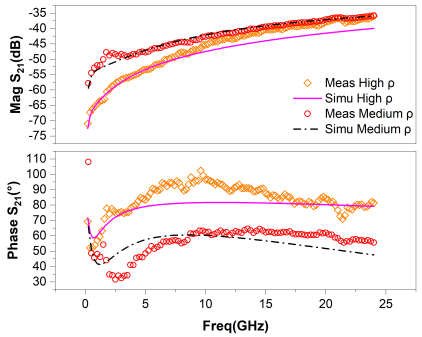
$$\varepsilon_{\text{tot}(S)} = 100 * \frac{1}{4} \sum_{ij} \left\{ \sum_{\text{freq}} \frac{|\text{meas}\,(S_{ij}) - \text{sim}\,(S_{ij})|^2}{|\text{meas}\,(S_{ij})|^2} \right\} \frac{1}{N_{\text{freq}}} \tag{5}$$

IV. CONCLUSION

In conclusion, we demonstrated the strength of EM simulations as a tool to understand the impact of the resistivity of SOI wafers followed by a methodology for the equivalent circuit extraction. Our results indicate that the layout of other dummy structures can also be optimized through predictive EM simulations before new fabrication runs are performed.



(a)



(b)

Fig. 8. S-parameters from measurements (symbols) and equivalent circuit simulations (solid and dash-dot lines) for different resistivity values ρ (Ohm·cm). (a) Magnitude and phase of the reflection coefficients S_{11}. (b) Magnitude and phase of the transmission coefficient S_{21}.

Moreover, a high resistivity wafer can offer improvements of the RF characteristics, necessary for the modelling of emerging devices fabricated on non-optimized technology platforms with constraints imposed by a single metallization layer.

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