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Abstract

Addressing temperature hot-spots resulting from self-heating effects (SHE) poses a significant challenge in the design of emerging nanoscale transistors, such as vertical junctionless nanowire field-effect transistors (VNWFETs), due to reduced thermal conductivity. Consequently, electrothermal modeling becomes crucial for a comprehensive understanding of the underlying physical mechanisms governing carrier degradation and thermal conduction in these nanoscale devices. In this study, we present an enhanced drift-diffusion model coupled with nonlocal Guyer-Krumhansl (GK) equations to accurately capture carrier-phonon interactions and explore the electrothermal characteristics of gate-all-around (GAA) VNWFETs. Pulsed current-voltage (I–V) measurements are employed to investigate the performance of a state-of-the-art 18nm VNWFET technology. Furthermore, we report on the influences of both trapping and SHE under high-bias conditions for varying pulse widths. Our findings reveal that optimization of mobility degradation mechanisms allows for improved control over the physical behavior of carrier transport in these emerging technologies. Through careful consideration of these factors, it becomes possible to enhance the overall performance of GAA VNWFETs, particularly in mitigating temperature hot-spots and addressing challenges associated with self-heating effects.

KEYWORDS: Nanowire field effect transistors; electrothermal modeling; pulsed current-voltage measurements; phonon-carrier interaction.

1. Introduction

The investigation of nanoscale electrothermal transport is regarded as a challenging task for modern semiconductor manufacturing processes [1-3]. Nanoelectronic devices offer potential benefits for the development of the new generation of complementary metal-oxide-semiconductor (CMOS) technologies [4]. The conventional planar MOS field-effect transistors (MOSFET) are no longer capable of being further scaled down owing to physical limitations

associated with its geometries. In addition, the physical performances of highly-scaled CMOS devices are limited by carrier degradation [5] and thermal instability [6]. Recently, vertical junctionless nanowire field effect transistors (VNWFETs) are being considered as a suitable solution for emerging nanoelectronics [7-10]. Moreover, VNWFETs can ensure a high energy current conservation that might provide promising advantages for device scaling and future transistors generations. In order to implement the gate-all-around (GAA) architecture, VNWFETs are fabricated based on silicon nanowires using a top-down approach with plasma etching [7]. In general, this technique ensures better carrier flow owing to specular surface scattering and small roughness. At the same time, scalable manufacturing methods and device miniaturization (following the trends of Moore's law) can lead to concerns related to electrostatic control, thermal management and power dissipation. Recently, nanowire FETs have been recommended by the electronic device community to satisfy future scaling trends [11].

Several approaches have been considered previously to investigate thermal management in electronic devices [12] and semiconductor materials [13]. However, additional thermal constraints are pronounced as the dimensions of the transistors are scaled down to 18 nm and bellow [9]. New electronic materials are therefore introduced within modern transistor architectures in order to satisfy both cooling strategies and high performances [1, 2]. The heat propagation in nanoscale transistors is non-uniform with localized temperatures (i.e., temperature hot-spots) higher than the device temperature [14]. Multiple temperature hot-spots make heat propagation quite complicated, which may exacerbate heat accumulation, known as the self-heating effect. Recent experimental studies of heat transport in semiconductor materials have shown that classical Fourier law fails with ultrafast nanoscale carrier transport [15]. Therefore, new theoretical approaches are being evaluated to explain non-equilibrium thermodynamics in modern semiconductor materials. In this context, the kinetic-collective

model (KCM) is an efficient framework capable of describing nanoscale thermal transport based on Boltzmann transport equation (BTE) without any fitting parameters [16]. The KCM focuses on the calculation of thermal conductivity using ab initio scattering rates from first principle calculations. According to the KCM, heat carriers (i.e., phonons) propagate through both (1) the collective mode due to the conservation of energy and momentum (hydrodynamic effect) and (2) the kinetic mechanism where the momentum is destroyed by resistive processes including boundary scattering [17,18]. Although, semiconductor heat transport is generally affected by phonon distribution, the charge carrier transport (electrons and holes) should also be addressed in the description of electrothermal effects.

As a fundamental concept in electrothermal transport, phonon-electron interaction is essential to control and manipulate energy in phononic and electronic devices [19-21]. In highly doped semiconductors with carrier concentrations ranging from 10^{19} to 10^{21} cm^{-3}, phonon-carrier coupling has a significant impact on energy transport in low-dimensional materials [19]. In condensed matter physics, a phonon-electron interaction is the main scattering event that influences the mobility and thermal conductivity in bulk materials. Due to higher concentrations, carriers cannot interact through the shortest possible length which then results into confinement effects [12]. Phonon confinement is indeed one of the current challenges in emerging CMOS devices. Between the oxide layer and semiconductor, the thermal boundary resistance degrades the heat flow leading to heat accumulation in the ultrathin nanowire [22-24]. Similarly, charge carriers are trapped at the interface where scattering mechanisms (e.g., phonon-boundary scattering) can dramatically modify the transport phenomena [25-27]. Therefore, the open question is how to simulate the electrothermal behavior of phonon and charge carrier transport correctly. In low dimensional materials, phonon-hole and phonon-electron interactions are addressed with ab-initio calculations of the phonon energy transport using the density-functional theory (DFT) [28]. However, DFT methods, such as discrete

ordinates method (DOM) [29], ShengBTE [30] and non-equilibrium Green's function [27] are only valid at atomic scale within a window of few nanometers. In general, these methods are computationally expensive and suitable only for simple geometries. It is well known that the macroscopic heat equation given by Fourier's law is no longer appropriate for describing ultrafast carrier dynamics. It is therefore recommended to develop mesoscopic methods to bridge the gap between macroscopic and atomic scales.

In this work, we report on the nanoscale electrothermal transport in an 18nm gate-all-around (GAA) VNWFET technology based on a coupled non-Fourier heat transfer formulation combined with an enhanced drift-diffusion model. The paper is organized as follow as: The finite element solver for electrothermal modeling including the nonlocal GKE and the enhanced DD model is presented in Sec. II. In addition, we introduce the experimental measurements on VNWFETs including pulsed current-voltage ($I-V$) characteristics in Sec. III. In Sec. IV, we validate our proposed framework by comparing the extracted thermal conductivity against theoretical and experimental data. Furthermore, we discuss the electrothermal transport in the VNWFETs under test with a focus on the physical origin of carrier trapping and phonon quantum confinement. Finally, conclusions and remarks are provided in Sec. V.

2. Computational Model

2.1. Nonlocal Guyer-Krumhansl (GK) equation: Phonon transport at nanoscale

Many of the previous works on this topic focus on phonon hydrodynamics considering that both normal (N) and resistive (R) scattering processes have a strong contribution to the physical origin of the heat transport in nanoscale devices [10,15,17,18]. In semiconductors, energy carriers are usually represented by the nature of its phonon flow. Guyer and Krumhansl proposed a solution (GKE) to the linearized BTE to predict the multiscale phonon transport. Under the relaxation time approximation, the Boltzmann transport equation (BTE) can usually be employed to treat phonon transport [15,29,31,32],

$$\frac{\partial f(r,v,t)}{\partial t} + v\nabla f(r,v,t) = \left(\frac{\delta f}{\delta t}\right)_{collision} \quad (1)$$

$$\left(\frac{\delta f}{\delta t}\right)_{collision} = -\frac{f-f_0}{\tau_R}$$

where τ_R is the relaxation time related to resistive collisions, r is the position vector, v is the group velocity, t is the time scale and f^0 is the equilibrium distribution function given by the Planck distribution [32],

$$f^0 = \frac{1}{\exp\left(\frac{\hbar w}{k_B T}\right)-1} \quad (2)$$

In which k_B is the Boltzmann constant, T is the temperature, $\hbar w$ is the phonon energy quanta where $\hbar$ is the reduced Planck constant and w is the frequency obtained from Debye's expression of the dispersion relation, $w = vk$, with k being the wave vector. The heat flux vector is then expressed as [31]

$$q(r,t) = \int_{\varepsilon} v(r,t) f\,(r,\varepsilon,t)\varepsilon D(\varepsilon) d\varepsilon \quad (3)$$

where ε is the kinetic energy and $D(\varepsilon)$is the density of states. To describe the phonon dynamics in low dimensional materials, the Callaway model is commonly used for modeling non-Fourier heat transport [15,32]. In recent studies, the GKE was developed based on a macroscopic hydrodynamic equation for nanoscale heat transport at ambient temperature. The GKE is thus expressed as [10,18]

$$q + \tau_R \frac{\partial q}{\partial t} = -\kappa\nabla T + l^2(2\nabla\nabla.q + \Delta q) \quad (4)$$

$$c\frac{dT}{dt} + \nabla.q = P \quad (5)$$

where q is the heat flux, τ_R is the phonon relaxation time, κ is the bulk thermal conductivity, ℓ is the nonlocal phonon mean free path (MFP) and c is the heat capacity. In general, the nonlocality of the heat flux gradient originates due to the phonon-boundary scattering and

confinement effects. Nanoscale thermal transport is usually characterized by the phonon mean free path. Based on the average MFP, ℓ, phonon transport can be classified into three regimes: ballistic regime (external boundary scattering), quasiballistic regime and bulk-like (diffusive) regime [24]. In sub-50 nm devices, ballistic transport governs the heat flow in Silicon materials, and it is expected that phonon confinement leads to a reduction of the thermal conductivity [33]. On the other hand, the non-equilibrium spatial effects of ultrafast carrier dynamics should also be taken into considerations for a complete description of the kinetic approach. Therefore, a slip boundary condition considering phonon-interface interactions will be discussed in the next section.

2.2. Slip boundary condition: effect of surface roughness

In recent years, a significant amount of research has focused on studying the interfacial heat conduction taking into account the effects of surface roughness and phonon-boundary scattering. The present GKE provides an enhanced formulation which allows us to investigate nanoscale heat transport beyond the classical Fourier's law. However, it is recommended at the same time to implement a suitable boundary condition to investigate the interfacial heat transport in nanomaterials. Thermal conductivity within the nanowire reduces with the dominance of ballistic transport, hence this non-local effect lead to the use of an effective thermal conductivity (ETC) for the nanowire system [18]. In this regard, we have developed an expression for the effective thermal conductivity depending on the surface roughness, the length of the structure and nonlocal effects owing to strong resistive scattering. For steady state phonon transport, $\frac{\partial q(r,t)}{\partial t} = 0$, the GK equation thus becomes

$$q = -\kappa \nabla T + l^2 \Delta q \tag{6}$$

The effective thermal conductivity, κ_{eff}, is then obtained as [10,18]

$$\kappa_{eff} = \frac{\int q(r) d\Gamma}{\frac{S\Delta T}{L}} \quad (7)$$

where ΔT is the temperature difference between the hot and the cold sources, Γ is the cross section, S is the surface area and L is the distance between the source and the drain contacts. For the phonon transport, the Umklapp scattering results in a thermal resistance across the interface region. The impact of thermal boundary resistance is largely manifested due to the heat carriers propagating in a confined space. To study the heat transfer under the influence of interface scattering, we introduce an additional parameter C_W defined as $C_W = \left(\frac{1+p}{1-p}\right)$ where p is the specularity parameter and is defined as [18,33],

$$p = exp\left(-\frac{16\pi^3\eta^2}{\lambda}\right). \quad (8)$$

Here, η is the roughness of the defects and λ is the phonon wavelength [34]. The parameter C_W is a non-dimensional coefficient that is used to describe the magnitude of specular and diffuse reflection at the interface. In the other words, C_W denotes the interaction of phonons that experience either a diffuse scattering (small p) or a specular scattering (large p). The slip boundary condition is therefore obtained from the tangential heat flux near the surface [18]

$$q_t = C_W \ell \nabla q_t . n \quad (9)$$

where n is the surface normal direction.

In order to precisely capture the electrothermal response, the GK equation needs to be carefully adjusted to offer further interpretations for carrier degradation mechanisms. A drift-diffusion (DD) model for electrical transport can be linked to the GK equation, which is mandatory for electrothermal modeling beyond the classical hydrodynamic regime.

2.3. Enhanced drift-diffusion (EDD) model: electrothermal transport

In nanoscale transistors, the drift-diffusion model is commonly used to predict the electron flow in semiconductors materials [5,21,35-37]. Due to progressive downscaling of emerging technologies, the standard DD model needs to be enhanced in order to satisfy the physics of ultrafast carrier transport in low dimensional systems. In order to describe the electrothermal behavior and carrier degradation, electron-phonon coupling is considered in the present framework along with associated boundary conditions. It should be noted that in a realistic scenario, hydrodynamic heat conduction mechanism is combined with pure electrical transport. Consequently, the heat source term is expressed as [37]

$$P = \vec{J}.\vec{E} + (R - G)(E_g + 3k_B T) \tag{10}$$

where $\vec{E}$ is the electrical field, $\vec{J}$ is the current density, $(R - G)$ is the generation-recombination rate and E_g is the energy band gap. Trap assisted recombination is commonly described by the Shockley-Read-Hall (SRH) statistics given by the following equation:

$$(R - G) = \frac{np - n_0^2}{\tau_n(n + n_0) + \tau_p(p + p_0)} \tag{11}$$

where n_0 and p_0 are the intrinsic carrier concentrations, τ_n and τ_p are the electron and hole lifetimes. The function $(R - G)$ represents the generation (G) and recombination (R) rates of charge carriers. In particular, both electron and hole can be trapped by impurities, defects and even interface roughness (interface traps). The interface trap charges (ITC) can consequently modify the *I-V* characteristics and eventually result in a strong temperature dependence of the phonon state. In addition, the presence of trapping processes affects the charge density state. In general, the rate of the recombination mechanism depends on the number of free carriers (n and p) and trapped carriers (n_t, p_t). In our proposed enhanced DD model, the densities of the trapped electrons and holes are given as [36]

$$n_t = \frac{N_t}{1+\exp\left(\frac{(E_c - E_{tn}) - E_{F,n}}{k_B T}\right)} \tag{12}$$

$$p_t = \frac{N_t}{1+\exp\left(-\frac{(E_V + E_{tp}) - E_{F,p}}{k_B T}\right)} \tag{13}$$

where E_{tn} and E_{tp} are the electron and hole trap energy levels, N_t represents the density of traps, E_c and E_V denote the conduction and valence band energies, respectively. The Poisson equations are specifically coupled to the DD equations through a trap assisted model. In this case, the electrostatic potential, V, satisfies the Poisson equation:

$$\nabla . (\epsilon \Delta V) = -q(p - n + N_D - N_A + p_t - n_t) \tag{14}$$

where q is the elementary charge, N_D and N_D are donor and acceptor concentrations, respectively. The current continuity and trap rate equations are linked by the following equations

$$\nabla . j_n = \nabla . (\mu_n n \nabla V) = -R + G \tag{15}$$

$$\nabla . j_p = \nabla . \left(\mu_p p \nabla V\right) = R - G \tag{16}$$

where μ_n and μ_p are the electron and hole mobilities. The drift diffusion model and the Poisson equation are then solved together using the semiconductor package in COMSOL Multiphysics simulator based on the finite element method. Fermi-Dirac statistics were considered for defining the source/drain Schottky regions. Due to ballistic transport, the mobility is affected by scattering mechanisms including phonon-electron and phonon-hole interactions. Furthermore, in heavily doped semiconductors, phonon-carrier coupling is experimentally observed at room temperatures. In COMSOL environment, we therefore included the Caughey-Thomas model to describe an effective mobility caused by phonon-carrier interaction effects. The effective mobilities for both carrier types are thus given by [35,38]

$$\mu_{n,eff} = \mu_{n,0} \times \left[1 + \left(\frac{\mu_{n,0} \times E}{v_s}\right)^2\right]^{-0.5} \quad (17)$$

$$\mu_{p,eff} = \mu_{p,0} \times \left[1 + \left(\frac{\mu_{p,0} \times E}{v_s}\right)^2\right]^{-0.5} \quad (18)$$

where v_s is the saturation velocity, $\mu_{n,0}$ and $\mu_{p,0}$ are the low field electron and hole mobilities, respectively. In our simulation framework, the Caughey-Thomas model is adopted along with the Poisson equation to enhance the conventional drift-diffusion model. Then, we carefully adjusted the electrothermal transport by considering both a nonlocal GK equation and the enhanced DD model. Here, the GK equation is established to describe the thermal propagation within the device based on non-Fourier modeling. Moreover, the enhanced DD model is considered for assessing electrical performance. The electrothermal coupling is achieved through a FEM solver for both phonon and electron transport. As shown in Fig. 1, our proposed framework investigates several physical phenomena in emerging nanoscale transistors such as (1) ballistic transport, (2) specular phonon scattering, (3) diffuse phonon scattering, (4) phonon confinement, (4) carrier trapping and (5) phonon-carrier interaction. The finite element method is used for modeling both thermal and electrical transports. Under COMSOL multiphysics [39], a set of partial differential equations (PDEs) is considered to solve the GK formulations under slip boundary conditions. The simulations were performed using a dense mesh resolution with 64420 spatial grid elements (extremely fine mesh of 0.1 nm). As illustrated in Fig. 2, the GK-DD framework is a new feature that provides a complete solution to predict the ultrafast carrier dynamics in sub 20 nm silicon nanowires. The materials properties used for our simulations are presented in Table I. The carrier mobilities and saturation velocities are obtained from the material library in COMSOL multiphysics.

3. Pulsed I–V measurements

Sub-20nm devices, such as VNWFET transistors are susceptible to electro-thermal effects due to highly miniaturized device dimensions. Through pulse (I-V) measurements, we can measure DC-like I-V curves and were able to isolate the effect of internal device temperature variations on the device. As mentioned in the manuscript, the very short gate pulses, (here we used pulse widths from 10µs to 10ms with a duty cycle of 10%) are used to ensure quasi-isothermal conditions, to minimize internal temperature changes due to applied bias and to not allow sufficient time to activate the Si-SiO_2 charge trapping. With conventional DC tests, these effects cannot be separated from the pure electrical characteristics of the device. In addition, 10% duty cycle facilitates device recovery to a quiescent state before starting the next measurement. Consequently, pulsed I-V measurement is suitable for investigating both self-heating and the trapping effects.

The devices studied in this work, fabricated by LAAS-CNRS [7], consist of multiple parallel vertical silicon nanowires arranged on a silicon substrate (Fig. 3) to build a 3D transistor. The parallel nanowires share a common gate-all-around structure consisting of a 5 nm oxide, a gate metal of chromium (Cr) and aluminum used for the top metal contact. The platinum silicide (PtSi) layers form top and bottom Schottky contacts with the silicon at both source and drain ends with reasonable Schottky barrier height to allow sufficient current. The drive current is further boosted through the use of multiple nanowires in parallel. The silicon nanowires are highly doped to ensure a junctionless transition between the channel and the nanowire access regions. Moreover, the choice of the gate metal work function with the p-doped Si and the nanowire diameter allows for fully depleted nanowire channels under off conditions with very low subthreshold leakage ensuring an on/off current ratio of 10^6. Fig. 3(a) schematically illustrates the architecture of the state-of-the-art 18 nm VNWFET with GAA structure which is expected to improve its thermal transport. $PtSi$ contacts are considered to ensure a weak contact

resistance and a low Schottky barrier height in the heavily p-doped devices [7]. A detailed TEM cross-sectional view of the device is shown in Fig. 3(b). Junctionless transistors such as VNWFETs are particularly required to be highly doped and the diameter of the nanowires are needed to be small enough (22 and 34 nm) to ensure better electrostatic control and a junctionless operation. Pulsed current-voltage ($I-V$) measurements are an effective mean to investigate the electrothermal transport in nanoscale transistors [1,40]. In this work, we used pulsed $I-V$ measurements from the vertical nanowire transistor technology to investigate the dynamics of heat flow and its physical interpretations. For the measurements, we considered several different pulse widths at high voltage biases. The principle of pulsed $I-V$ characteristics is centered around the application of a short gate pulse on the transistor terminals without leaving sufficient time for its internal temperature to change. As shown in Fig. 3(c), the pulse width used in our setup is varied between 1µs and 10ms with a small duty cycle of 10 % to ensure that the channel temperature does not change significantly [40].

4. Results and discussion

4.1. Model validation

In this section, the modeling framework consisting of the GK equation and the enhanced DD model is validated against both experimental and theoretical (KCM and BTE) results. Fig. 4(a) plots the thermal conductivity of a silicon nanowire at $T = 300K$. The GK equation demonstrates a good agreement with KCM [16], BTE [41] and experimental data [42,43]. The strong reduction of the thermal conductivity is observed below 100 nm. In sub-100 nm regime, ballistic transport (carrier flow having large MFP) dominates leading to ultrafast heat conduction. Consequently, ballistic phonons in the ultrathin nanowire are likely to experience a significant boundary scattering sensitive to the surface roughness. For $C_W = 2$, the thermal conductivity increases since the phonons experience specular scattering at the surface. For rough surfaces, $C_W = 1$, and the phonon-boundary scattering causes a confinement effect which

reduces the thermal conductivity [44-46]. Fig. 4(b) plots the normalized thermal conductivity across the silicon nanowire. The nonequilibrium boundary conditions given by equation (9) ensures the accuracy of the thermal transport model. The tangential heat flux boundary condition is mandatory for modeling nonequilibrium distribution due to phonon jumps near the adiabatic surface. The classical hydrodynamic equation is limited to large scale devices where nonlocal effects are negligibly small, whereas the present nonlocal GKE accurately describes the thermal transport particularly in ultra-thin nanowire. Next, we validated the model against experimental $(I-V)$ characteristics of the VNWFETs by comparing simulations results obtained using the enhanced drift-diffusion model with the measurement data. Fig. 5 shows the $(I-V)$ output characteristics of the device for different pulse widths. As is evident from Fig. 5(a), (b), (c), (d), (c) and (e), the EDD predictions match well with the measurement data. Under all pulsed conditions and at high gate voltages, an increase of the drain current is observed along with the absence of saturation. The trap density, N_t, increases with the pulse width as shown in Table II. This can be explained by the following: The carrier trapping phenomena is very weak at $V_g = \frac{V_d}{2}$. However, at high bias conditions, the maximum electrical field occurs at the drain end of the channel which results an aggressive hot carrier degradation [25]. Along the channel, carriers experience several scattering processes (defect, boundary and impurity) and gradually lose momentum upon reaching the drain region. The carrier trapping is generally dominant in the oxide and is expected to saturate at large pulse widths ($t_w = 500\ \mu s$). A few of these carriers might escape collision ('lucky carrier), however it is possible that they can interact with the phonons and therefore their mobility is reduced [47]. The phonon-carrier scattering is a major known effect responsible for carrier energy degradation and a loss of momentum. In the next section, we will focus on the role of phonons on electrothermal transport in emerging nanowires transistors.

4.2. Nanoscale electrothermal transport in 18nm vertical GAA VNWFET

To investigate the impact of phonon-carrier interactions, the GK-EDD framework is considered to predict the electrothermal response of the VNWFET devices. Fig. 6 plots the simulated $I_D - V_{DS}$ characteristics of the VNWFET devices (25NWs and $D = 22\,nm$) at high bias $V_{GS} = -2.2V$ for different surface roughness. For both $C_W = 1$ (diffusive boundary scattering) and $C_W = 2$, the I_D is not much impacted by the phonon-boundary scattering. The ultra-thin silicon nanowire restricts the carriers leading them to be trapped in the oxide. In conventional CMOS devices, the drain current is significantly affected by the reduction of the mobility owing to the phonon-scattering mechanism. Interestingly, the mobility of the VNWFET is not influenced by the increase of the temperature as shown in Fig. 7(a). When the temperature increases from $300\,K$ to $500\,K$, the VNWFET shows only a $2.6\,\%$ reduction of mobility, contrary to conventional CMOS devices that show a significant degradation of $36\,\%$ [8]. To explain the observations in Fig. 7(a), the loss of mobility is not directly linked to the phonon dynamics, rather it can be a result of the defect generation. At the nanoscale regime, strong phonon-phonon scattering could lead to a nonlocal effect (thermodynamic non-equilibrium effects [32]) that generates defects at the surface. In the heavily doped nanowires, the generation of defects may lead to carrier trapping. Fig. 7(b) shows the effective mobility of VNWFETs for different NWs and diameters. As the diameter of the nanowire increases, an enhancement of the mobility is clearly observed. This is because the carriers experience less collisions due to a lower defect generation and thus gain an additional amount of momentum.

The understanding of phonon-carrier interactions in emerging nanoelectronics is crucial for scalable manufacturing in order to achieve an optimum performance. It is well known that the scaling of ultra-scaled CMOS devices are limited by carrier scattering due to surface roughness [20]. For deeply scaled nanowires, heat carriers lose their momentum due to the surface-phonon scattering due to surface roughness which leads to significant heat confinement. In addition, it

is expected that the surface damage from the etching step during fabrication could give rise to diffuse phonon scattering. Therefore, the nature of the surface roughness might directly influence the heat transport. Fig. 8(a) depicts the temperature distribution within the silicon nanowire at high bias $V_{DS} = V_{GS} = -2.2V$ for $D = 22\,nm$ with 25 NWs in parallel. The temperature reaches the maximum near the drain end of the VNWFET. It is clear that phonon-surface scattering has a strong impact on its temperature variation. A smooth surface ($C_W = 2$) helps to enhance the thermal transport in the device. However, a rough surface causes severe perturbation in the carrier transport that might lead to quantum confinements (QC) effects resulting an increase of the temperature. In addition, the heat conduction is mainly dependent on the degradation of the thermal conductivity. Indeed, the effective thermal conductivity increases from 5.2 $Wm^{-1}\,K^{-1}$ to 11.5 $Wm^{-1}\,K^{-1}$ for $C_W = 1$ and $C_W = 2$, respectively (Fig. 8(b)). An increase of 4.2% of the thermal conductivity can be regarded as a significant improvement in the thermal performance. In general, thermal conductivities of nanoscale FETs (e.g., FinFETs and FDSOI) are quite weak due to both defect-induced surface roughness and QC effects [48]. To further investigate the heat propagation in the device, we carried out 3D thermal transport in the VNWFET for $D = 22\,nm$ with 16 NWs in parallel. Fig. 9 shows the temperature evolution in the VNWFET device for both $C_W = 2$ (Fig. 9(a)) and $C_W = 1$ (Fig. 9(b)). Here, we considered a finer mesh resolution to achieve better accuracy. It is clear that the heat is accumulated in the drain region as expected. During heat propagation along the nanowire, phonons might be scattered by carriers and the boundary effects (the surface roughness). Therefore, the nature of the surface roughness might directly influence the phonon flow. At extremely small device dimension and considering ultrafast thermal transport (ballistic regime), quantum confinement effects become non-negligible since resistive scattering dominates at higher temperatures. The reduction of the thermal conductivity and phonon confinement manifest as temperature hot-spots. From a qualitative point of view, smoother interfaces provide

better thermal control and optimized thermal conduction in the device. To avoid heat accumulation, it is recommended to increase the thermal conductivity, and therefore reduce the impact of resistive transport caused by phonon QC effects.

5. Conclusion

In summary, we investigated electro-thermal effects in GAA VNWFET using multiphysics simulations and pulsed (*I*-*V*) measurements. We present a new finite element method-based modeling framework aimed to describe phonon and carrier transport in complex 3D geometries of an emerging nanoelectronic technology. In addition, we have introduced a non-Fourier ultrafast thermal transport for hydrodynamic heat equations. In order to precisely analyze the electrothermal characteristic, we couple the thermal transport equations with an enhanced drift-diffusion model to predict the mechanism of degradation and the charge trapping phenomena. Our results demonstrate that the electrical performances of the VNWFET devices are not affected by phonon scattering and surface roughness. However, due to phonon confinement effects, we observe a heat accumulation near the drain region at high bias conditions. High number of nanowires and larger diameters help reduce the phonon-boundary scattering rate. Both phonon-boundary scattering and back-scattering mechanisms lead to a significantly resistive phonon transport, which causes the 'confinement effect' [10]. On the other hand, larger diameters in junctionless transistors imply a loss of gate control. To avoid this issue, it is therefore an optimum choice to increase the number of nanowires because it could mean a more efficient heat dissipation due to an increased effective thermal conductivity in a higher number of parallel nanowires, leading to an enhanced thermal transport. Thus through the choice of optimum design criteria, VNWFET devices are capable of offering an excellent thermal performance enabling a better carrier energy transport under high-temperature conditions.

Both charge trapping and phonon confinement effects contribute to thermal degradation because of a significant reduction in the thermal conductivity. The miniaturization of CMOS

technologies results in the reduction of carrier mobility, thermal conductivity and drain current. The physical mechanism of degradation directly impacts the device performance as the carriers encounter scattering mechanism. For instance, smother surfaces provide a specular transmission and reflection which ensure better immunity to carrier confinement and trapping.

Data availability statement:

All data that support the findings of this study are available upon reasonable request from the authors.

Acknowledgments

This work was supported by the project FVLLMONTI funded by European Union's Horizon 2020 research and innovation program under grant agreement N^0 101016776.

Credit author statement

Houssem Rezgui: Format analysis**,** Writing-Original Draft**,** Methodology**,** Software **Yifan Wang:** Interpretation of data, Analysis, Visualization **Chhandak Mukherjee**: Methodology, analysis, Investigation, Writing-Review & Editing **Marina Deng**: Investigation, Writing-Review & Editing **Cristell Maneux**: Funding acquisition, Validation, Writing-Review & Editing.

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Table I: Physical parameters of the finite element simulations.

Parameters	**Values**
Gate length	18 nm
Gate work function	4.65 eV
κ_{bulk} (Si) [17]	150 $Wm^{-1} K^{-1}$
κ_{bulk} (Cr) [17]	111 $Wm^{-1} K^{-1}$
κ_{bulk} (SiO_2) [31]	1.4 $Wm^{-1} K^{-1}$
ℓ (Si) [17]	185 nm

Table II: The evolution of trap density with pulse widths

Pulse width	**Trap density (m^{-2})**
$t_w = 1\ \mu s$	1×10^{15}
$t_w = 100\ \mu s$	3×10^{15}
$t_w = 500\ \mu s$	4.3×10^{15}
$t_w = 1\ \mathrm{m}s$	4.35×10^{15}
$t_w = 10\ \mathrm{m}s$	4.4×10^{15}

Figures:

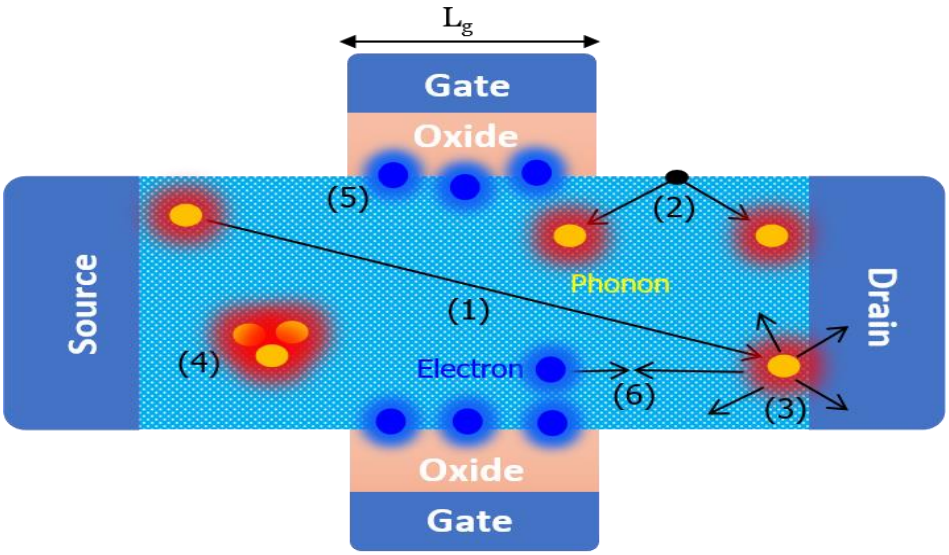


Fig. 1. Schematic representation of carrier transport along the channel length.

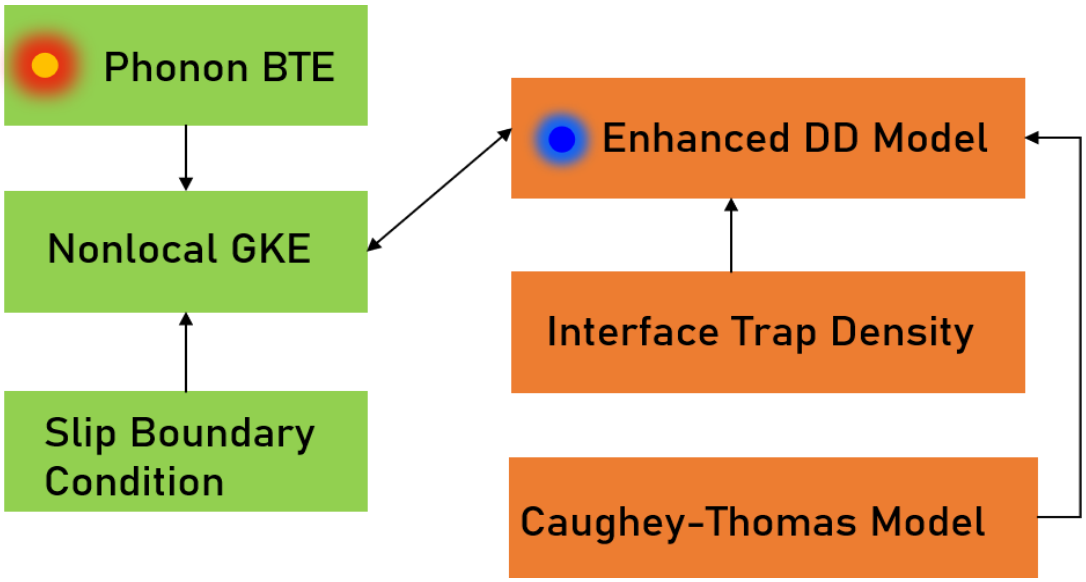


Fig. 2. Principle formalism of the finite element solver for electrothermal transport.

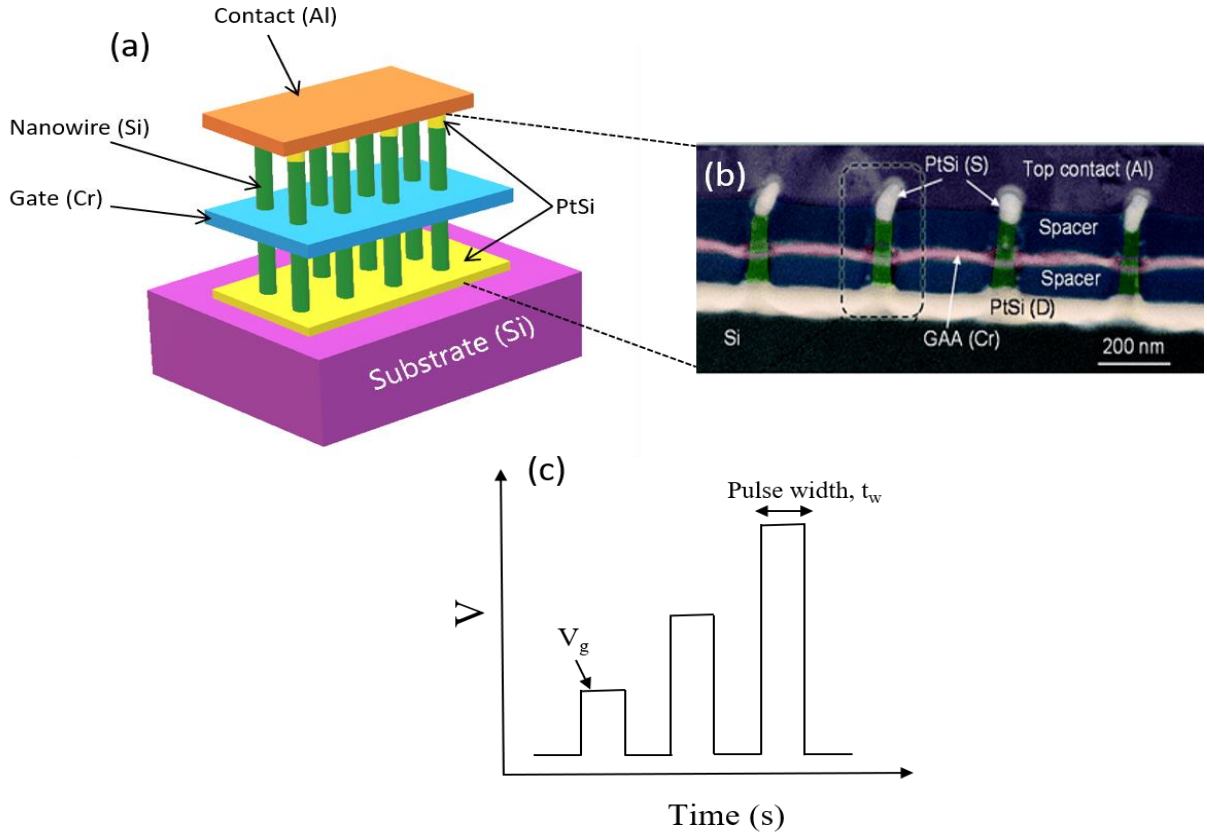
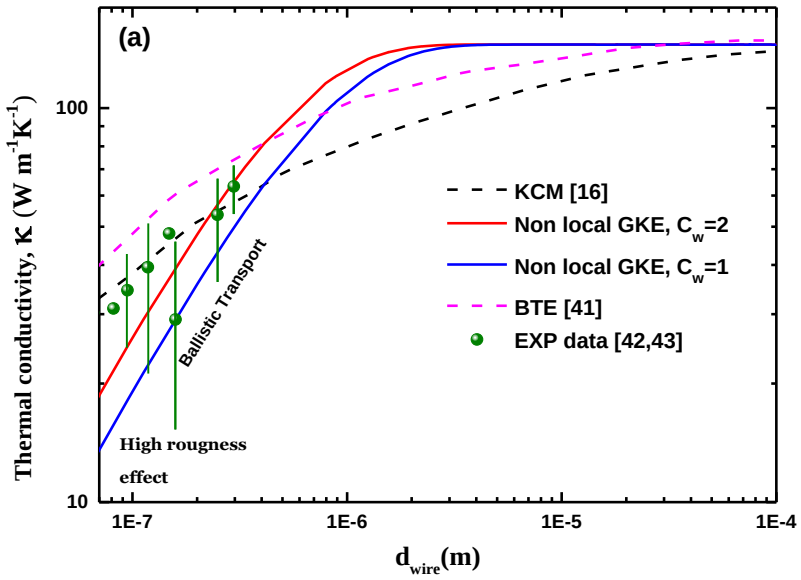


Fig. 3. Schematic representation of (a) vertical GAA junctionless nanowire field effect transistors. (b) TEM cross-section of the VNWFET device. (c) Pulsed (I-V) measurement setup.



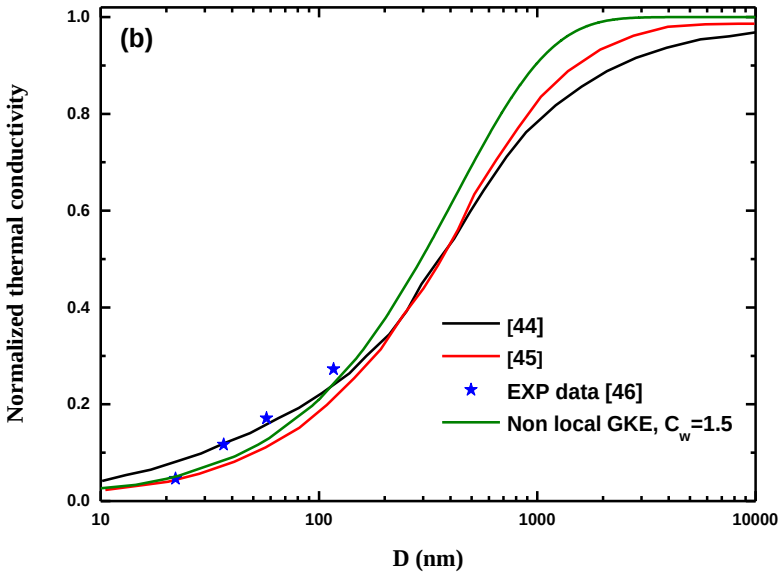
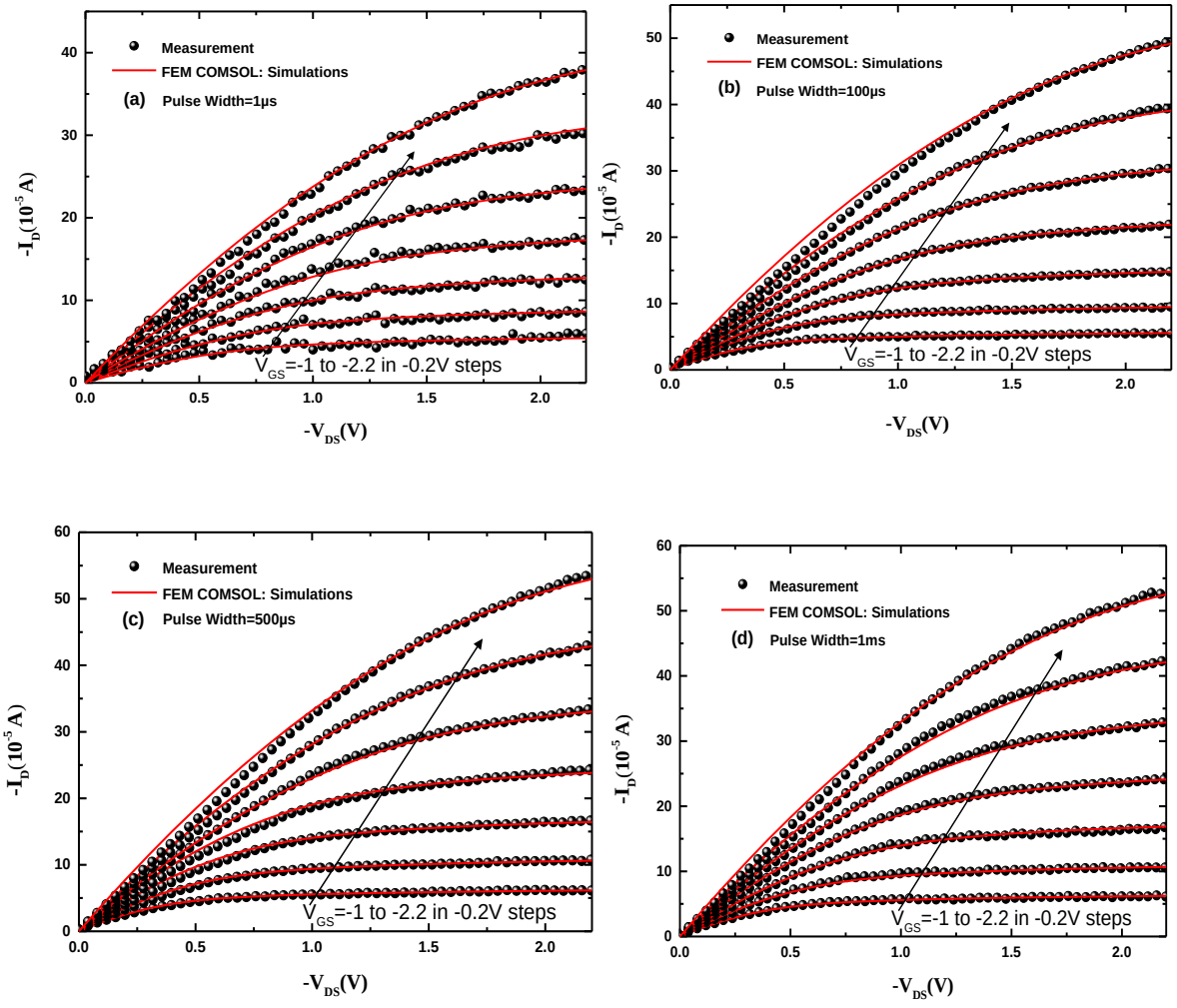


Fig. 4. Comparison of (a) effective and (b) normalized thermal conductivity for silicon nanowire at room temperature.



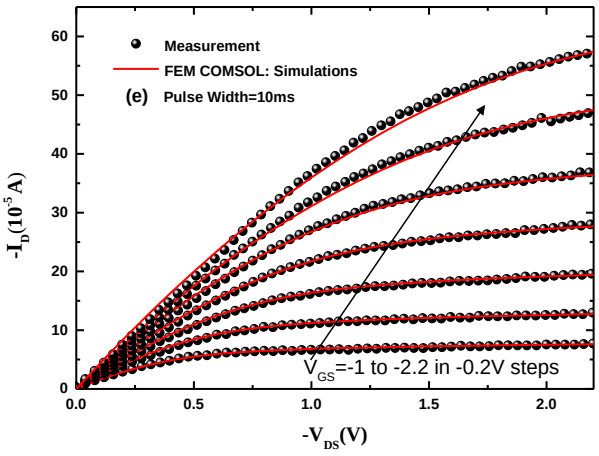


Fig. 5. Pulsed I-V characteristics of the p-type VNWFET including 25 nanowires in parallel with $D = 22\ nm$ at $T = 300K$. (a) $t_p = 10\ \mu s$, (b) $t_p = 100\ \mu s$, (c) $t_p = 500\ \mu s$, (d) $t_p = 1\ ms$ and (e) $t_p = 10\ ms$. The surface roughness parameter is fixed at $C_w = 1$.

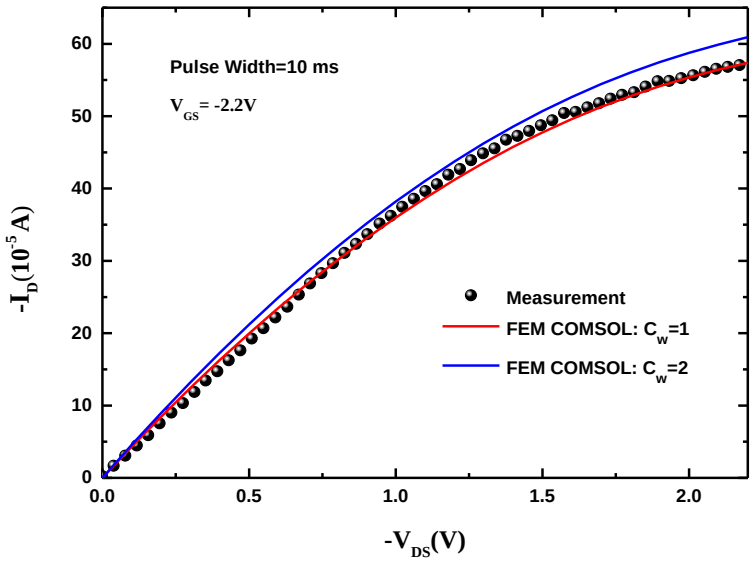


Fig. 6. Evolution of drain current for different surface roughness at high bias condition $V_{GS} = -2.2V$.

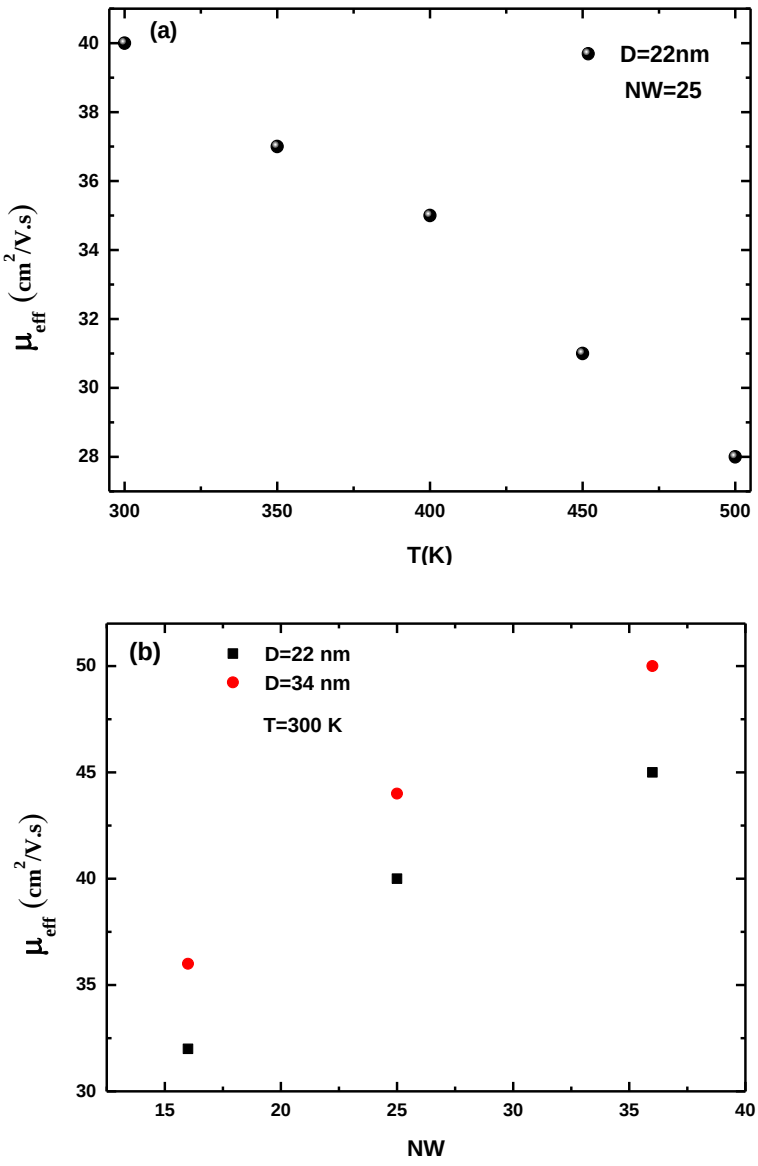


Fig. 7. The extracted effective mobility in VNWFET as function of (a) Temperature and (b) Nanowires in parallel.

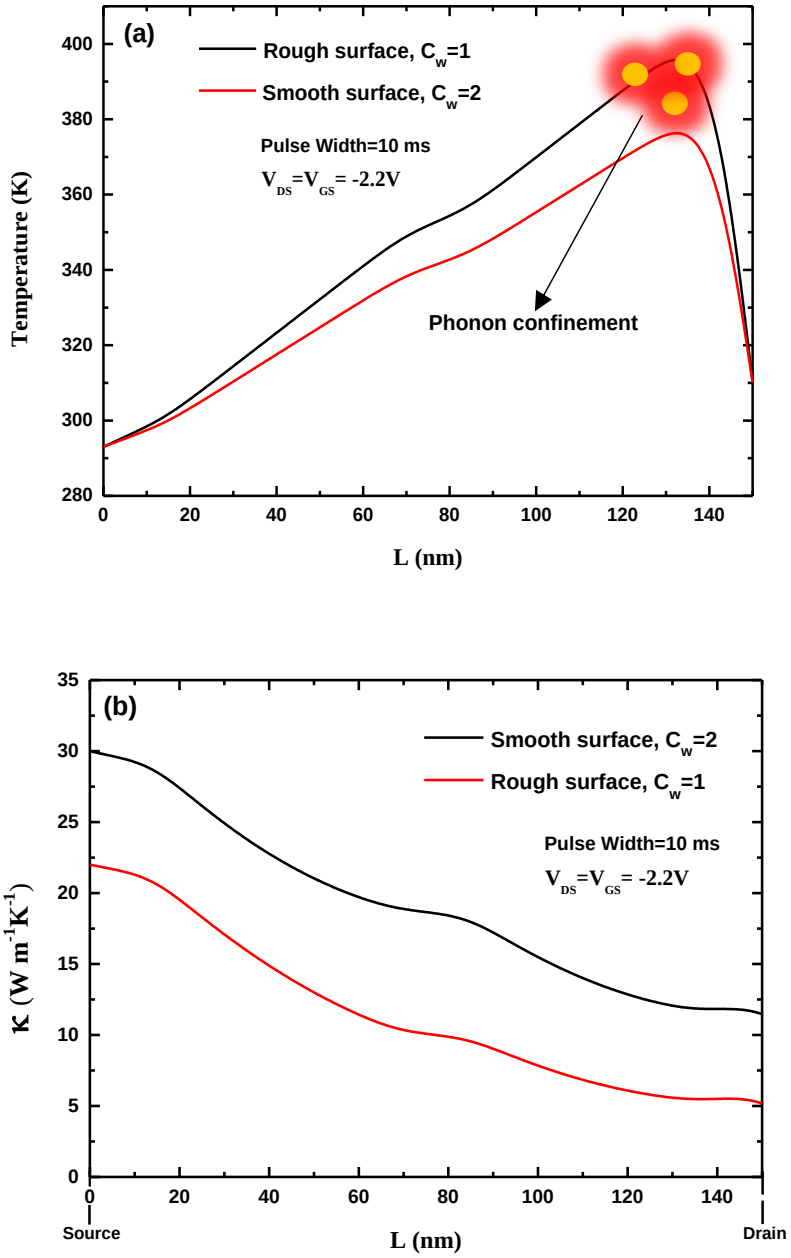


Fig. 8. The extracted (a) temperature and (b) thermal conductivity along a single nanowire for different surface roughness.

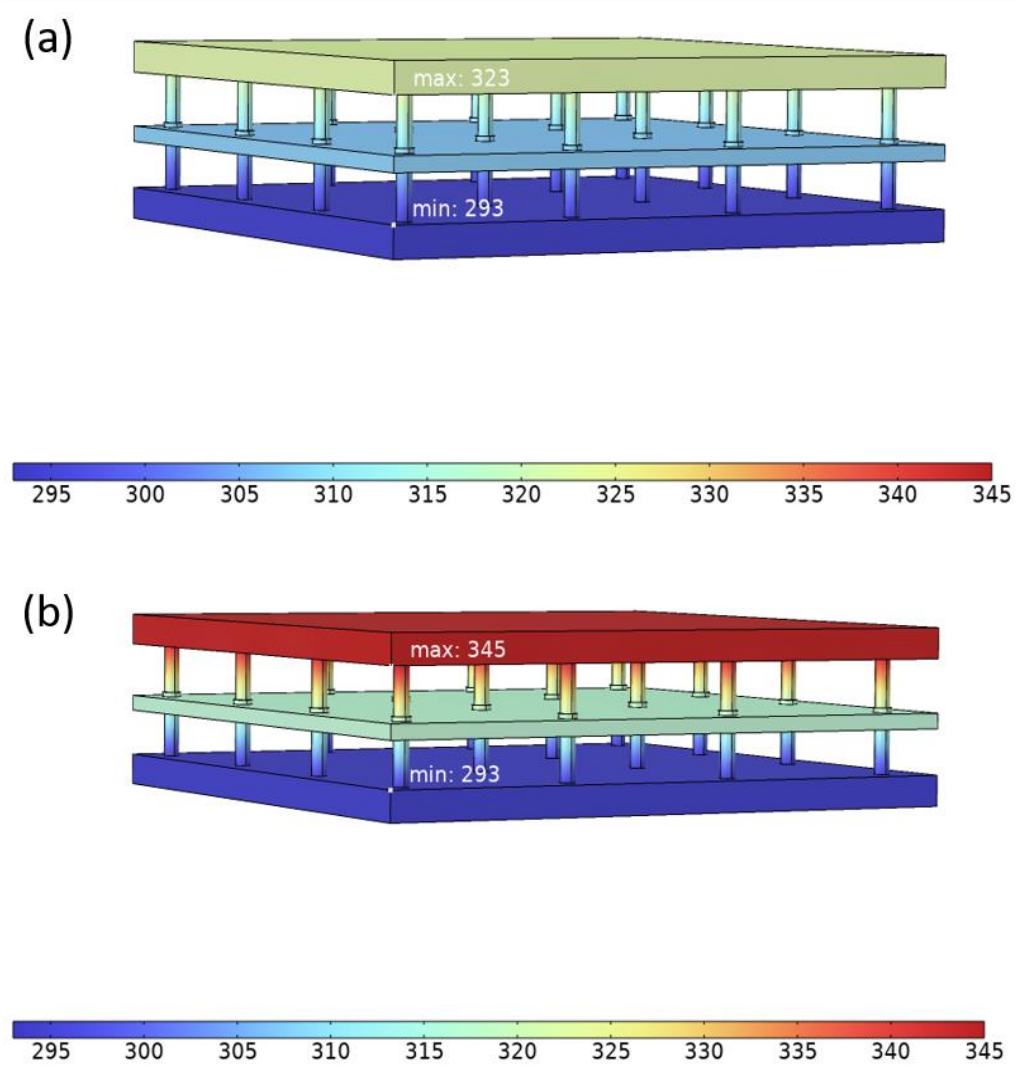


Fig. 9. 3D thermal distribution in VNWFET including 16 NWs in parallel with $D = 22\,nm$ at high bias condition $V_{GS} = V_{DS} = -2.2V$. (a) Surface roughness; $C_w = 2$, (b) Surface roughness; $C_w = 1$.