

# Challenges in characterizing BiCMOS SiGe HBT technologies

for FOM evaluation and compact modelling

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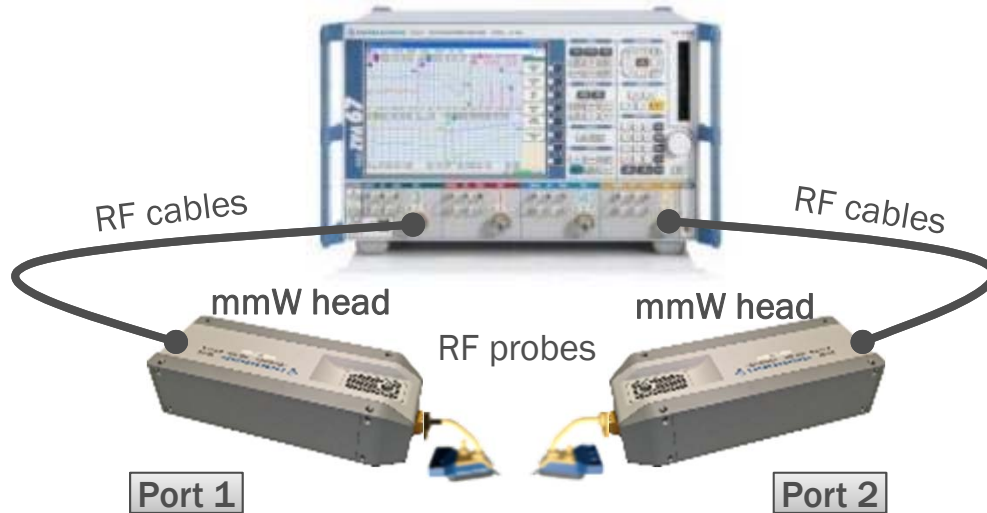
# OUTLINE

- Introduction
  - Measuring FOM of transistors and calibration methods
  - Impact of probe coupling on FOM measurements
- 16 errors terms methodology and definition of its standards
- Results: SiGe HBT measurement up to 220 GHz & comparison with simulation
- Conclusion

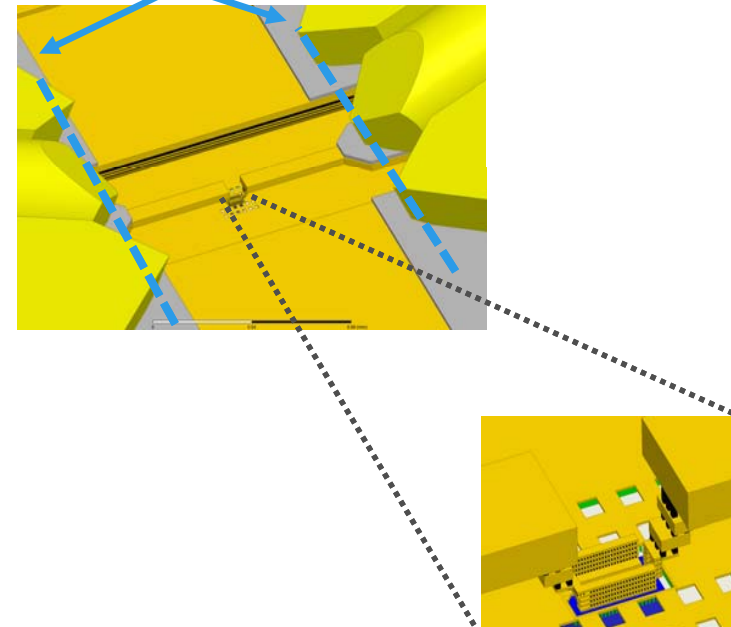
# INTRODUCTION

## Off-wafer calibration procedure

Vector Network Analyzer (VNA)



Reference plane after calibration



1 → Off-wafer calibration on ISS



Impedance Standard Substrate

2 → On-wafer de-embedding

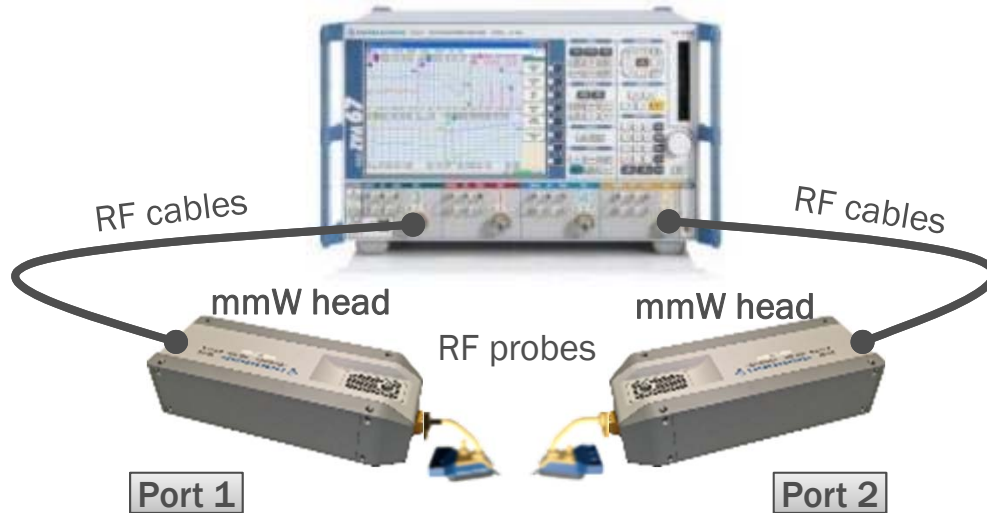
- "Complete" OPEN (at M1)
- "Complete" SHORT (at M1)

Open-Short de-embedding or PSO / PTSO ...

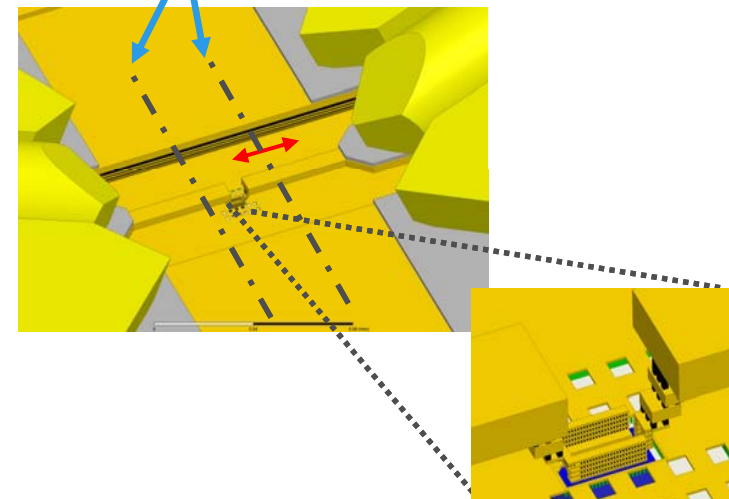
# INTRODUCTION

## On-wafer calibration procedure

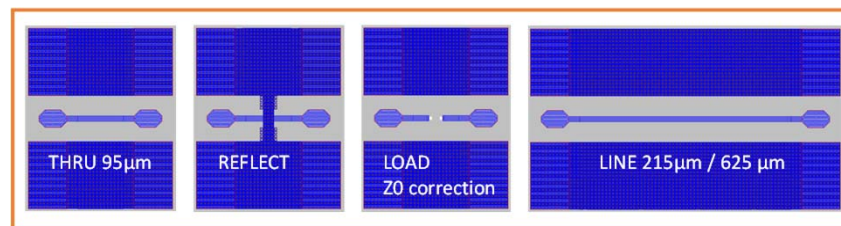
Vector Network Analyzer (VNA)



Reference plane after calibration



1 → On-wafer TRL calibration



2 → On-wafer de-embedding

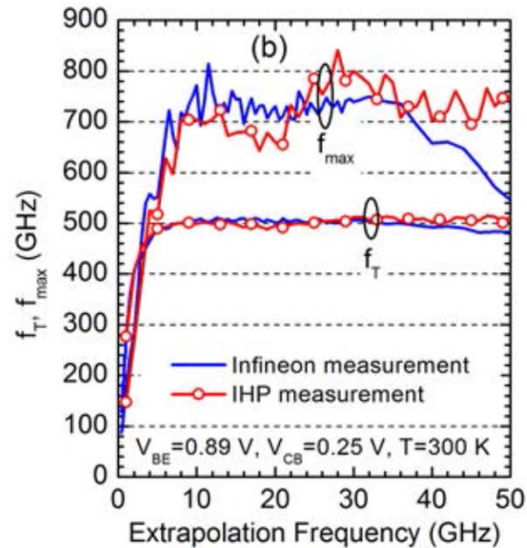
- "Complete" SHORT (at M1)
- "Complete" OPEN (at M1)

Choose ref. plane & apply SO or OS de-embedding

# Impact of test structure and probes on calibration ?

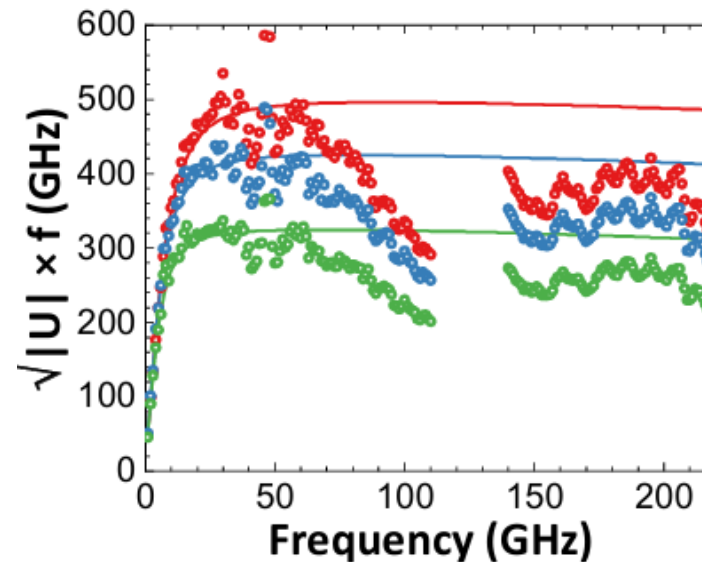
Impact of calibration/probes on  $f_{\max}$  measurement

Example 1 on SiGe HBT



Mason's and H21 gain-bandwidth product vs frequency for the same SiGe HBT measured at IHP and Infineon  
B. Heinemann *et al* IEDM 2016, [4]

Example 2 on InP DHBTs



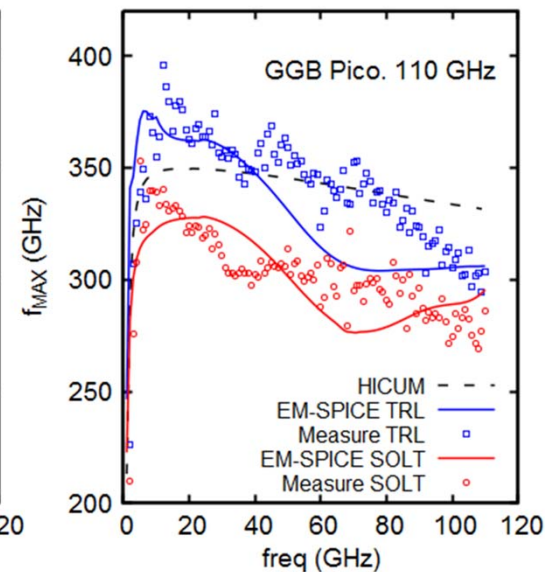
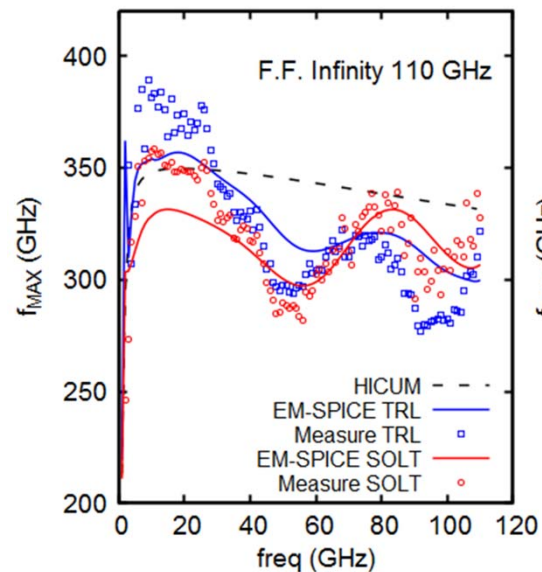
Bipolar transistors (InP DHBTs) Mason's gain-bandwidth vs frequency product at different collector current  $I_C$  and  $V_{CE} = 1.6$  V  
N. Davy *et al* EuMIC 2023 [5]

- ⇒ Measuring FOMs of miniaturized transistors becomes a challenge when their  $f_{\max} \gg 100$  GHz
- ⇒ Parasitic from EM probe coupling ~ intrinsic element of the transistor

# Impact of test structure and probes on calibration ?

## Impact of calibration/probes on FOM measurement

- Measuring the same device with two different probes
- Measuring the same device with off-wafer or on-wafer calibration



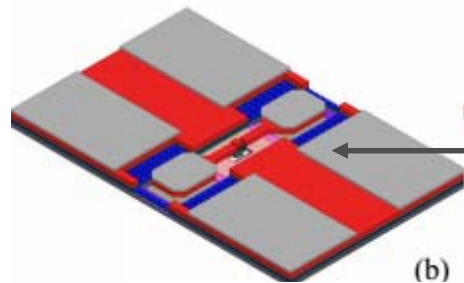
➔ Influence of probes is not removed by calibration

# Impact of test structure and probes on calibration ?

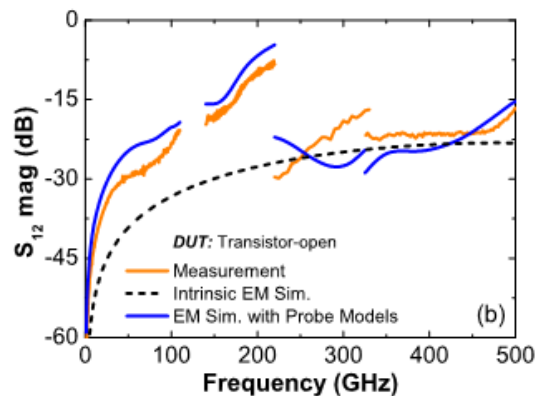
Impact of calibration/probes on FOM measurement : measurement up to 500 GHz & discontinuities



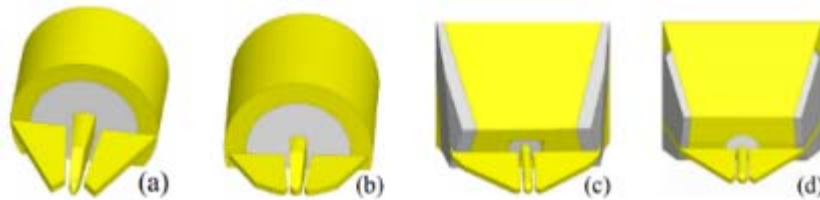
Worst case example : 90 $\mu$ m inter-probe distance



Transistor open



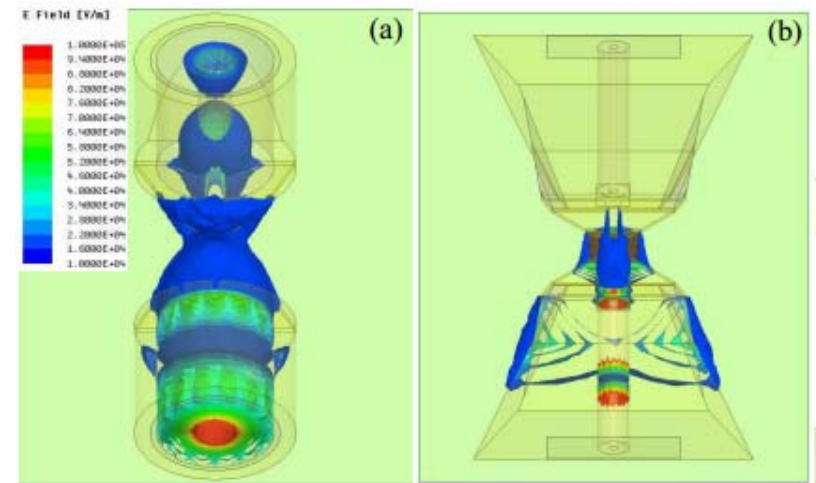
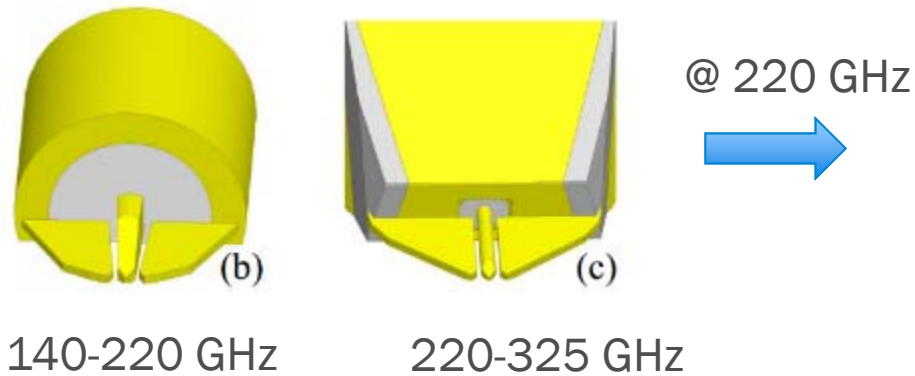
- ❑ Discontinuities & trends are clearly explained by EM model
- ❑ The discontinuities are not the result of probe misplacement since reproduce by EM simulation but the result of an inaccurate calibration and structures design



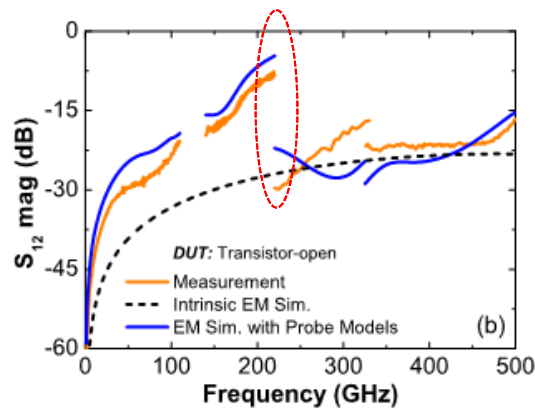
# Impact of test structure and probes on calibration ?

Impact of calibration/probes on FOM measurement : measurement up to 500 GHz & discontinuities

- Advance probe models is required to understand measurement imperfections



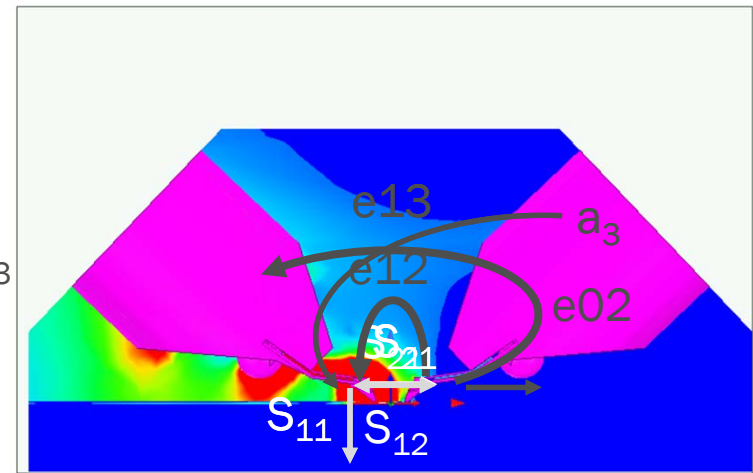
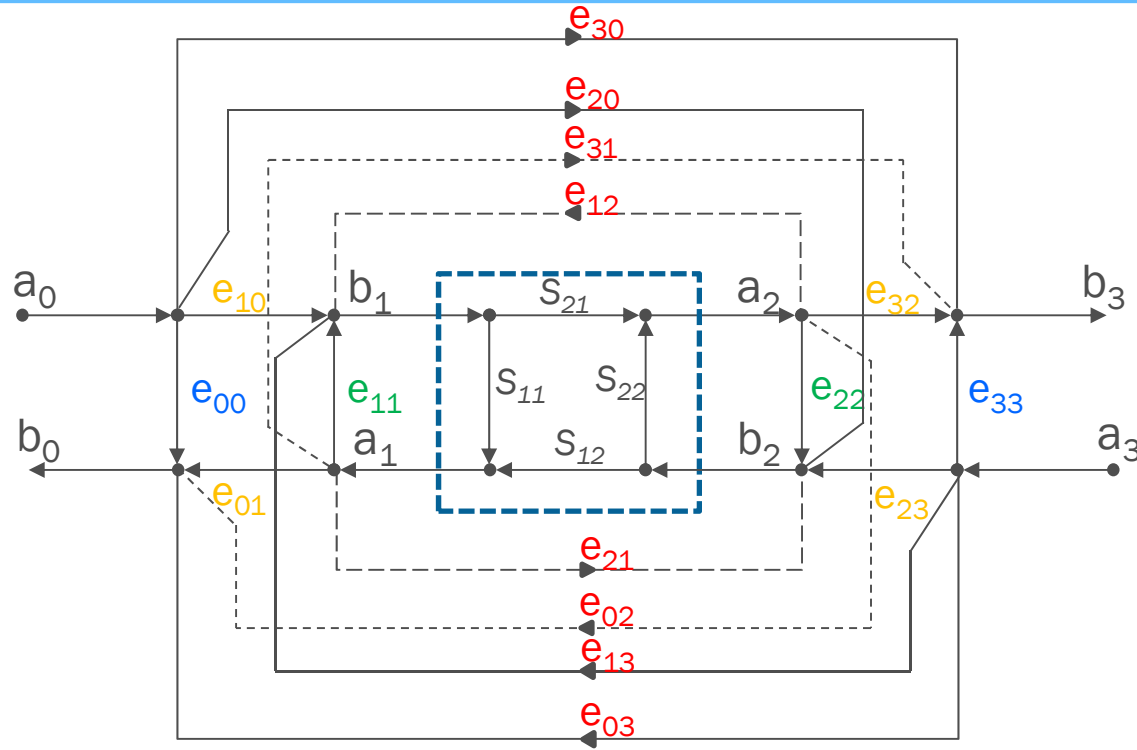
Electric field (E-field) distribution (top and side views) in the transistor-open at 220 GHz using two probe models



- Probes couplings need to be calibrated
- Use of the 16 terms-error model



# 16 error terms model



$e_{30}$  and  $e_{03}$  models leakage within the VNA

Port Match:  $e_{11}$ ,  $e_{22}$

Directivity:  $e_{00}$ ,  $e_{33}$

Frequency Response:  $e_{01}$ ,  $e_{10}$ ,  $e_{32}$ ,  $e_{23}$

Leakage:  $e_{30}$ ,  $e_{03}$ ,  $e_{31}$ ,  $e_{13}$ ,  $e_{21}$ ,  $e_{12}$ ,  $e_{20}$ ,  $e_{02}$



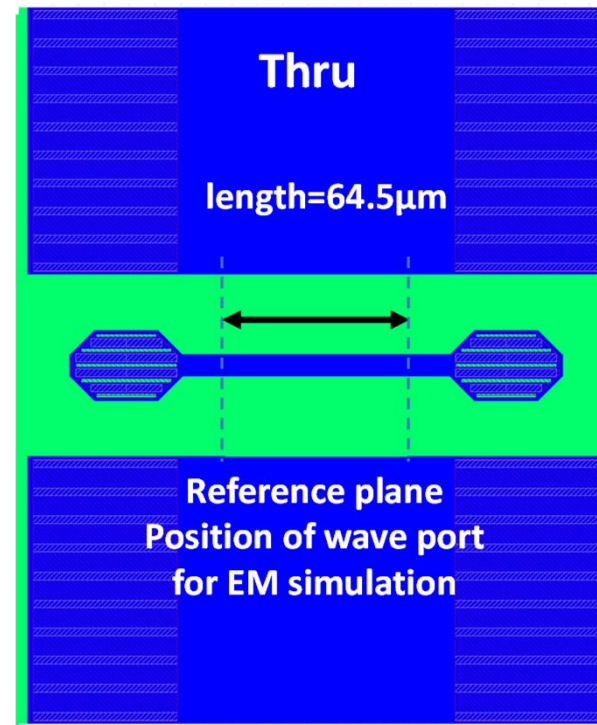
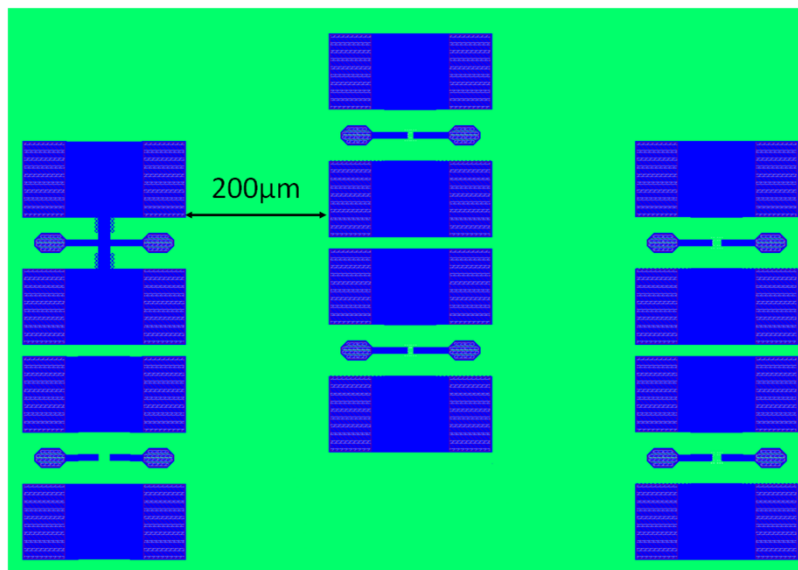
- Error terms find using SVD
- Implementation in ICCAP using Python and PEL

J. V. Butler et al., *IEEE Trans. MTT* 1991, doi: 10.1109/22.106567

# Design of test structures for on wafer calibration

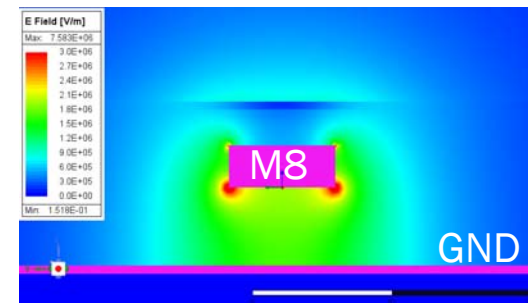
BiCMOS 55nm layout

Floorplan

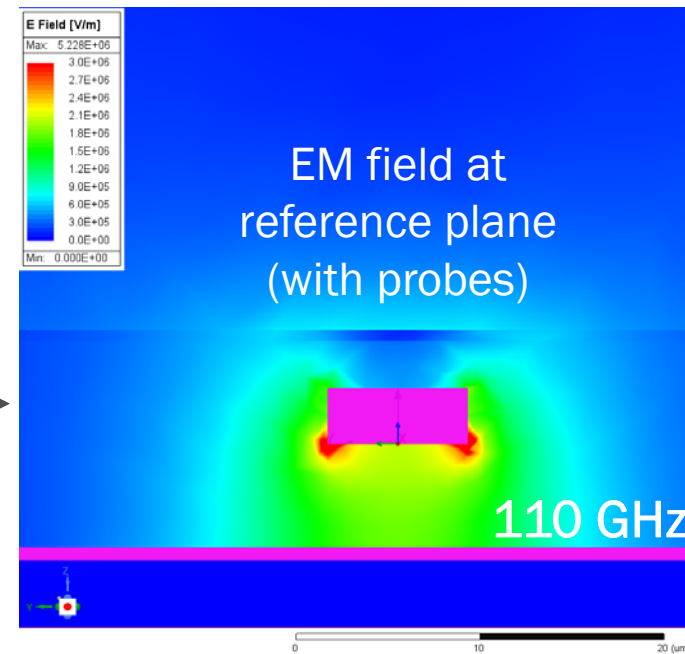
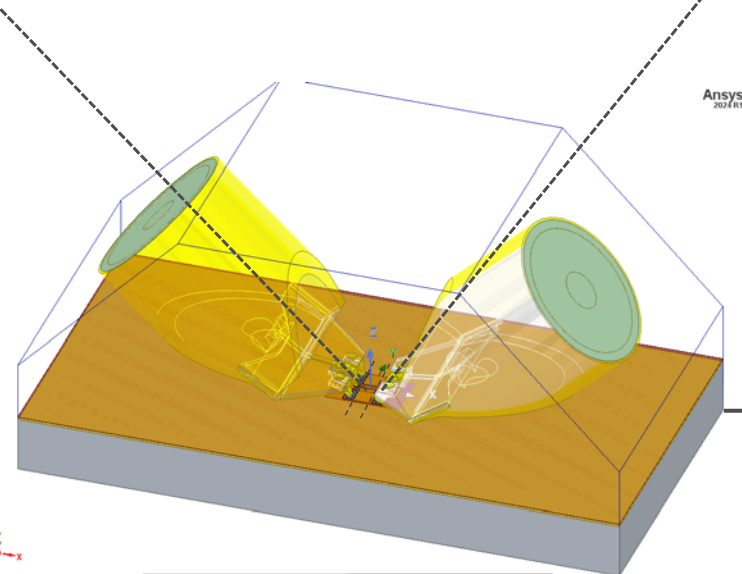
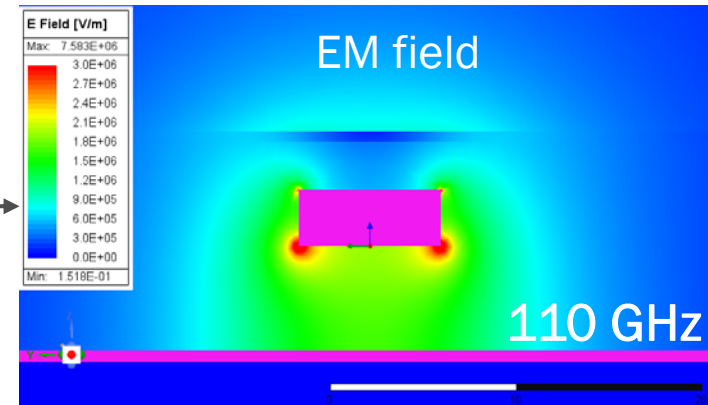
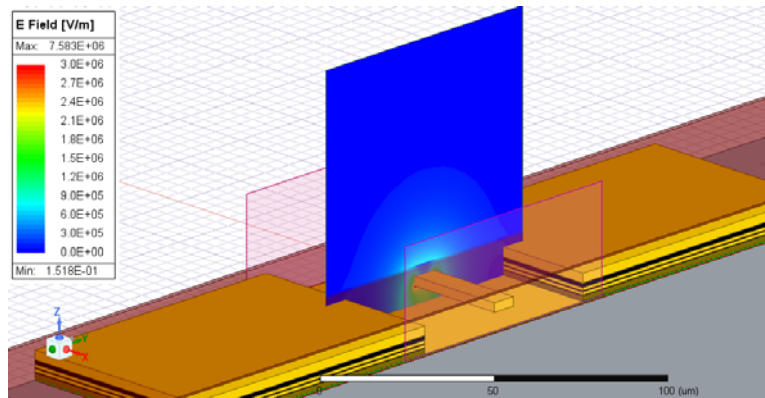


Microstrip line cross-section

- 5 test structures used for 16T calibration:
  - Thru, Short M8, Open M8, Load, Load-Short
- 3 lines available for TRL calibration



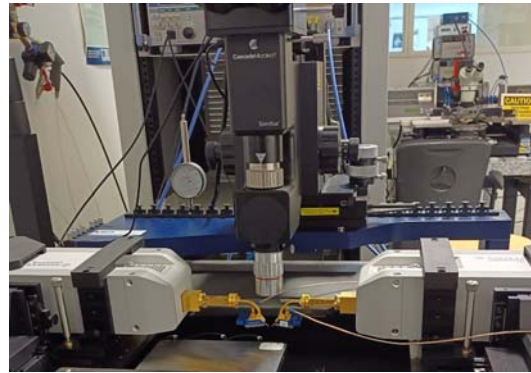
# Verification of propagation mode establishment for TRL



# Definition of standards

Build intrinsic test structure in EM simulator using layout and BEOL definition

Feed EM simulator parameter using DRM

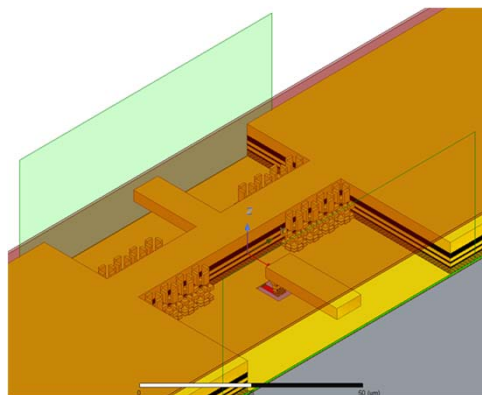


Adjust physical parameters in EM simulator and update EM & 16T cal. if need

1

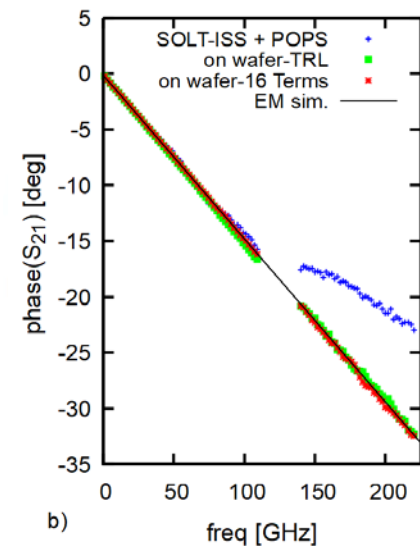
2

3



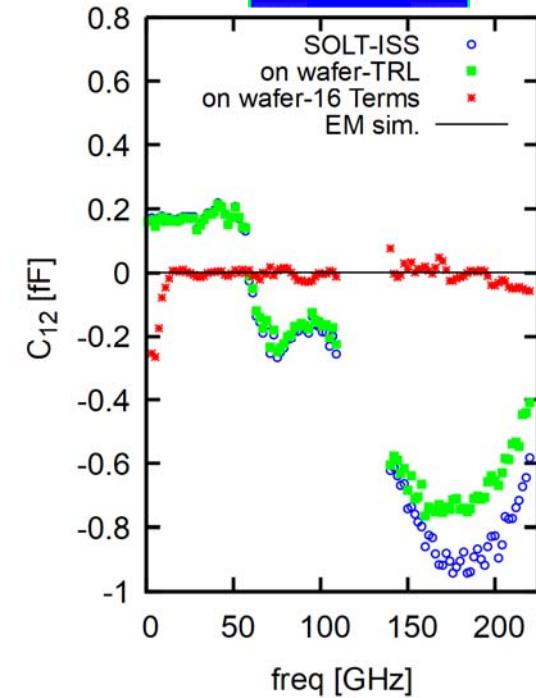
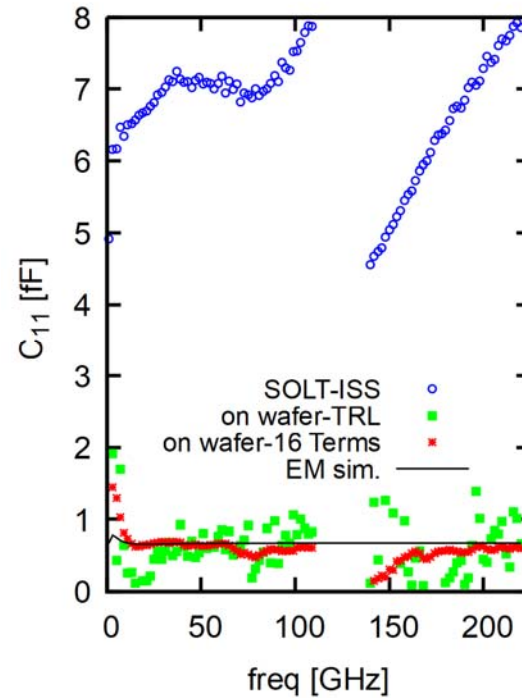
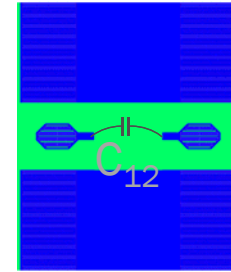
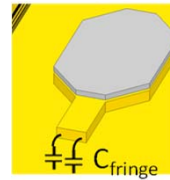
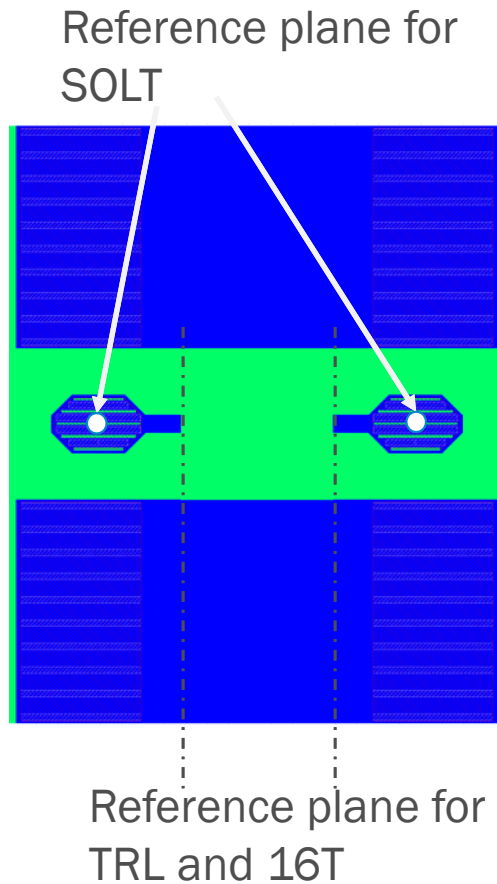
Perform raw measurements

Apply TRL and 16T simultaneously and verify consistency (lines & error terms)



# Results: verification (1/3)

Pad-open (no used for calibration)

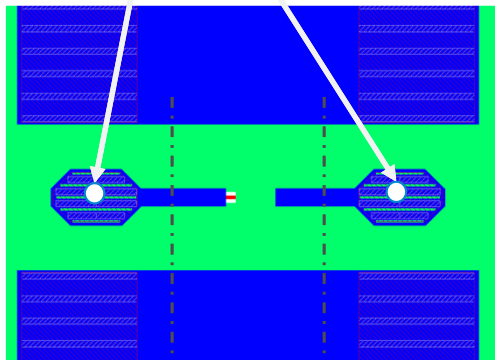


16T performs better than SOLT and is more accurate than TRL for C12

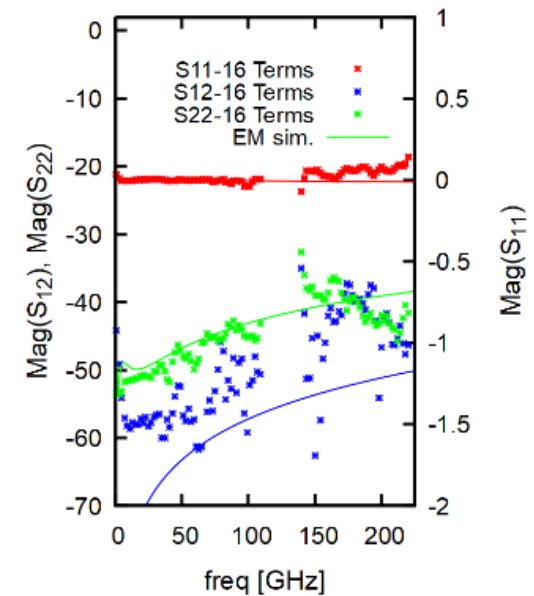
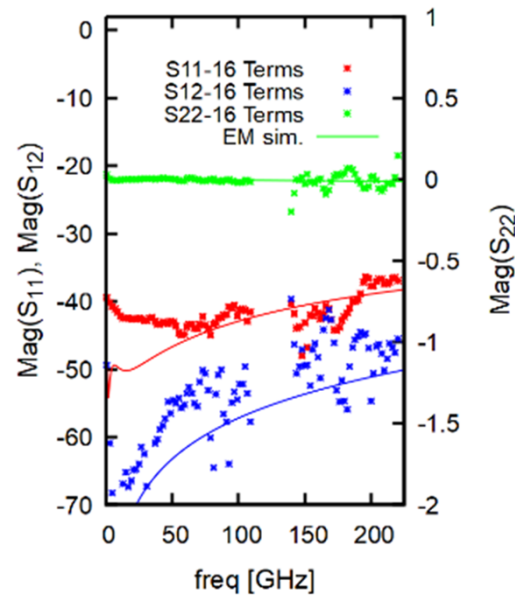
# Results: verification (2/3)

Load-open and open-load (no used for calibration)

Reference plane for SOLT



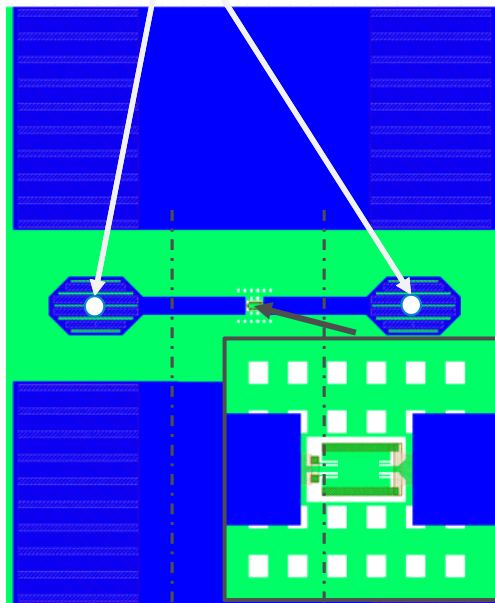
Reference plane for TRL and 16T



# Results: verification (3/3)

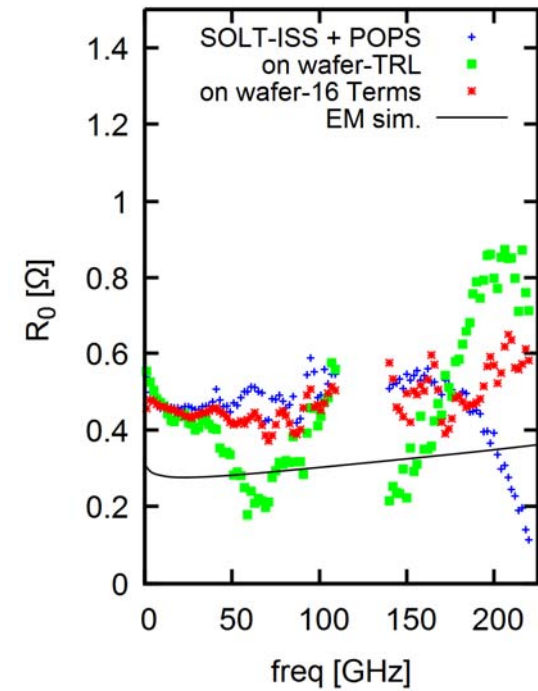
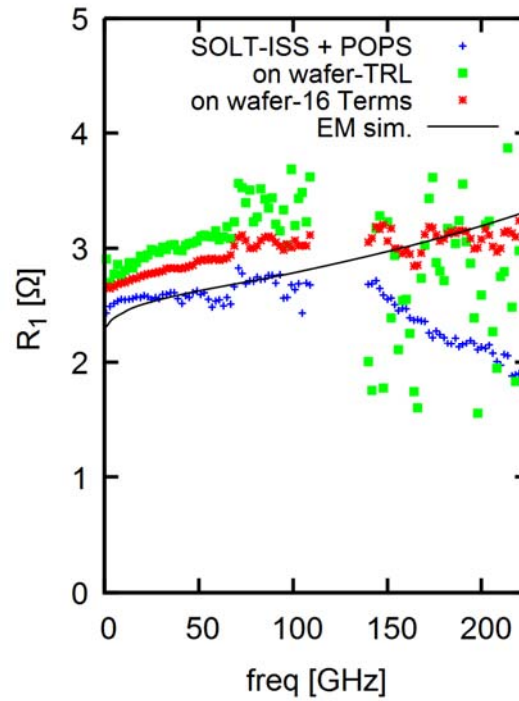
Transistor-short (no used for calibration)

Reference plane for SOLT



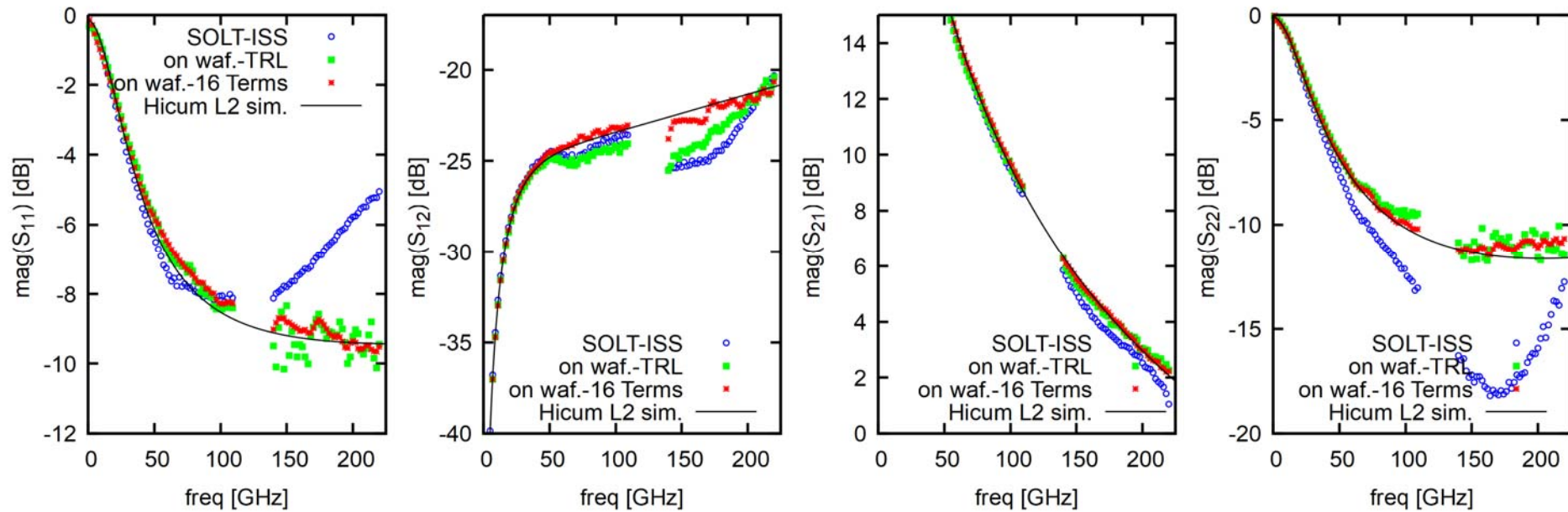
Reference plane for:

- TRL and 16T
- SOLT after pad-open/pad-short de-embedding



# Results: transistor S parameters (2/2)

Measurement performed at  $V_{BE}=0.9$  V and  $V_{CB}=0$ V



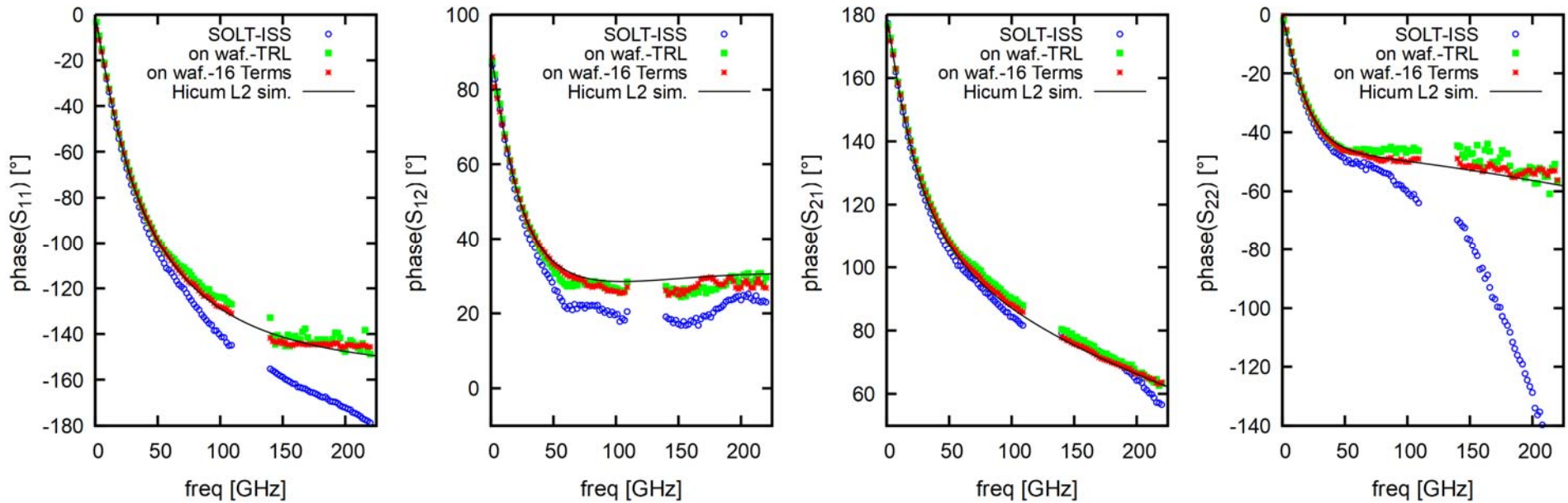
De-embedding is :

- transistor-short/transistor-open for TRL and 16T
- transistor-open/transistor-short for SOLT-ISS



# Results: transistor S parameters (2/2)

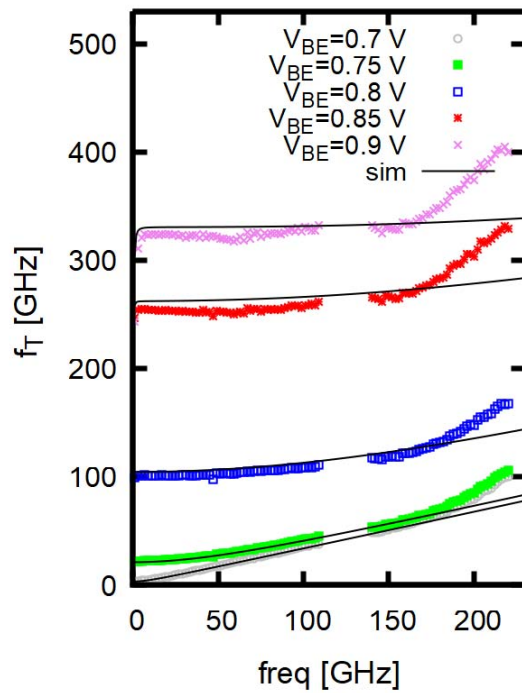
Measurement performed at  $V_{BE}=0.9\text{ V}$  and  $V_{CB}=0\text{V}$



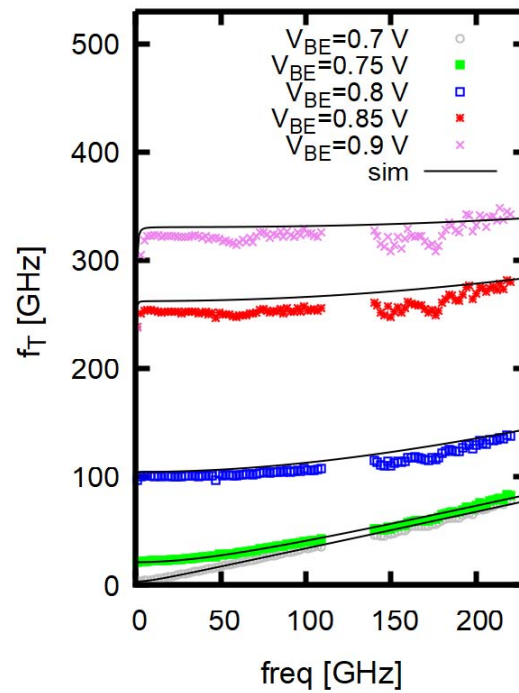
# Results: transistor FOM measurement (1/2)

Transit frequency extraction: H21 current gain \* frequency

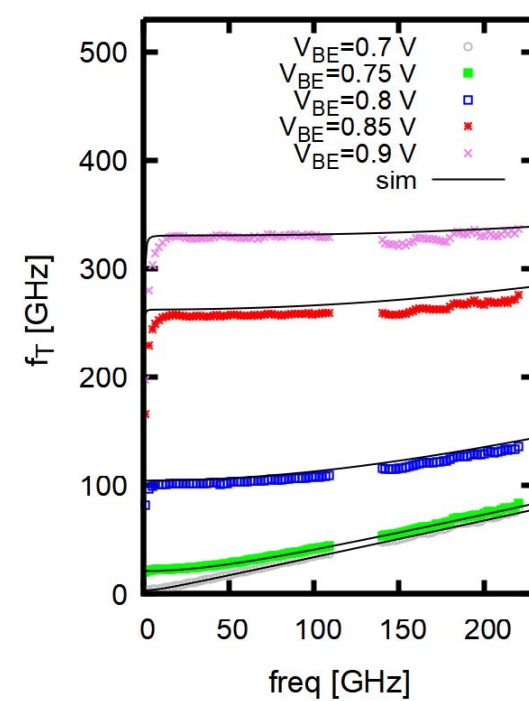
### SOLT



### On-wafer TRL

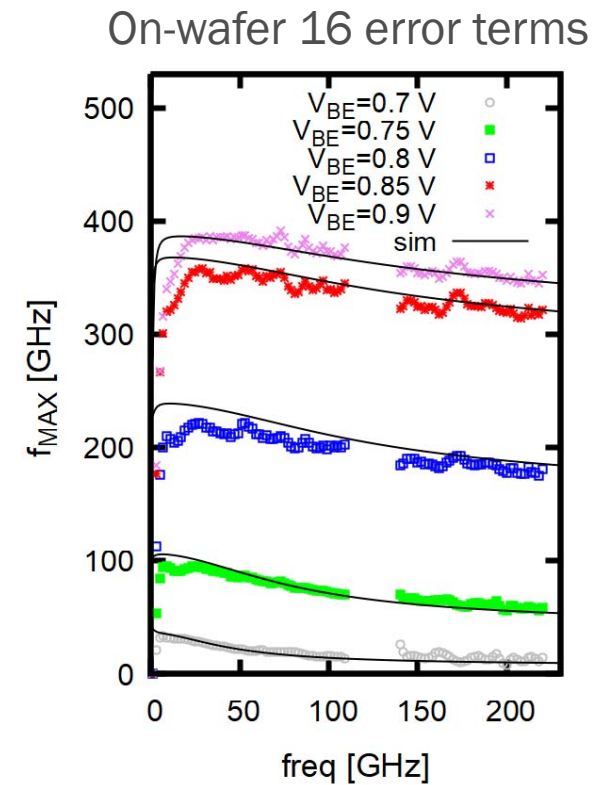
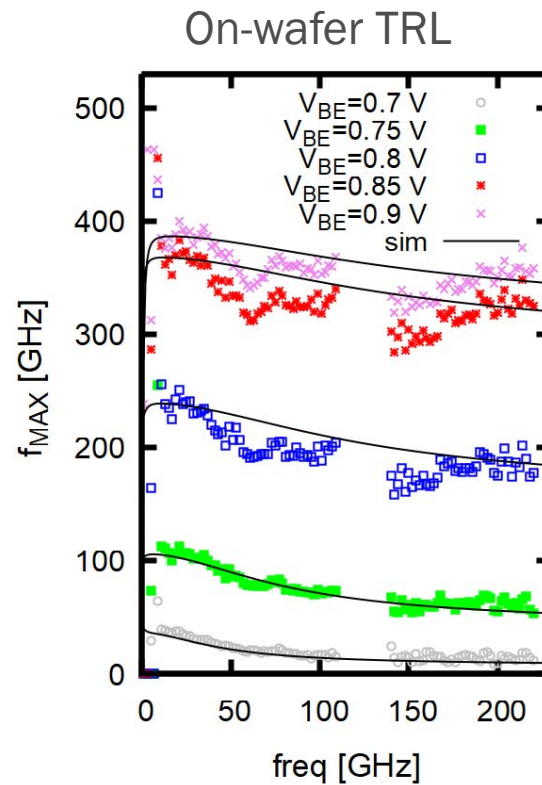
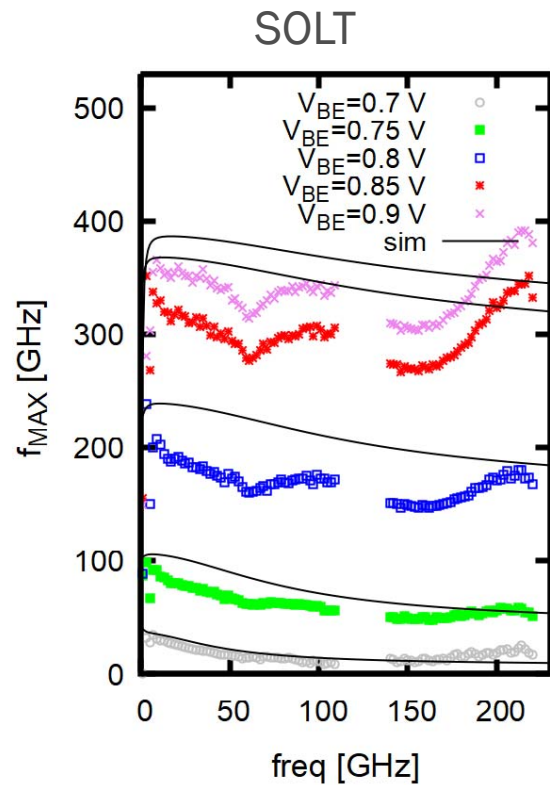


### On-wafer 16 error terms

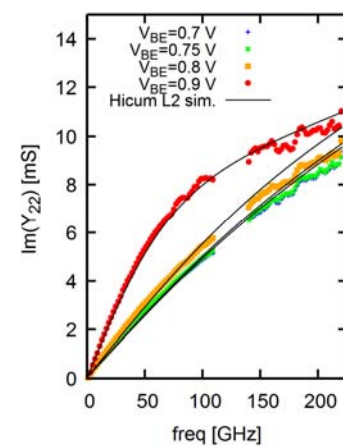
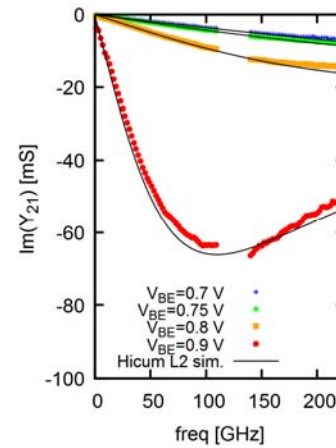
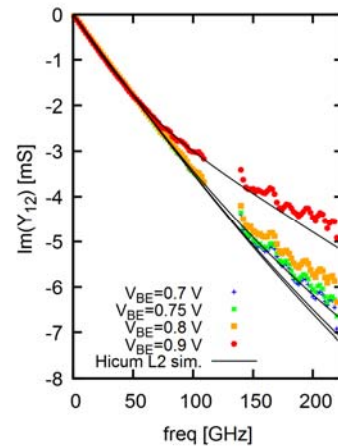
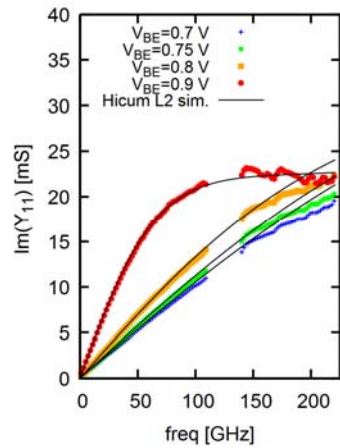
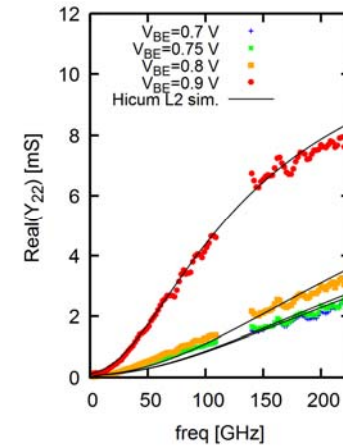
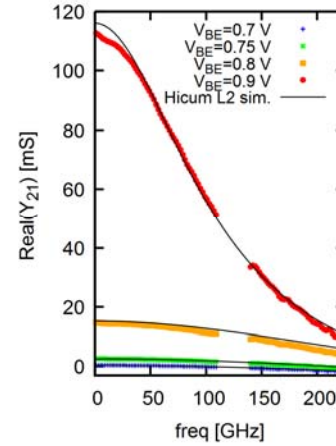
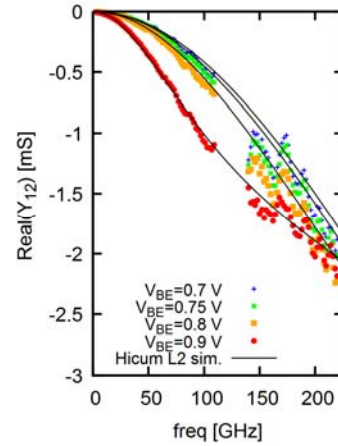
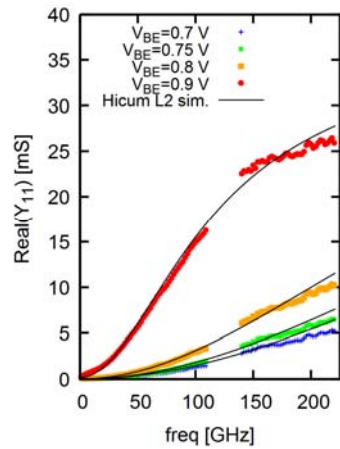


# Results: transistor FOM measurement (2/2)

Maximum oscillation frequency extraction:  $\text{Power gain}^{1/2} * \text{frequency}$

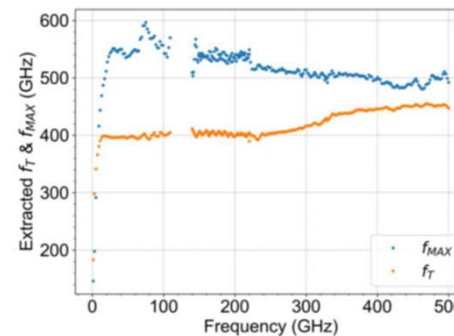


# Compact model verification up to 220 GHz



# Conclusion

- 16 error-terms algorithm has been implemented in ICCAP using SVD (Python & PEL code)
- Specific standards have been designed in BiCMOS from STM
- Definition of reference standards has been done using EM simulation and TRL measurement
- TRL is efficient if crosstalk can be neglected (not the case for high density Si techno.)
  - $e_{12}$  introduced by the probe must be  $\ll S_{12}$  of the intrinsic transistor when using TRL
  - => otherwise: use the 16 error terms calibration
- Outlooks: see the 16T calibration applied on BiCMOS 55X HBT ( $f_{MAX} > 500$  GHz) (see it at IEEE [RWW2025](#) ) showing almost no-band discontinuity on measurement up to 500 GHz



# Acknowledgements

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- Acknowledgement to **SHIFT** : SHIFT Sustainable technologies enabling Future Telecommunication applications (Grant agreement ID: 101096256 DOI: [10.3030/101096256](https://doi.org/10.3030/101096256))
- Acknowledgments to RF-Net and NANOCOM platform from my lab.
- Acknowledgement to **ANR PRECISE**



# Bibliography

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- ▶ [4] C. Yadav, « Importance and Requirement of frequency band specific RF probes EM Models in sub-THz and THz Measurements up to 500 GHz », *IEEE Trans. Terahertz Sci. Technol.*
- ▶ [5] N. Davy et al., « InP DHBT On-Wafer RF Characterization and Small-Signal Modelling up to 220 GHz », in *2023 18th European Microwave Integrated Circuits Conference (EuMIC)*, sept. 2023, p. 101-104. doi: 10.23919/EuMIC58042.2023.10288849.
- ▶ [6] B. Heinemann et al., « SiGe HBT with  $f_x/f_{max}$  of 505 GHz/720 GHz », in *2016 IEEE International Electron Devices Meeting (IEDM)*, déc. 2016, p. 3.1.1-3.1.4. doi: 10.1109/IEDM.2016.7838335.
- ▶ [7] S. Fregonese et al., « Comparison of On-Wafer TRL Calibration to ISS SOLT Calibration With Open-Short De-Embedding up to 500 GHz », *IEEE Trans. Terahertz Sci. Technol.*, vol. 9, n° 1, Art. n° 1, janv. 2019, doi: 10.1109/TTHZ.2018.2884612.
- ▶ [8] L. Galatro et M. Spirito, « Millimeter-Wave On-Wafer TRL Calibration Employing 3-D EM Simulation-Based Characteristic Impedance Extraction », *IEEE Trans. Microw. Theory Tech.*, vol. 65, n° 4, Art. n° 4, avr. 2017, doi: 10.1109/TMTT.2016.2609413.