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Gate voltage dip as a new indicator for on-line health monitoring of SiC MOSFETs

Mathis Picot-Digoix, Frédéric Richardeau, *Senior Member, IEEE*, Jean-Marc Blaquière, Sébastien Vinnac, Stéphane Azzopardi and Thanh-Long Le

Abstract—Due to the poor quality of the silicon carbide / silicon dioxide interface realisation and their thin gate oxide layer, SiC MOSFETs are more susceptible to charge trapping mechanisms than silicon MOSFETs. These phenomena are amplified over time, resulting in decreased transistor performance and increased losses. To monitor this ageing mechanism, an analog method is proposed to extract a newly discovered health indicator from the gate voltage (V_{GS}) waveform. This is accomplished by slowing down a specific turn-on using a dual-channel active gate driver. The on-line health monitoring method is then experimentally validated on a 1200V-36A SiC MOSFET in both no-load and pulse width modulation (PWM) conditions.

I. INTRODUCTION

In silicon (Si) MOSFETs, Si and silicon dioxide (SiO_2) have a natural chemical affinity, which facilitates the growth of a uniform and low-defect oxide layer. In contrast, silicon carbide (SiC) has a different and more complex crystalline structure than Si, which makes the SiC/ SiO_2 interface more prone to defect formation and reduces the channel mobility [1]. To offset the reduced electron mobility in SiC MOSFETs, the gate oxide thickness is reduced to optimize channel resistance and achieve an acceptable threshold voltage V_{TH} . Thinning the gate oxide increases the applied electric field, and the electrical stress [2]. In addition, SiC MOSFETs tend to operate at high temperatures. Both of these contributions further facilitate a charge trapping tunneling process in defects at the near-oxide interface. As a result, the intrinsic parameters of the MOSFET drift over time, leading to performance degradation and reliability concerns.

Gate oxide health monitoring strategies have emerged around different indicators to aid in the maturation of SiC MOSFETs: V_{TH} [3], the gate plateau voltage V_P [4]–[6], its duration Δt_P [7], the gate leakage current I_{GSS} [8], and the source inductance voltage [9]. Extracting these parameters on-line within an operating converter is challenging. A solution to extract V_{TH} [10]–[12] is to detect the transistor channel formation and to extract the value of V_{GS} at that moment by leveraging the high-voltage DeSat diode. However, it has not yet been validated in on-line PWM mode. Another method uses the frequency spectrum characteristics of the transient gate voltage during the turn-on process. It extracts high-order V_{GS} harmonics to detect gate oxide degradation [13].

A low voltage strategy is proposed for on-line monitoring of the health of SiC MOSFETs. The Device Under Test (DUT) is a discrete TO-247-3 package 1200V-36A-80m Ω SiC MOSFET. This strategy further functionalises a switched-resistor active gate driver (AGD) presented in [14], [15]. The

proposal introduces a gate voltage dip (V_{DIP}) as a new health indicator that is particularly well-suited to analog tracking.

II. ACTIVE GATE DRIVER AND NEW GATE VOLTAGE DIP

To extract health indicators from the V_{GS} turn-on waveform, the switching speed must be reduced, allowing enough time for signal processing and optimising the signal-to-noise ratio. A high-value gate resistance buffer is dedicated to slow down the turn-on. To integrate this measure into a power converter, a dual-channel switched-resistor AGD is illustrated in Fig. 1.

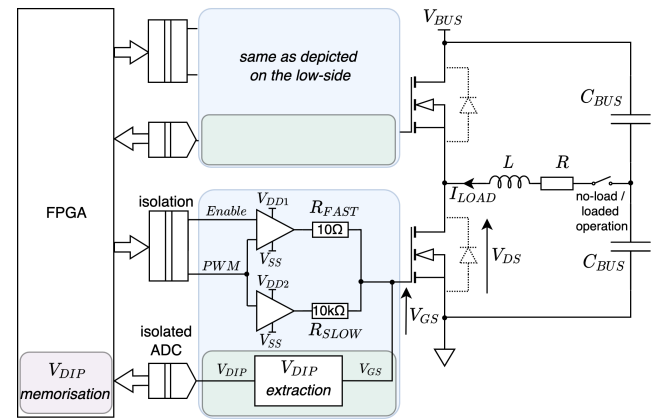


Fig. 1. Experimental setup and proposed AGD architecture for MOSFET health monitoring within an inverter leg ($V_{BUS}=600\text{V}$, $L=7.6\text{mH}$, $R=780\Omega$, $C_{BUS}=6\text{mF}$, $V_{SS}=-5\text{V}$, $V_{DD1}=V_{DD2}=20\text{V}$)

As depicted in Fig. 2, during normal PWM operation, the low-value gate resistance *Fast* buffer governs the switching ($Enable=1$). Then, a punctual slow turn-on is inserted within the PWM frame by placing the *Fast* buffer in high impedance ($Enable=0$), allowing the *Slow* buffer to take over.

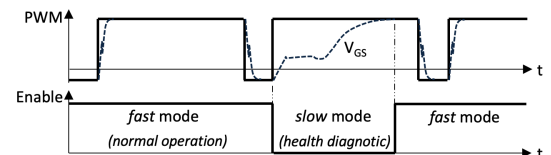


Fig. 2. Control signals chronogram, slow turn-on insertion in a PWM frame

Under these specific turn-on conditions, the gate enters a quasi-flying state, leading to the emergence of a previously overlooked phenomenon.

The current provided by the driver is initially considered negligible. As the MOSFET turns on and the drain-source voltage (V_{DS}) decreases during the Miller plateau, V_{DS} eventually

falls below a critical threshold value, V_{DSTH} (13V), as shown in Fig. 3a. At this point, the reverse transfer capacitance, C_{GD} , significantly increases (see Fig. 3b), which amplifies the gain between dV_{DS}/dt and dV_{GS}/dt (see eq.(1)).

$$\frac{dV_{GS}}{dt} = \frac{C_{GD}}{C_{GD} + C_{GS}} * \frac{dV_{DS}}{dt} \quad (1)$$

This increase causes the negative dV_{DS}/dt (i.e., the reduction in V_{DS}) to induce a transient drop in V_{GS} , resulting in the characteristic voltage dip, V_{DIP} (see Fig. 3a). This dip continues until V_{GS} approaches V_{TH} when the channel is nearly closed. Notably, V_{TH} has been widely recognized as a reliable health indicator in numerous studies [2]–[5]. Therefore, the dip value itself can serve as a similarly reliable health indicator.

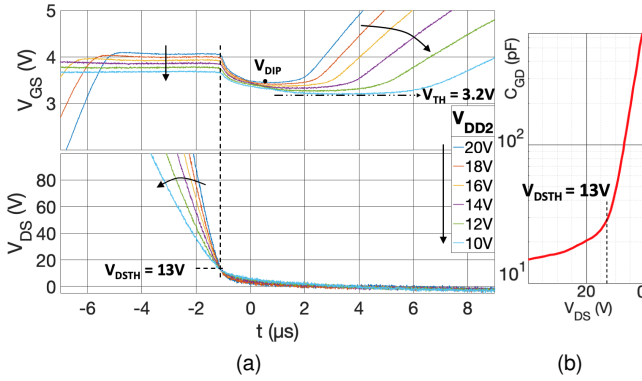


Fig. 3. Experimental waveforms of the plateau area and the corresponding drain voltage V_{DS} during a no-load slow turn-on under different drive voltages V_{DD2} (V_{TH} is extracted from a previous SMU characterisation) ($V_{BUS}=600V$, $T_{CASE}=20.5^{\circ}C$) (a) and evolution of C_{GD} with V_{DS} (from datasheet) (b)

In practice, even with a high gate resistance (10k Ω in this case), the driver still supplies some charge and maintains a minimal gate current, preventing V_{GS} from dropping fully to V_{TH} . Several tests in Fig. 3a were conducted with reduced driver voltages (V_{DD2}) to minimize the influence of the driver, thereby lowering the supplied current and achieving a dip value close to V_{TH} . This makes V_{DIP} a new indicator relevant to on-line gate oxide health monitoring.

III. HEALTH MONITORING STRATEGY

V_{DIP} represents a local minimum in the V_{GS} waveform, making it suitable for extraction. To achieve this, an analog circuit to extract V_{DIP} from V_{GS} is proposed. The core of this circuit is a modified peak detector, referred to as a "voltage dip memoriser" (see Fig. 4). It operates in three phases. During phase 1, the memory capacitor (C_{MEM}) tracks V_{GS} via diode D_1 . In phase 2, C_{MEM} discharges to V_{DIP} through diode D_2 . In phase 3, once V_{DIP} is captured, a switch is added in series with D_1 to ensure that C_{MEM} remains at V_{DIP} and does not follow the subsequent rise of V_{GS} . This prevents any post-dip fluctuations in V_{GS} from affecting the stored value. Fig. 5 shows the overall architecture.

When a high-value gate resistance (R_{SLOW}) is used, gate leakage currents can significantly affect V_{GS} . To mitigate this, a high-input impedance instrumentation amplifier is employed to isolate the gate from the extraction circuit for V_{DIP} . The

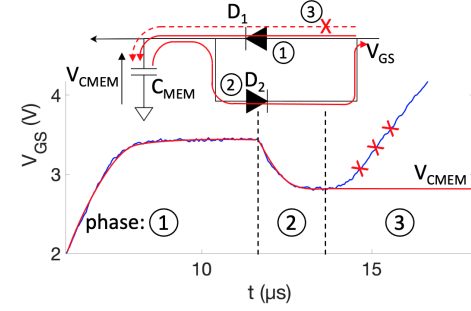


Fig. 4. Working principle of the proposed gate voltage dip memoriser

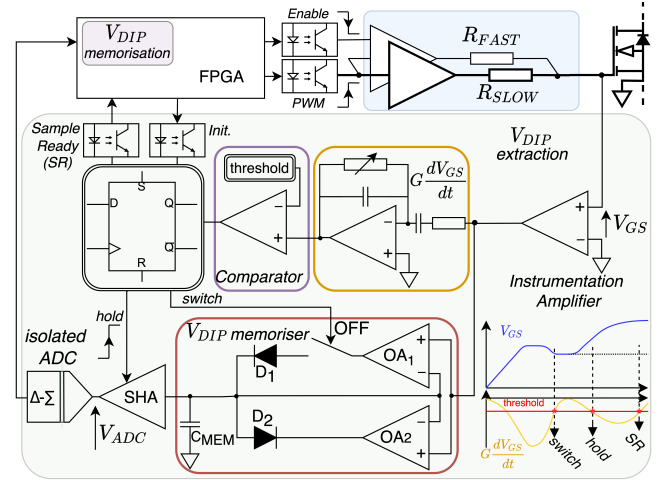


Fig. 5. Overview of the proposed AGD and V_{DIP} extraction scheme

resulting V_{GS} signal is then sent to the dip memoriser, which uses two low-leakage PN diodes (D_1 , D_2). To prevent the diodes' forward voltage from impacting V_{CMEM} , they are compensated using operational amplifiers (OA_1 , OA_2). C_{MEM} is selected as the maximum output capacitance acceptable by OA_1 and OA_2 to ensure maximum stability of the memorised dip value. Once C_{MEM} stores the V_{DIP} value, a sample-and-hold amplifier (SHA) is triggered, which maintains its output at V_{DIP} . The SHA provides up to 5mA output current, sufficient for processing by the ADC. Upon receiving a "SampleReady" signal (SR), the FPGA initiates the acquisition of V_{DIP} with 16-bit precision, and the value is stored in memory for long-term monitoring. Any drift in V_{DIP} could indicate potential ageing of the SiC MOSFET. The timing and control of the dip memoriser and SHA are managed by a trigger chain that includes an adjustable gain differentiating stage, a threshold comparison stage, and a series of flip-flops. This chain can be adjusted to accommodate different DUTs.

IV. EXPERIMENTAL VALIDATION

The health monitoring AGD board is shown in Fig. 6. It is plugged into a 600V inverter leg and is controlled by a Graphical User Interface (GUI) through an FPGA board. The proposed AGD drives the low-side (LS) switch, while the high-side (HS) is equipped with a standard gate driver.

The health monitoring method is first characterised under no-load condition. The HS switch is turned on first to charge

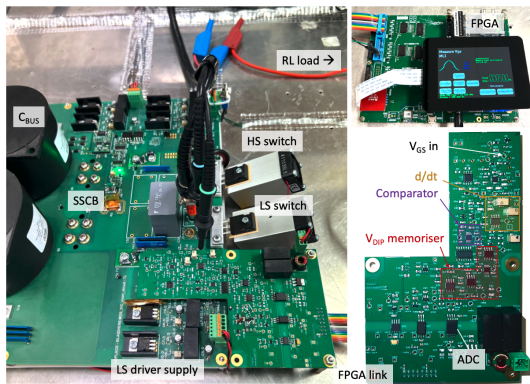


Fig. 6. 600V SiC MOSFET inverter leg power bench, controller interface, and proposed AGD inserted in the power bench

the internal capacitances of the LS switch. As depicted in Fig. 7a, V_{CMEM} correctly tracks V_{GS} and C_{MEM} stores the dip for 13 μ s. In *sample* mode, the output of the SHA V_{ADC} follows its input V_{CMEM} with a 400mV offset. Upon transitioning into *hold* mode, its output settles in 150ns to the input voltage (V_{DIP}) and holds it for 34 μ s. Simultaneously, the ADC (Δ - Σ) digitises the memorised V_{DIP} with a Sinc3 filter algorithm to obtain 16-bit precision within 20 μ s. Once the dip value is acquired, it is displayed on the GUI. This non-invasive slow turn-on only lasts for 13 μ s or 25% of the switching period. The health monitoring method is then characterised on a MOSFET under accelerated ageing. Initially, a fresh

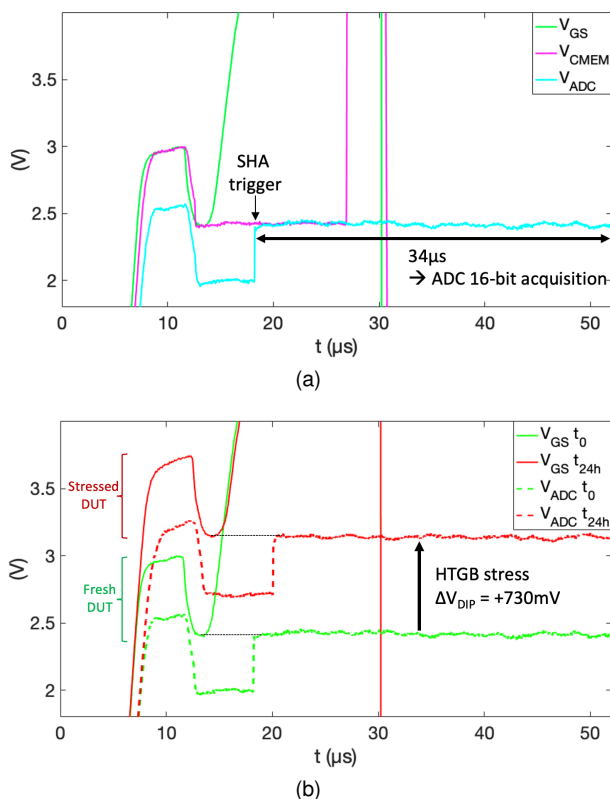


Fig. 7. V_{GS} and dip memorisation waveforms during a slow no-load turn-on (a), comparison of V_{GS} and input of the ADC V_{ADC} between a fresh (t_0) and a stressed MOSFET (t_{24h}) (b) ($V_{BUS}=600$ V, $f_{SW}=20$ kHz, $f_{MOD}=100$ Hz)

MOSFET is characterised as a reference (in green colorline in Fig. 7b). The DUT then undergoes a High-Temperature Gate Bias (HTGB) stress of $V_{GS}=35$ V, $T_{CASE}=150^\circ$ C for 24 hours. This speeds up the charge-trapping mechanism that gradually appears in normal operation. The DUT case is then cooled down to a stable room temperature of 20.5 $^\circ$ C, and re-characterised (in red colorline in Fig. 7b). This results in a V_{DIP} drift of +730mV, indicative of significant ageing, detected by the proposed AGD.

To assess the stability and reliability of the measurements, 20 consecutive slow turn-on cycles are performed. Each resulting V_{DIP} value, extracted by the FPGA and displayed on the control screen, is recorded. Under no-load conditions, the Relative Standard Deviation (RSD) of these measurements is just 0.146%, affirming the conceptual validity and measurement stability during on-line operation.

Fig. 1 depicts a possible connection of an RL load to the

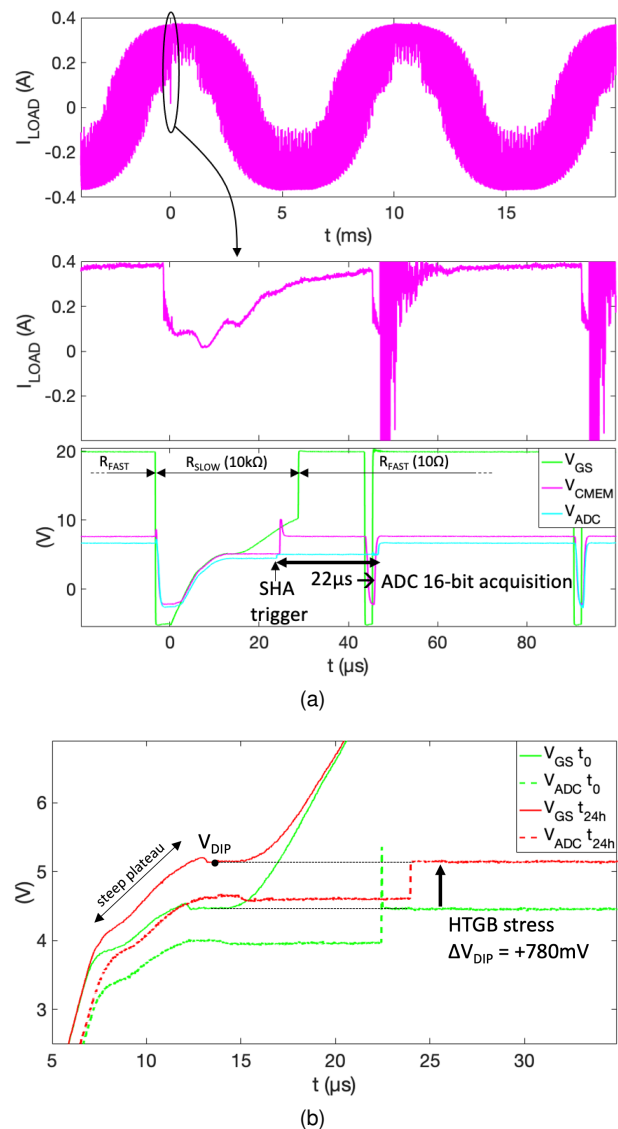


Fig. 8. Gate voltage and dip memorisation waveforms during a slow turn-on under a light load current of 370mA (a), comparison of V_{GS} and input of the ADC V_{ADC} between a fresh MOSFET (t_0) and an aged MOSFET (t_{24h}) (b) ($V_{BUS}=600$ V, $f_{SW}=20$ kHz, $f_{MOD}=100$ Hz)

midpoint of the inverter leg to characterise the proposed AGD under on-line and loaded conditions. Within a PWM frame (see Fig. 2), a slow turn-on is implemented with a circulating load current through the high-side body diode. The slow turn-on should be initiated when the load current is minimal to avoid significant distortion of the V_{GS} turn-on dynamics. Excessive load currents cause a non-flat plateau, characterised by a steep slope depicted in Fig. 8b, thereby obscuring the dip's presence. Then, the identical HTGB stress protocol is applied to a fresh MOSFET under loaded conditions. Despite a notable reduction in dip amplitude due to the influence of load current, the dip memoriser successfully extracts the dip, which is accurately transmitted to the ADC. Following the accelerated ageing stress, a V_{DIP} drift of +780mV is detected by the FPGA. The stability of the measurements under the influence of a load current is assessed with the same protocol as before. Under on-line and loaded conditions, the RSD of these measurements is 0.235%, validating the concept and reliability of the extracted V_{DIP} values.

TABLE I
OVERVIEW OF THE PERFORMANCES OF THE PROPOSED HEALTH
MONITORING SOLUTION

	before/after stress ΔV_{DIP}	V_{DIP} RSD
No-load	+730mV	0.146%
RL load	+780mV	0.235%

Tab. I shows a summary of the performances of the proposed on-line health monitoring method.

V. CONCLUSION

SiC MOSFETs are susceptible to charge-trapping phenomena in the gate oxide interface region over prolonged operation, leading to an increase in threshold voltage and power losses. A gate voltage monitoring method is introduced for on-line detection of these ageing mechanisms. This method involves extracting and monitoring a gate voltage dip. This dip is a newly identified electrical signature that reliably reflects the MOSFET's health status. The gate driver comprises two parallel channels: a low-value gate resistance buffer for normal fast switching and a high-value gate resistance buffer for selectively slowing down a specific turn-on. This turn-on slowdown is intended to induce the appearance of the dip and allow enough time for its extraction. Moreover, under a reduced drive voltage of 10V, the voltage dip approaches the threshold voltage, enabling its on-line monitoring. The proposed health monitoring gate driver is evaluated under both no-load and loaded conditions. After accelerated ageing of the MOSFETs in both scenarios, the controller effectively detects a gate voltage dip drift exceeding 700mV. This validates the functionality and sensitivity of the proposed approach in detecting ageing signatures, while ensuring robust measurement stability and repeatability during on-line PWM operation.

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