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***Operando* electrical biasing TEM experiments of Ge-rich GST thin films with FIB sample preparation**

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Abstract

Ge-Sb-Te (GST) ternary alloy is the core material for phase-change memory (PCM). Compared with Ge₂Sb₂Te₅ (GST-225), Ge-rich GST (GGST) has a higher crystallization temperature (about 400°C) and thereby an improved thermal stability. In this paper, we propose a methodology dedicated to studying the phase changes by operando transmission electron microscopy (TEM). The methodology combines focused ion beam (FIB) specimen preparation and injection of electrical pulses for *in-situ* studies. We show how the microstructure is correlated to the electrical switching dynamics in GGST nanobridges. The electrical pulse modification, the electrochemical migration, local current density, void formation and the corresponding switching mechanism are discussed.

25 **Key words:** GGST, PCM, crystallization, *Operando* electrical biasing TEM, phase
26 change

27 1. Introduction

28 The fast switching speed, moderate programming currents and good scalability render Ge-
29 Sb-Te chalcogenides (GST) a good candidate for the active material in non-volatile random-
30 access memory (RAM) [1-5] and neuromorphic memory devices [6-9] for cloud-computing
31 and artificial-intelligence applications. GST alloys undergo a reversible amorphous-to-
32 crystalline phase transition that can be controlled by laser pulses or the Joule heating generated
33 (inside the GST itself) by injecting electrical pulses. The RESET process for devices, in which
34 GST alloy is melt-quenched from the crystalline state after a short-duration high-energy pulse,
35 produces an amorphous state in the active region. During the SET process, the amorphous
36 region is recrystallized when the GST alloy is heated to a temperature between its melting point
37 and the crystallization temperature. The phase transformation is accompanied by a strong
38 variation of the electrical resistivity up to 2-3 orders of magnitude. Within a PCM cell, the
39 resistance can vary from several k Ω in its crystalline state (SET) to 10⁶ Ω in its amorphous state
40 (RESET).

41 The most widely used and studied chalcogenide alloy is GST-225, the crystallization of which
42 occurs at 150°C or 350°C depending on whether it was originally in its metastable cubic GST
43 (*c*-GST, space group: Fm-3m) phase or hexagonal GST (*h*-GST, space group: P-3m1) phase,
44 respectively [10]. While GST-225 PCM cells can be reversibly switched reliably and for great
45 many cycles, the low crystallization temperature (from amorphous to *c*-GST) has limited their
46 use in neuromorphic and automotive applications.

47 Various solutes (Ge [11-15], C [16, 17], O [18], Bi [19], Sb [20], Se [21], Sm [22], Ti [23],
48 Ga [7], N [24-28]) have been added to tailor the desired phase change characteristics, among
49 which GGST, with additional Ge, is widely used owing to an increased crystallization
50 temperature and thus a better thermal stability. The improved RESET retention in GGST
51 facilitates its automotive-grade application [29]. GGST thin films are usually deposited on a
52 substrate at low temperature by physical vapor deposition (PVD), by which almost any
53 stoichiometry can be accommodated. Most studies focus on GGST with Ge contents up to 55
54 at.% [30]. Up to now, isothermal annealing analyses performed by X-ray diffraction (XRD)
55 [14], TEM [13-15], *in-situ* heating TEM [27, 31] and *in-situ* synchrotron XRD [15, 26] have

56 revealed an enhanced thermal stability in GGST, in which Ge diffusion and phase separation
57 occur followed by the *c*-GST formation. In contrast, full understanding of electrical switching
58 dynamics, especially the role of extra Ge content, is apparently missing for GGST.

59 *Operando* TEM aims to provide real-time observation of the phase change dynamics for
60 chalcogenide PCMs and devices. A fundamental understanding of nanostructure evolution
61 during electrical switching is beneficial to monitor future device design. In GST-225, previous
62 *operando/in-situ* electrical biasing TEM experiments featuring various device architectures,
63 including nanowires [32-34], nanobridge [35], dome-shaped [36], confined memory devices
64 [37, 38] and thin film devices [39, 40], have given critical insights into the switching reliability
65 and the “set-stuck” failure mechanism of GST-225. Upon switching, threshold switching was
66 observed in GST-225, in which different initial nanostructure distributions (*i.e.* crystalline and
67 amorphous domains) could lead to distinct threshold switching processes [35]. In the molten
68 state of dome-shaped or confined memory devices, strong electromigration is responsible for
69 void formation and ultimate failure [36-38].

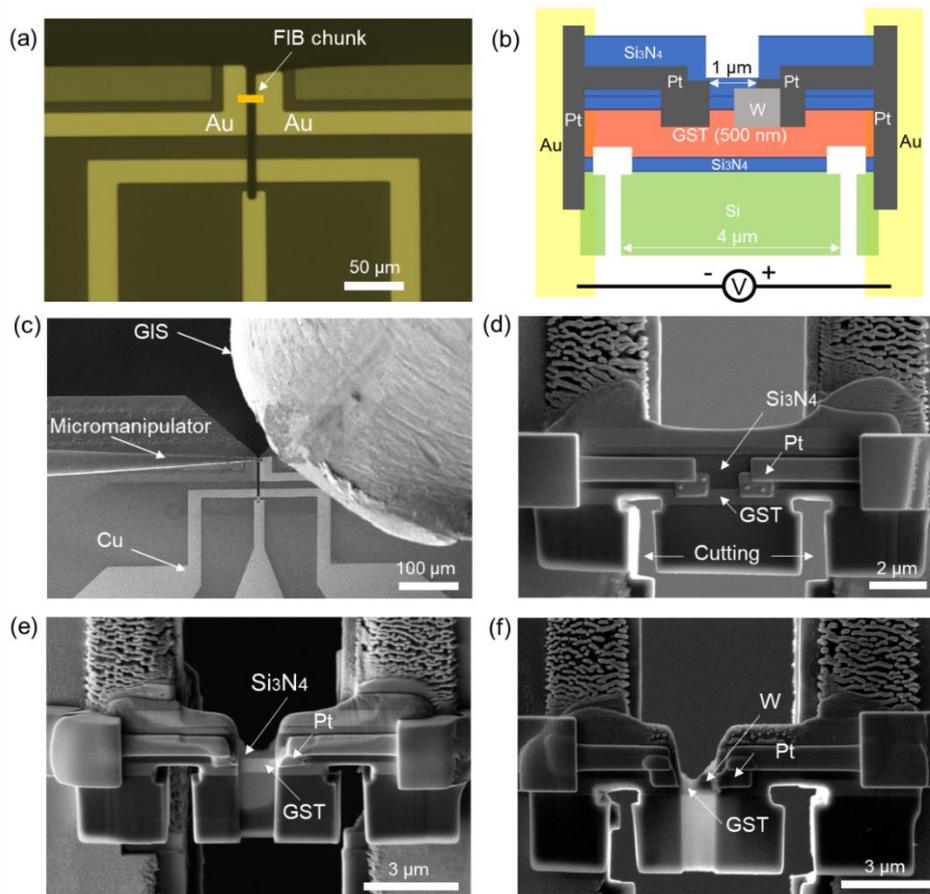
70 In the present work, by developing a novel methodology using dedicated FIB specimen
71 preparation, we have successfully observed the reversible electrical switching behaviors in
72 GGST nanobridge structures during *operando* electrical biasing TEM experiments.

73 **2. Experimental section**

74 A 500 nm-thick GGST film (>30 at.% Ge) was fabricated on Si (100) wafer using physical
75 vapor deposition. A 10 nm-thick Si₃N₄ was deposited on the Si substrate prior to GGST growth
76 to electrically isolate the GST layer to the substrate, and after the growth to protect the surface
77 from oxidation. The final bottom-to-top stacking sequence is thus: Si substrate/10 nm Si₃N₄/500
78 nm GGST/10 nm Si₃N₄. Samples cut from the wafers were annealed in a horizontal Carbolite
79 furnace with flowing N₂ gas at 180-550 °C for 10 min, 30 min or longer period (12 h). The N₂
80 gas avoids the reaction with air during thermal annealing. XRD was performed on a Bruker D8
81 Discover diffractometer with a 2D Vantec 500 detector. The X-ray analysis used a Co K_α
82 emission with a wavelength of 1.79 Å. TEM experiments for high-resolution imaging and
83 electron diffraction were carried out in a Tecnai F20 instrument (ThermoFisher Scientific) at
84 an accelerating voltage of 200 kV. Cross-sectional thin foils were prepared by site-specific lift-
85 out procedure using a Helios Nanolab 600i dualbeam FIB-SEM instrument (ThermoFisher

86 Scientific). XRD and TEM analyses help to identify the microstructure and phase distribution
87 prior to *operando* TEM experiments.

88 Delicate FIB sample preparation, by which a nanobridge GGST device is shaped on a
89 commercialized Hummingbird chip, is the key to our *operando* electrical biasing TEM
90 experiments. Fig. 1(a) and (b) display the local structure of Hummingbird chip and the designed
91 specimen architecture, which represent an active GGST region of $500 \times 500 \text{ nm}^2$. Prior to FIB
92 sample preparation, an approximately 800 nm-thick Si_3N_4 was deposited to protect the bulk
93 surface (with a scale of $5 \times 8 \text{ mm}^2$). The radio frequency (RF) sputtering deposition of Si_3N_4
94 was conducted in a Vinci PVD-4 magnetron sputtering machine. The lift-out of the chunk was
95 performed at a stage tilting angle of 52° with the aid of the micromanipulator, and, subsequently,
96 the chunk was mounted between Au electrodes of the Hummingbird chip, as illustrated in Fig.
97 1(c). During the lift-out procedures, gas injection system (GIS) was used to create Pt deposition
98 between the contacts. Next step is to ensure the electrical circuit path and to thin the chunk. To
99 avoid leakage current from additional electrical pathways (besides the GGST path), we pre-
100 thinned the chunk to 500 nm and then undercut the Si substrate from both sides, as shown in
101 Fig. 1(d). Deposition of Pt was used to shorten the effective length of the GGST circuit path to
102 about 1 μm . Then the chunk was milled to a thickness of about 60 nm, shown in Fig. 1(e), with
103 the milling voltage gradually decreasing from 30 kV to 5 kV. Through an extra W deposition
104 from GIS in SEM view, the effective electrical pathway across the GGST nanobridge was
105 further reduced to 500 nm, as seen in Fig. 1(f). The final cleaning was carefully performed at 2
106 kV to minimize beam damage and surface contamination. After FIB sample preparation,
107 encapsulation with about 12 nm Si_3N_4 prevents the GGST evaporation during *operando*
108 electrical biasing TEM observations.



109

110 **Fig. 1** Designed specimen architecture and FIB sample preparation procedures for operando
111 electrical biasing TEM experiments. (a) Local structure of Hummingbird chip with a FIB-
112 extracted rectangular chunk in orange color. (b) Designed specimen structure; (c) Mounting
113 of the extracted chunk onto the Au contacts of hummingbird chip using a micromanipulator;
114 Cutting-off on the Si substrate; (e) Step-by-step thinning of the specimen; (f) Final
115 specimen structure with a reduced region of interest ($500 \times 500 \text{ nm}^2$) due to extra W
116 deposition. In (d), the cutting-off on the Si substrate avoids extra electrical circuit paths
117 during operando electrical biasing TEM experiments.

118 *Operando* electrical biasing TEM experiments were performed on a Hitachi HF3300-C
119 (I2TEM) microscope operating at 300 kV dedicated to electron holography and *in-situ*
120 experiments. It is equipped with a cold-field emission gun for optimal brightness, a high-speed
121 $4\text{k} \times 4\text{k}$ camera (OneView, Gatan Inc.), and an imaging aberration corrector (BCOR, CEOS)
122 allowing a spatial resolution of 0.5 nm in Lorentz mode and 0.08 nm in high-resolution mode
123 [41]. A description of the commercial *in-situ* biasing sample holder (Hummingbird), as well as
124 the supporting chip (Hummingbird), can be found in Supplementary Fig. S1. Recently, by using
125 the same Hummingbird chip and its compatible holder, we have also realized the *in-situ*
126 electrical switching of an embedded PCM device [42]. Prior to *operando* TEM experiments,
127 the electrical measurements were performed using a Keithley 2635B source meter. The

128 electrical pulses were injected from a Keithley 4200A-SCS parametric analyzer with a time
129 resolution of 20 ns.

130 **3. Results and discussion**

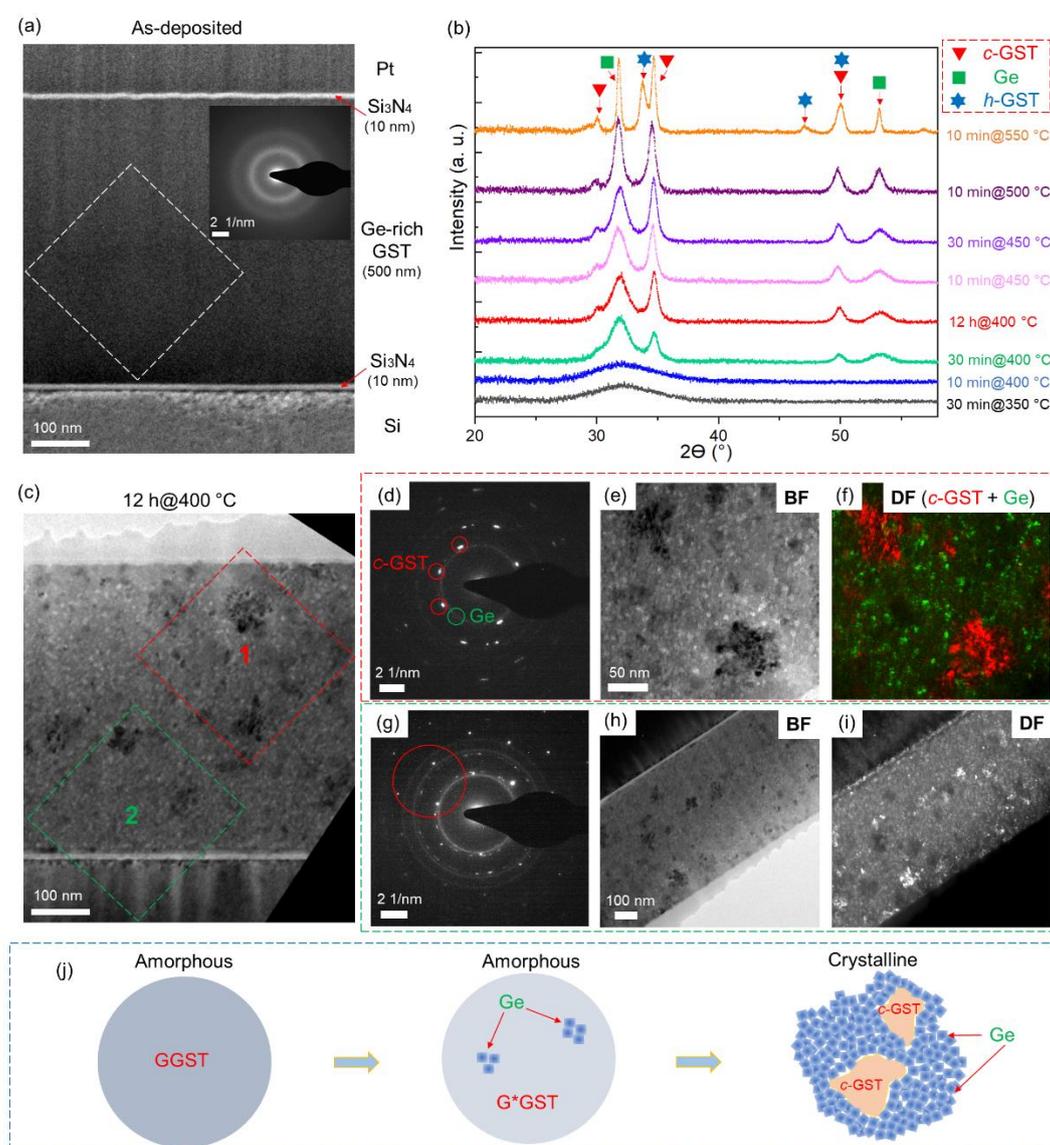
131 **3.1 XRD and *ex-situ* TEM characterizations**

132 Fig. 2(a) presents the stack of the as-deposited layers: the 500 nm-thick GGST layer is clearly
133 visible between the 10 nm-thick insulating Si₃N₄ layers to isolate GGST from electrical and
134 thermal conduction. The as-deposited GGST is in the initially amorphous state according to the
135 inserted selected area electron diffraction (SAED) pattern, as appeared in Fig. 2(a). Fig. 2(b)
136 plots the XRD spectra after annealing at elevated temperatures. The TEM images of the
137 microstructure and corresponding SAED patterns after annealing at various temperatures are
138 also given in Fig. 2(c) to Fig. 2(i) and in Supplementary Fig. S2.

139 We observed no phase change below 400 °C. As expected, diamond cubic Ge (space group:
140 Fd-3m) and metastable rocksalt *c*-GST phases are formed after annealing at 400 °C for over 30
141 minutes (or at higher temperatures). After annealing at 400 °C for 12 h, the microstructure is in
142 a crystalline state comprising *c*-GST and Ge phases, as shown in Fig. 2(c) and (d). According
143 to the corresponding bright field (BF) and dark field (DF) images in Fig. 2(e) and (f), the *c*-
144 GST grains are homogeneously distributed into the Ge matrix. These *c*-GST grain size can
145 reach a diameter of about 70 nm. In contrast, Ge phase has fine grain size (typically smaller
146 than 9 nm in diameter). The high-resolution images for *c*-GST and Ge grains are given in
147 Supplementary Fig. S3. Fig. 2(g)-(i) present the SAED pattern and the corresponding BF and
148 DF images, in which both BF and DF ones have a broad field of view in order to show the
149 microstructure in the whole GGST layer. Numerous large crystalline grains, with white contrast,
150 are evident in the DF image Fig. 2(i). The DF contrast will thus be used to identify the
151 microstructural variation in the region of interest during *operando* electrical biasing TEM
152 observations. When increasing the temperature up to 550 °C, the *h*-GST phase appears after an
153 annealing of 10 min with massive voids.

154 Let us go back to the phase transition for an annealing temperature of 400°C; we first
155 observed the diffusing Ge (111) peak after 10 minutes, and then sharper Ge peaks and newly
156 formed *c*-GST peaks appear in 30 minutes. This infers that Ge grains are created prior to *c*-GST,
157 and that the GGST crystallization is mediated by Ge diffusion and phase segregation. It
158 proceeds via the homogeneous nucleation of grains followed by their growth. Ge grains
159 nucleate first and then *c*-GST phase forms and gradually evolves to a large size (via the so-

160 called “Ostwald ripening” [43]) when the surrounding composition is proper. The
 161 crystallization process at 400 °C is schematically depicted in Fig. 2(j). The amorphous GGST
 162 firstly evolves to an intermediate state (G^*GST), an amorphous microstructure with the
 163 exclusion of some Ge to form cubic Ge grains, and then transforms to a mixture of Ge and c -
 164 GST. Our observations agree well with the proposed progressive phase separation process of
 165 cubic Ge and subsequent formation of c -GST during isothermal annealing of GGST [15].
 166 Besides, the formation of Ge grains (at about 400 °C or below) was also reported to benefit
 167 from the prior formation and subsequent dissolution of intermediate Pnma GeTe structure [15].
 168 Although Ge enrichment in GGST potentially retards its crystallization process, it guarantees
 169 the SET programming in working cells [44].

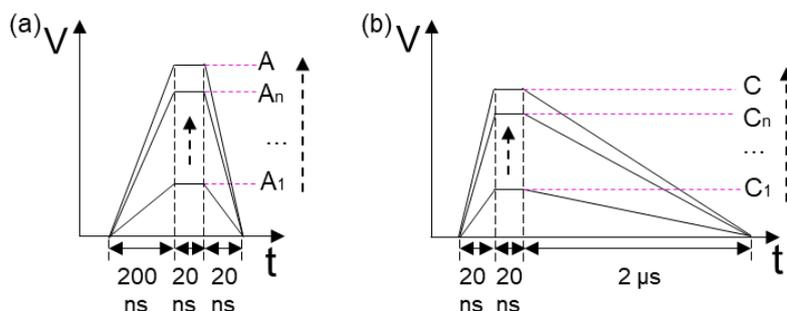


170
 171 **Fig. 2** (a) Amorphous 500 nm-thick GGST layer in the as-deposited state. (b) XRD spectra of the
 172 GGST thin films after annealing (Co target, $\lambda = 1.79 \text{ \AA}$). (c) Microstructure after annealing at 400 °C

173 *for 12 h. (d)-(f) SAED pattern, BF and DF images from region 1 in (c). (g)-(i) SAED pattern, BF and*
174 *DF images from region 2 in (c). (j) Schematic illustration of crystallization process at 400 °C. In (a),*
175 *the inset SAED pattern shows the amorphous structure of the as-deposited GGST. The BF and DF*
176 *images in (e) and (f) have an about 135° clockwise rotation from the selected region 1 in (c). And, in*
177 *(f), the c-GST phase and the Ge phase are marked in red and green, corresponding to the selected red*
178 *and green spots in (d), respectively. In comparison to region 2 in (c), the BF and DF images in (e)*
179 *and (f) have an about 135° clockwise rotation and also a broad field of view in order to show the*
180 *microstructure of the whole GGST layer. And, in the DF image (i), some large crystalline grains, with*
181 *bright contrast, are evident. This image was captured with a large objective aperture being applied as*
182 *marked in red solid circle in (g). In (j), G*GST represents the intermediate state of the GGST material,*
183 *with some grown Ge grains but prior to c-GST formation.*

184 3.2 Operando electrical biasing TEM observations

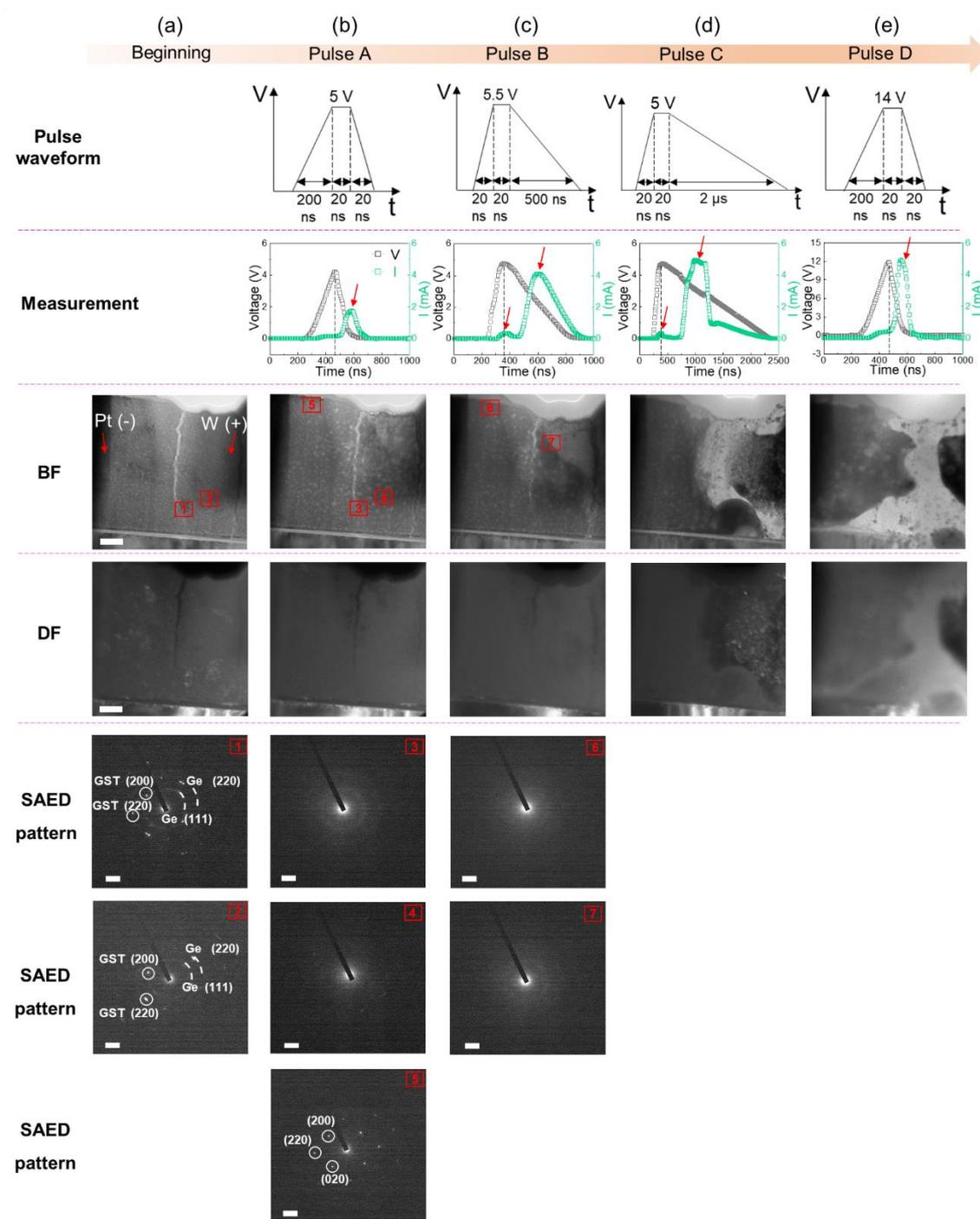
185 *Operando* electrical biasing TEM experiments were performed on the FIB-prepared
186 specimen from the annealed material at 400 °C for 12 h. Once the dedicated FIB preparation
187 mastered, an important work was realized to adapt the shape of the electrical pulses for
188 controlling the phase transformation. The pulse waveforms for RESET and SET are shown in
189 Fig. 3. Considering a relatively long GGST bridge path (about 500 nm), and consequently an
190 important electrical resistance, a large voltage amplitude was required. In order to ensure a
191 steady Joule heating accumulation and a controlled temperature rise, our pulsing strategy was
192 to limit the peak voltage duration and then gradually increase the pulse amplitude until
193 switching. The peak voltage duration was 20 ns, and the pulse interval about 10 s. For RESET,
194 the rise edge was 200 ns, and, for SET, a longer fall edge up to 2 μs was adopted. The use of a
195 parametric analyzer for the electrical pulses allow to measure the current flowing through the
196 nanobridge sample during each pulse.



197
198 **Fig. 3 Pulse waveforms for (a) RESET and (b) SET. Pulse A and pulse C indicate those**
199 **induce the phase changes, and pulses A_n and C_n correspond to the last ones that have not**
200 **switched the microstructure.**

201 Fig. 4(a) shows the active region of interest of about $500 \times 500 \text{ nm}^2$, and the W electrode
202 which is positively biased. A slight fracture is present, but the remaining part allows to have an
203 electrical connection from one electrode to the other. GGST is in the initially crystalline state,
204 and some c-GST grains, with white contrast, are clearly observed in the DF image in Fig. 4(a).
205 The injected electrical pulses, as well as the measured current and voltage profiles, are also
206 given in Fig. 4. After injecting a critical electrical pulse (pulse A), with 5 V amplitude, 200 ns
207 rise, 20 ns duration and 20 ns fall, most crystallites have transformed to amorphous state, as
208 revealed by the DF images and SAED patterns in Fig. 4(b). And the corresponding high
209 resolution TEM (HRTEM) images for those selected regions, before and after phase change,
210 are shown in Supplementary Fig. S4. The residual crystalline region (marked by “5” in Fig.
211 4(b)) is revealed by the SAED pattern, and its HRTEM image can be referred to Supplementary
212 Fig. S5. Meanwhile, voids were formed in the matrix, and the ones share larger size appear
213 close to the W electrode.

214



215

216 **Fig. 4** Microstructure evolution (in BF, DF images and SAED patterns) with the corresponding
 217 applied electrical pulses using operando electrical biasing TEM methodology. (a) Initial crystalline
 218 state. (b)-(e) After the switching electrical pulses (A, B, C and D). The specimen has an active region
 219 of interest of about $500 \times 500 \text{ nm}^2$, with the Pt (cathode) and W (anode) electrodes from both sides.
 220 In (b) & (c), SAED patterns of the selected regions, marked in red and green, respectively, indicate a
 221 crystalline to amorphous phase change in this critical region (marked by "5") after the pulse B. In
 222 (b)-(e), the current peaks, occurring at fall edges, are marked by red arrows. The scale bars for the
 223 BF/DF images and the two SAED patterns are 100 nm and 2 1/nm, respectively.

224 The subsequent electrical pulses were intended to recrystallize the GGST, since, after pulse
225 A, the microstructure is amorphous except for a critical region at the edge. Surprisingly, as seen
226 in Fig. 4(c), this edge region is completely amorphized after an electrical pulse (pulse B) with
227 5.5 V amplitude, 20 ns rise, 20 ns duration and 500 ns fall. As seen in the inserted SAED pattern,
228 the residual *c*-GST crystallite has been amorphized. Another striking phenomenon is the
229 nanovoid rearrangement, in which a large one forms close to W electrode while the others seem
230 to shrink. A fully amorphous structure after pulse B infers that a 500 ns fall edge is insufficient
231 for the GGST crystallization in our specimen geometry.

232 The size effect of the GGST bridge and electron percolation could explain the nanostructure
233 evolution after pulse B. In contrast to smaller bridge or confined PCM cells, a less uniform
234 microstructure was obtained in our bridge specimen after a switching pulse A, since the
235 accumulated Joule heating is insufficient to melt the whole GGST bridge and thus forms a
236 mixed amorphous-crystalline structure. During subsequent pulse B, the electron conduction
237 follows specific percolation paths and the residual crystalline region melts and is switched to
238 amorphous. Meanwhile, other regions re-melted and became amorphous. This pulse B
239 demonstrates the value of *operando* TEM analysis and reveals the complex correlation between
240 crystallinity, specimen geometry and electrical pulses.

241 Another type of electrical pulse (pulse C) with 5 V amplitude, 20 ns rise, 20 ns duration and
242 2000 ns fall, successfully initiated the crystallite formation, as seen in Fig. 4(d). However, the
243 specimen architecture has been modified after the pulse C, and a small part of GGST (adjacent
244 to W electrode) has been removed. The last electrical pulse, pulse D in Fig. 4(e), has 14 V
245 amplitude, 200 ns rise, 20 ns duration and 20 ns fall. The microstructure seems to be in an
246 amorphous state, but the specimen architecture is destroyed.

247 From the electrical measurements performed thanks to the parametric analyzer during the
248 injected pulses, we noticed that most current profiles show two peaks, particularly for pulse B
249 and pulse C. These current peaks are marked by red arrows in Fig. 4. The 1st current peaks
250 always present low values (hundreds of μA) and seem to correspond to an inductive current
251 created inside the instrumental set up (cables, sample holder, chip, ...) due to the rapid increase
252 of voltage. The 2nd ones delay a certain time from the voltage peaks with much higher values
253 of several mA. The measured peak currents for those switching pulses (A, B, C and D) and their
254 last ones before switching (A_n , B_n , C_n and D_n) are listed in Table 1. A detailed comparison of
255 the switching pulses and their previous ones before switching could be seen in Supplementary
256 Fig. S6, Fig. S7, Fig. S8 and Fig. S9, respectively. For those switching pulses, the 2nd current

257 peaks give values 1.8, 4.0, 4.9 and 4.9 mA, respectively for A, B, C and D. This infers an
258 approximate peak current density of (11.2 ± 5.2) MA/cm², given a specimen thickness of 60 nm,
259 in the order of magnitude estimated from the sample preparation. The local current density is
260 in the same range of magnitude than the confined GST-225, with a value of 9 MA/cm² during
261 SET process [38]. Table 1 also lists the delay times of the 2nd current peaks from voltage peaks
262 (or 1st current peaks), during which a continuous accumulation of Joule heating leads to the
263 melting and subsequent phase change of GGST. It is worth of mentioning that, here, the current
264 delay times between peaks are not due to the instrumental measurement delays or unavoidable
265 parasitic effects, the latter of which may contribute to a time-scale from hundreds of ps to
266 several ns [45].

267 **Table 1 Measured current peaks and delay times between the 2nd current peak and the voltage**
268 **peak**

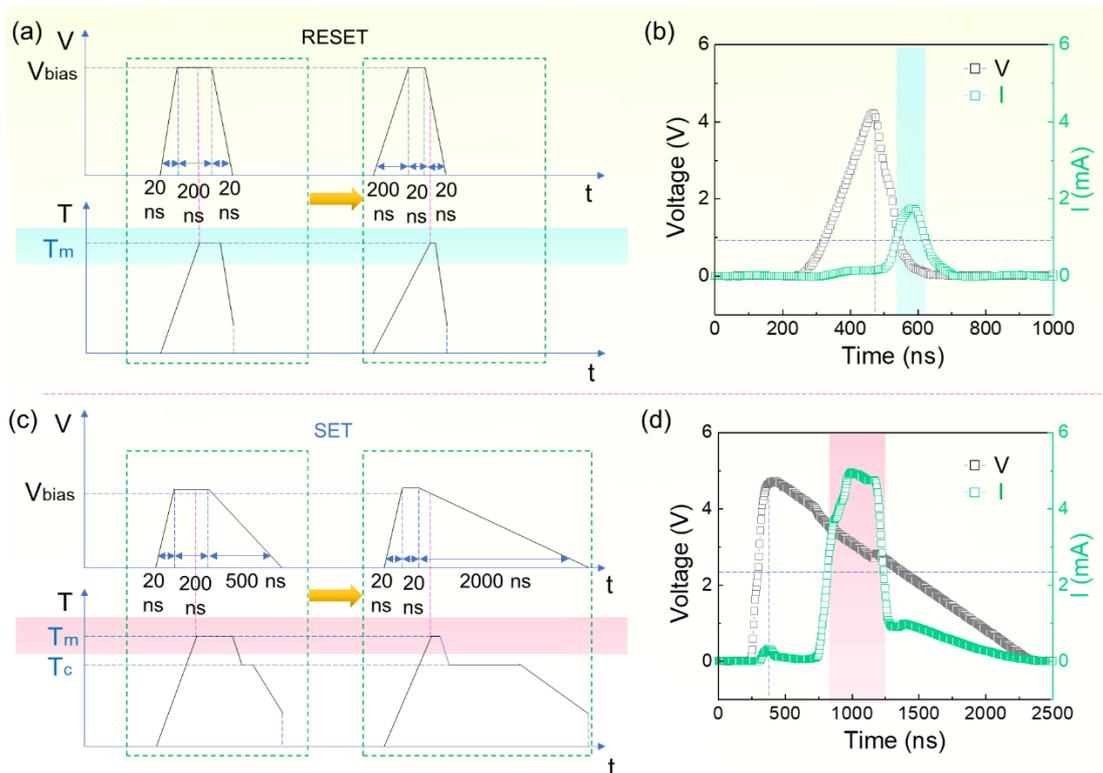
	1 st current peak (μ A)	2 nd current peak (μ A)	Delay time (ns)
Pulse A_n	125	156	115
Pulse A	146	1800	115
Pulse B_n	352	-	-
Pulse B	356	4000	250
Pulse C_n	322	-	-
Pulse C	323	4900	605
Pulse D_n	489	297	90
Pulse D	418	4900	90

269 Notes: “-” means that no clear peak or delay time is detected.

270

271 3.3 Phase change during SET and RESET

272 In general, Joule heating is responsible for the phase change of GST chalcogenide. However,
273 excessive Joule heating, accumulated upon a long duration pulse at high voltage, may instantly
274 disintegrate the GGST nanobridge and result in destructive switching. We presented some
275 failure examples in Supplementary Fig. S10, in which (1-1.5) μ m-length GGST nanobridges
276 were fabricated. This is the reason why the electrical pulse waveforms were modified for
277 present GGST nanobridge specimen, with a 500 nm-length electrical path. Fig. 5 schematically
278 illustrate the modified electrical pulses and the corresponding temperature variations during
279 SET and RESET processes.



280

281 **Fig. 5 Illustrations of the modified electrical pulses for operando electrical biasing TEM experiments.**

282 **(a) RESET process. (b) Measured voltage and current profiles during pulse A. (c) SET process. (d)**

283 **Measured voltage and current profiles during pulse C. Here, V_{bias} , T_m and T_c represent the pulse**

284 **voltage, melting temperature and crystallization temperature, respectively.**

285 During RESET process in Fig. 5(a), by limiting the peak duration time (20 ns) and increasing
 286 the rise time (200 ns), the duration of the microstructure in its molten state could be controlled.
 287 This helps the phase change dynamics to be followed and also inhibit excessive Joule heating
 288 at a high voltage. After the switching pulse A shown in Fig. 5(b), the current peak occurs at the
 289 fall edge, which ensures a crystalline to amorphous switching without destroying the bridge
 290 structure. In Fig. 5(c), during SET process, the idea is to ensure the smooth crystallization in
 291 the GGST nanobridge. The high crystallization temperature (about 400 °C) in GGST plays an
 292 important role in its solid-state phase transformation or the SET process, in which case a
 293 reduced peak duration time (20 ns) and a prolonged fall time (2000 ns or even longer) were
 294 applied to avoid long stay at peak voltage in its molten state and also to fulfill the retarded
 295 crystallization of a heterogeneous microstructure. The fact that, after the switching pulse C (Fig.
 296 5(d)) for the SET process, the bridge structure has been modified seems indicated that the GGST
 297 nanobridge indeed experience melting before its crystallization.

298 For both SET and RESET processes, melting happens during their fall edges instead of peak
299 voltage regime. If we define the width of half current peak as the melting period, then the
300 melting periods are 80 ns and 370 ns, respectively, for SET and RESET processes of our GGST
301 nanobridge. For RESET process, this melting duration may be further reduced by changing the
302 fall edge to a two-step cooling edge.

303 Compared with the voltage and current profiles in Fig. 5(b) and (d), we noticed the RESET
304 process undergoes a threshold switching while the SET process does not. In the former case,
305 after reaching the peak voltage, the electrical resistivity was reduced and thus the measured
306 current continuously increases at the fall edge until melting. With the initially polycrystalline
307 structure, the conduction occurs via the emission of carriers from defects energetically located
308 very close to one of the bands, with the activation energy depending on programming conditions
309 [46, 47]. The threshold switching processes have also been widely reported in GST-225 [35,
310 48-51], in which the electronic switching occurs via an abrupt increase of the current density at
311 a critical electric field. In our GGST nanobridge, the threshold field is estimated to be about 10
312 V/ μm , which is in the same order of magnitude than that in GST-225 nanobridge, with a value
313 of 4 V/ μm [35]. During RESET process, a higher threshold voltage was also observed from I-
314 V sweeping in GGST cells compared to the ones of GST-225 [52]. This infers that GGST may
315 achieve a higher reading voltage. By contrast, the measured current of the SET process starts
316 to decrease firstly at the fall edge. It then rises and the GGST starts to melt after reaching the
317 critical Joule heating. Consequently, the SET process is likely to be dominated by Joule heating.

318 During reversible phase change or in the molten state, there is a considerable electrochemical
319 migration along with void formation and evolution [38]. As reported for GST-225, the nanovoid
320 formation can be ascribed to the coalescence of Te vacancies [53], the motion of cations and
321 anions (Ge^+ , Sb^+ and Te^- ions) [54] and the material stress resulting from volume variations
322 during phase transformations [55]. The Te^- ions move towards the positively biased electrode,
323 while Ge^+ and Sb^+ ions migrate towards the inverse direction. In GST-225, strong Sb^+
324 electromigration was proven to be the prominent factor for nanovoid formation, since its
325 velocity was estimated about 1.7 times faster than Ge^+ or Te^- migration [36-38]. In the present
326 GGST nanobridge, electromigration leads to the formation of nanovoids during pulse A. The
327 initial nanovoid distribution may be affected by the thermal annealing at 400 °C considering
328 the (Ge + *c*-GST) heterostructure. Upon pulse B, these nanovoids evolve to a larger one adjacent
329 to W electrode. This large nanovoid may play a significant role on the temperature distribution
330 of GGST nanobridge. Indeed, as the size of void grows, the Joule heating is confined to the

331 narrow channel next to the void, resulting in a higher peak temperature [38]. This peak
332 temperature distribution may explain why some GGST materials, originally close to the
333 nanovoid, experience a slight evaporation after pulse C.

334 **4. Conclusion**

335 The *operando* TEM observations of GGST nanobridge provides an overview of the dynamic
336 nanostructures upon electrical switching. This methodology could be a powerful aid in
337 engineering electrical pulse waveforms for a specific device geometry. The dedicated FIB
338 specimen preparation allows the elaboration of GGST nanobridges from bulk materials or to
339 extract the PCM cell, without any lithography patterning. Furthermore, our *operando* technique
340 could be applied to other commercial electronic devices, or materials with thermal phase
341 transition, by slightly adapting the FIB preparation workflow. Furthermore, electrical
342 measurements can be correlated with complementary scanning TEM techniques (EDS or EELS)
343 for an insightful understanding of structural, chemical and electrical properties for individual
344 devices at the nanometer scale.

345 For the studied phase change material, *i.e.* GGST nanobridges, presented in this article, the
346 main conclusions are:

347 (1) During thermal annealing, the amorphous phase of GGST transforms to a mixture of cubic
348 Ge and *c*-GST phases at 400 °C, and Ge forms prior to cubic GST-225. After annealing at
349 400°C for 12 h, *c*-GST has a larger grain size while Ge has a finer size.

350 (2) The reversible phase changes of GGST nanobridges were observed using *operando* (*in situ*
351 electrical biasing) TEM experiments. The RESET process exhibits a threshold switching,
352 whereas the SET process does not. The peak current densities were measured to be (11.2 ± 5.2)
353 MA/cm² during SET and RESET processes, which is in the same order of magnitude as
354 confined GST-225. GGST presents a sluggish crystallization characteristic, in which longer
355 retention is required for its crystallization. Owing to strong electrochemical migration, some
356 nanovoids were formed in GGST nanobridge and evolve with following electrical pulses.

357 (3) During electrical switching, the GGST nanobridges indeed experience melting before
358 crystallization, and instant explosions could occur under long stay at relatively high switching
359 voltages. To avoid a melting at high voltages, the electrical pulse waveforms were modified
360 and, accordingly, the switching current peaks occur in the fall edge for both SET and RESET

361 processes, which better controls the continuous Joule heating accumulation and phase change
362 dynamics.

363 (4) Our *operando* electrical biasing TEM observations provide a direct route to understand
364 dynamic nanostructures upon electrical switching in GGST alloys, which could aid in device
365 design.

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376 **Declaration of competing interest**

377 The authors declare that they have no known competing financial interests or personal
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