PWM Strategy for the Cancellation of the Common Mode Noise Generated in a Multicell DC–AC Converter

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***Abstract*—A new control law of an Input Parallel Output Serie DC-AC multi-cell converter is proposed to cancel the CM noise while keeping the DM noise low. The control law called Interleaved Symmetrical Unipolar respects the conditions studied and detailed in this paper to achieve CM noise cancellation. The conditions are generalized whatever an even number of cells in series. The results are validated against experiments and show reduction of the CM choke volume in comparison to a conventional Interleaved Bipolar control law.**

***Index Terms*—DC-AC inverter, electromagnetic compatibility, pulse width modulation, passive filters**

I. Introduction

THE need to mitigate the climate change by reducing CO_2 emissions has put the electrical energy to the forefront of the considered solutions. As a consequence, Direct-Current to Alternating-Current (DC-AC) step-up bidirectional efficient converters are of great interest for connecting, for example, storage batteries to the grid for applications such as electric mobility, remote application and renewable energy storage. At the same time the deployment of all these converters should not create rebound effects notably on the raw material depletion, and on the stream of Waste from Electrical and Electronic Equipment (WEEE) [1].

One way to tackle these challenges is to use high power density and efficient multi-cell converters [2]. Indeed, their use shows a great reduction of the overall volume of the magnetic components for output and Differential-Mode (DM) filtering, as demonstrated in [2]–[4]. In addition, their intrinsic modularity could be a lever to increase their circularity [5] while reducing WEEE by reusing and/or refurbishing conversion cells for second hand applications. But to harness these potential advantages these converters need to pass EMI standards. Although the DM part of the problem has been already addressed several times, the Common-Mode (CM) part is less studied.

One of the main challenges that comes with the multi-cell approach is the multiplication of switching potentials (several by cell) that excite the multiple parasitic capacitances to ground and mitigation at the output of the converter by a bulky CM filter is here counterproductive in term of overall mass and volume. The noise should be limited at the source and its propagation kept inside the multicell converter.

CM cancellation and balancing techniques, also called CM recycling, have been extensively studied in the past for DC-DC converters [6]–[8], motor drives [9], Power Factor Correction (PFC) inverter [10], three phases back-to-back inverters [11]. This technique can be also applied to multi-cell power converters. Three phases multicell converters with Space Vector Pulse Width Modulation (SPWM) can achieve CM cancellation thanks to Zero CM Vectors [12]–[14]. These modulation schemes are not applicable for single-phase systems. The impedance balancing technique has been applied successfully for two cells singe-phase Cascaded H-Bridge (CHB) in [15], but this technique is not sufficient for multi-cell CHB. A symmetrical (or mirror) bridge phase shift modulation has been proposed in [16] to reduce the generated CM noise but at the expense of an increase of DM current ripple.

The goal of this paper is to propose a new pulse width modulation (PWM) strategy for the cancellation of the CM noise generated by a multi-cell single-phase DC-AC converter while keeping low the AC side output current ripple thanks to interleaving. The outline of this paper is as follow: in the Section II the main principles of CM cancellation and balancing techniques are recalled and applied to the topology of each cell and of the multi-cell converter. In Section III a new control strategy is proposed to mitigate CM noise emissions and to keep output current ripple similar with respect to the number of interleaved levels, in Section IV experimental validation is performed and the gain on the CM filter volume is demonstrated, finally Section V concludes this article.

II. Impedance Balancing in a Multi-Cell Converter Toward CM Cancellation

This section deals with the impedance balancing of the converter to enable CM cancellation by control strategy which is explained in Section III. The principle of work of CM cancellation is recalled, then the symmetries of the DC-AC cell and of the multi-cell converter are shown.

A. CM cancellation principle of work

The principle of work of CM cancellation in a converter chain is described in [6], [7] and recalled in the Fig. 1 where

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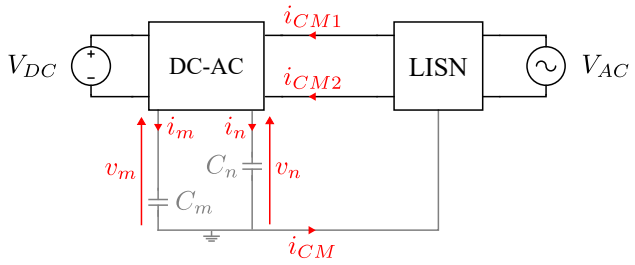

Figure 1. Principle of work of the CM cancellation.

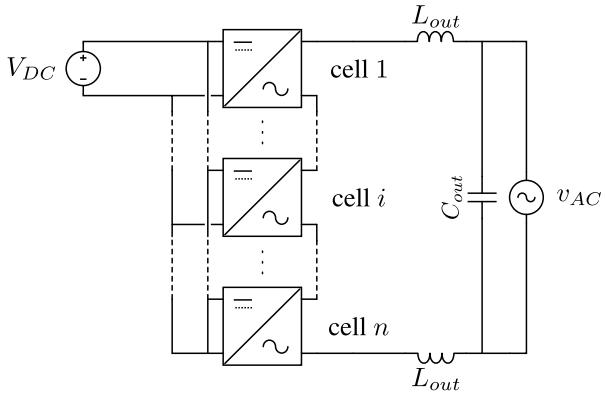

Figure 2. Circuit topology of an IPOS PCA with n cells.

the CM current is defined by the following equations:

$$i_{CM} = i_{CM1} + i_{CM2} = i_m + i_n, \tag{1}$$

$$i_{CM} = C_m \cdot \frac{\mathrm{d}v_m}{\mathrm{d}t} + C_n \cdot \frac{\mathrm{d}v_n}{\mathrm{d}t}, \tag{2}$$

where C_m and C_n, the parasitic capacitive coupling between the converter and the ground are excited, respectively by potential variations v_m and v_n. To cancel the CM current i_{CM}, the currents i_m and i_n should cancel each other. This leads to

$$C_m \cdot \frac{\mathrm{d}v_m}{\mathrm{d}t} = -C_n \cdot \frac{\mathrm{d}v_n}{\mathrm{d}t}. \tag{3}$$

From the previous equation one can deduce that if C_m is equal to C_n, v_m and v_n should be out of phase and equal in magnitude, to cancel i_{CM}. The areas that see voltage transition (called hot spots) and their coupling paths to ground will be studied in the next sub-section.

B. Topology of the multicell converter

The topology of the considered multicell converter is recalled in the Fig. 2. The Input Parallel Output Serie (IPOS) configuration has been used. The multi-cell converter, also called a Power Converters Array (PCA) is composed of n stacked cells. Each cell is identical to the others and their topology is described in the Fig. 3. The cell is actually a DC-AC converter composed of a Dual Active Bridge (DAB) for the isolated DC-DC part cascaded with a DC-AC full bridge voltage source inverter (VSI). The AC side filtering inductors L_{DM} are distributed on the output terminals along each cell. The identified hotspots are all the midpoints of

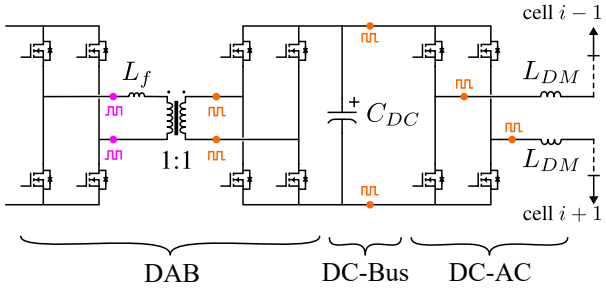

Figure 3. Circuit topology of a AC-DC conversion cell i with its hot spots in the primary (magenta) and secondary (orange) side of the transformer.

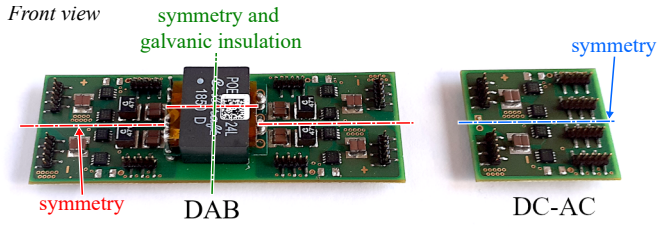

Figure 4. Circuit layout of a DC-AC cell split in two parts: the DAB on the left and the full bridge inverter on the right.

each leg (switching cell) in the conversion cell. The DC-Bus terminals are also considered as hotspots. Its potential is dependent upon the upstream and downstream cells states because of the series combination of the conversion cells on the AC side. The parasitic couplings of these hotspots with the ground on the secondary side and with the reference plane on the primary side will be identified in the next subsection.

C. Parasitic capacitance modelling at conversion cell scale

All conversion cells are the same. For practical reasons all conversion cells are split in two parts as illustrated in the Fig. 4. The first part includes the DAB converter which provides galvanic insulation thanks to its High Frequency (HF) transformer, and the second part is the full-bridge VSI which converts DC to AC. The layout has been designed with physical and impedance symmetry in mind to ensure that the parasitic capacitive couplings to the ground and reference planes are of similar value for each leg. Each cell is then assembled on the motherboard depicted in the Fig. 5. This motherboard connects the inputs of all conversion cells in parallel to the DC + and DC – terminals (battery side). The motherboard also provides series interconnections for all AC-side output terminals of the converter cell. At last, the motherboard also includes connection to ground and various configuration for control signals interconnections between the control board (in red on the Fig. 5) and the various conversion cells on the motherboard. The symmetry is kept at the motherboard level. In this example, a PCA of 6 conversion cells is shown in Fig. 5. On the primary side of the DAB the reference potential is called Ref., on the secondary side it is called ground (Gnd).

The parasitic capacitive couplings from a DC-AC conversion cell to the ground and reference planes are listed and

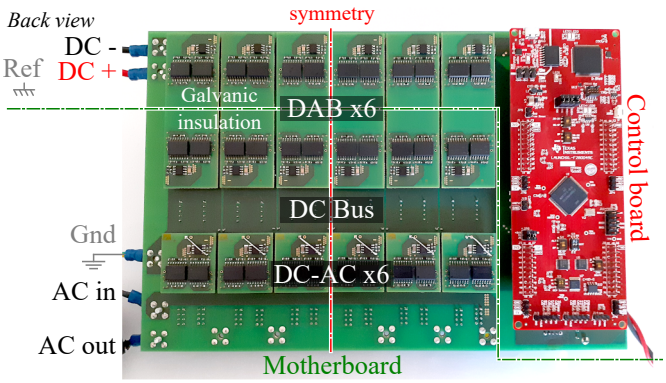

Figure 5. Motherboard of a PCA equipped with its 6 AC-DC cells and control board.

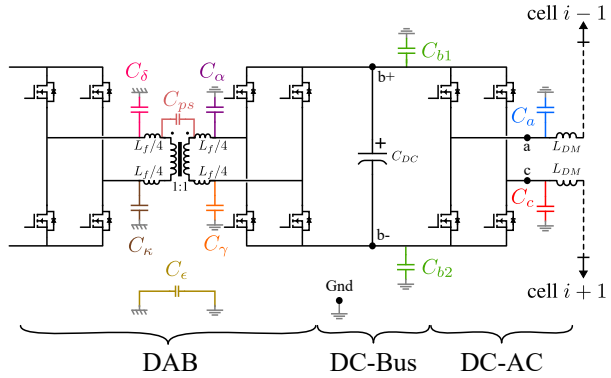

Figure 6. Parasitic capacitances to the Gnd and to Ref. of a DC-AC cell.

depicted in the Fig. 6. The capacitance from the primary side of the DAB to the Ref. are C_δ and C_κ. The capacitive couplings across the galvanic insulation are C_{ps} the inter-winding capacitance of the transformer and C_ϵ the overall capacitance between Ref. and Gnd. The two latter are low in comparison to the other parasitic capacitances on the secondary side (2 times smaller than $C_\alpha, C_\gamma, C_{b1}, C_{b2}$). So, the primary side of the DAB is neglected in the following.

The capacitances C_α, C_γ between the midpoint of the legs of the secondary side of the DAB and Gnd are considered part of the total DC bus parasitic capacitance to Gnd $C_b = C_\alpha + C_{b1} + C_\gamma + C_{b2}$, because their potential depends mainly upon the state of the upstream and downstream cells that are in series combination at the AC part and because C_{DC} (1000 µF) is much bigger than C_b (157 pF). This leads to the secondary side switching events of the DAB being also neglected in the following. As a consequence, the circuit of the Fig. 6 is simplified to the left-hand side circuit of the Fig. 7 with the parasitic capacitance C_b (evenly distributed on the DC bus for the sake of simplicity) and the parasitic capacitance C_a and C_c of each leg. In the HF equivalent circuit, the two $C_b/2$ are actually in parallel and form C_b as depicted in the right-hand side of the Fig. 7. This simplification is realistic for the frequency range of a few MHz and necessary to keep the model at PCA level reasonable. The parasitic capacitances C_a and C_c are taken into account in the equivalent circuit of a cell whereas prior work from the literature [16] omits them.

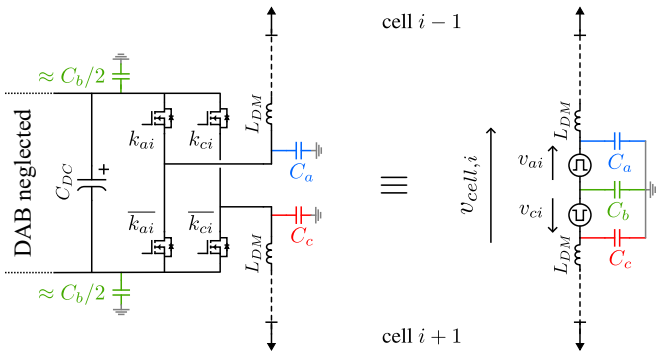

Figure 7. Circuit of the DC-AC part of the cell i with its parasitic capacitances and its equivalent circuit.

Table I
VALUE OF PARASITIC CAPACITANCES OF INTEREST.

Parasitic Capacitances	Values (pF)
C_{ps}	19.5
C_{b1}	33.1
C_{b2}	38.9
C_α	44.1
C_γ	40.9
$\mathbf{C_a}$	**17.9**
$\mathbf{C_b}$	**157.0**
$\mathbf{C_c}$	**17.9**

These parasitic capacitors are usually the main propagation paths for CM current in VSI and it is important to consider them as well in multicell converters.

Knowing the time domain hash functions k_{ai} and k_{ci} ($0 \equiv$ transistor k_{ai} open and $1 \equiv$ closed) it is possible to derive the equivalent circuit of the conversion cell. In this equivalent circuit the bridge legs have been replaced by equivalent voltage sources

$$v_{ai} = k_{ai} \cdot V_{DC}, \tag{4}$$

and

$$v_{ci} = k_{ci} \cdot V_{DC}. \tag{5}$$

The difference between these voltages gives the cell output voltage

$$v_{cell,i} = v_{ai} - v_{ci}. \tag{6}$$

Thanks to the symmetrical layout, C_a and C_c are of similar values as shown in the Table I. The values of the parasitic couplings have been measured thanks to an impedance analyser (*E4990* equipped with the *16047E* adapter).

Now that the parasitic capacitances have been identified and characterized, the impacts of the control strategies and switching event location are derived in the next section.

III. Control Strategy for CM Cancellation and Low Amplitude DM Current Ripple

The goal of this section is to analyse qualitatively conditions for the cancellation of CM currents in the VSI stage of the IPOS PCA as a function of the control strategy. Then, it will be possible to choose the best one from a point of view of CM

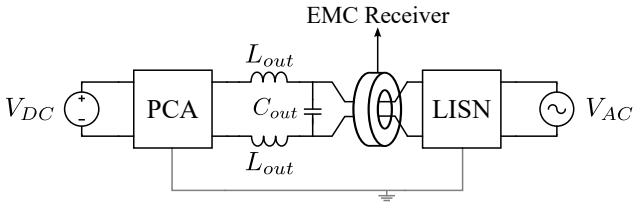

Figure 8. Circuit topology of a IPOS PCA with n cells.

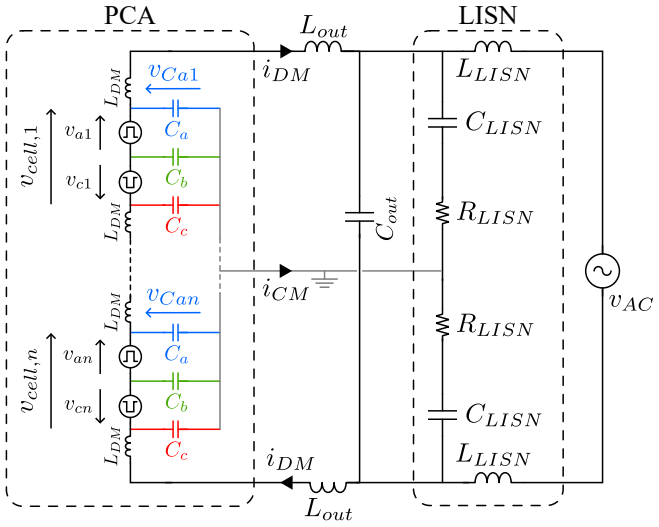

Figure 9. Equivalent circuit of the PCA for the conducted EMC study.

noise mitigation and low amplitude DM current ripple. As a consequence, the previously presented PCA setup is completed with a ground plane and a Line Impedance Stabilization Network (LISN), as described in the Fig. 8. The multicell converter CM current is directly measured thanks to a current probe plugged into the EMC receiver.

The study will focus on the cancellation of the common-mode current through careful symmetrical operation of the multicell converter. Then the current ripple of an interleaved converter with paired or not paired cells will be detailed. Finally, three different control strategies will be compared.

A. Modelling of the CM current in the PCA

The equivalent circuit of the cell from Fig. 8 is used in the Fig. 9 to detail the PCA HF equivalent circuit within the EMC setup. The LISN has been replaced by its equivalent model as well with L_{LISN}, C_{LISN} and R_{LISN}. According to Kirchhoff's current law, the total common mode current i_{CM} is the sum of the currents that go through the parasitic capacitances C_a, C_b, C_c of each conversion cell. It can be expressed as

$$i_{CM} = \sum_{i=1}^{n} \left(C_a \cdot \frac{\mathrm{d}}{\mathrm{d}t} v_{Cai} + C_b \cdot \frac{\mathrm{d}}{\mathrm{d}t} v_{Cbi} + C_c \cdot \frac{\mathrm{d}}{\mathrm{d}t} v_{Cci} \right), \tag{7}$$

with v_{Cai}, v_{Cbi} and v_{Cci} the voltages across the parasitic capacitances C_a, C_b and C_c of the i^{th} cell. The main difficulty is to express each parasitic capacitance voltage in a simple manner to assess quickly the potential of a control strategy. To that end, the following assumptions are considered: the C_{out} is big enough to absorb the main part of the HF transitions of i_{DM}. This leads to DM and CM decoupling and

$$\frac{\mathrm{d}i_{DM}}{\mathrm{d}t} = \frac{\sum_{m=1}^{n} v_{cell,m}}{2 \cdot (L_{out} + n \cdot L_{DM})}. \tag{8}$$

Assuming that the impedances of the a, b and c parasitic capacitances are greater than the LISN impedance, with ω the pulsation,

$$\forall \lambda \in \{a, b, c\}, \left| \frac{1}{\mathrm{j}\omega C_{LISN}} + R_{LISN} \right| \ll \left| \frac{1}{\mathrm{j}\omega C_{\lambda}} \right| \tag{9}$$

leads to v_{Cai}, v_{Cbi}, v_{Cci} being only dependent upon voltage drops produced by i_{DM} in such a way that

$$v_{Cai} = (2 \cdot (i-1) \cdot L_{DM} + (L_{out} + L_{DM})) \cdot \frac{\mathrm{d}i_{DM}}{\mathrm{d}t} - \sum_{k=1}^{i-1} V_{cell,k}. \tag{10}$$

By injecting (8) in the previous equation, the voltage across C_{ai} is expressed as

$$v_{Cai} = \frac{2i + \alpha - 1}{2(\alpha + n)} \cdot \sum_{m=1}^{n} v_{cell,m} - \sum_{k=1}^{i-1} v_{cell,k}, \tag{11}$$

where $\alpha = L_{out}/L_{DM}$. It is interesting to note that v_{Cai} does not depend upon the inductance values but on their ratio $\alpha = L_{out}/L_{DM}$. Then the remaining voltages are deduced from the previous equation

$$v_{Cbi} = v_{Cai} - v_{ai}, \tag{12}$$

and

$$v_{Cci} = v_{Cai} - v_{cell,i}. \tag{13}$$

Then it follows that

$$s_a = \sum_{i=1}^{n} v_{Cai} = \frac{n}{2} \sum_{m=1}^{n} v_{cell,m} - \sum_{i=1}^{n-1} (n-i) v_{cell,i}, \tag{14}$$

which is further simplified to obtain:

$$s_a = \sum_{i=1}^{n} \left(i - \frac{n}{2} \right) v_{cell,i}. \tag{15}$$

It is interesting to note that this equation does not depend upon the value or the ratio of the inductances but solely on the voltage transition of each leg and its position i in the series string. The same is performed for b and c capacitances,

$$s_b = \sum_{i=1}^{n} v_{Cbi} = \sum_{i=1}^{n} \left(\frac{n}{2} - i \right) \cdot \left(v_{a(n-i+1)} + v_{ci} \right), \tag{16}$$

$$s_c = \sum_{i=1}^{n} v_{Cci} = \sum_{i=1}^{n} \left(i - 1 - \frac{n}{2} \right) \cdot v_{cell,i}. \tag{17}$$

By substitution it comes that

$$i_{CM} = \frac{\mathrm{d}}{\mathrm{d}t} \left(C_a \cdot s_a + C_b \cdot s_b + C_c \cdot s_c \right). \tag{18}$$

Table II
HASH FUNCTIONS AND VOLTAGES OF CELL 1 AND n WHEN CONDITION 1 IS MET.

Hash function of cells 1 and n when condition 1 met.				Voltage of cell		Condition 2, K		Control scheme	
k_{a1}	k_{c1}	k_{an}	k_{cn}	$v_{cell,1}$	$v_{cell,n}$	$v_{a1}+v_{cn}$	$v_{an}+v_{c1}$	Bipolar	Unipolar
0	1	0	1	$-V_{DC}$	$-V_{DC}$	V_{DC}	V_{DC}	x	x
1	0	1	0	V_{DC}	V_{DC}	V_{DC}	V_{DC}	x	x
0	0	1	1	0	0	V_{DC}	V_{DC}		x
1	1	0	0	0	0	V_{DC}	V_{DC}		x
0	0	0	0	0	0	0	0		
1	1	1	1	0	0	$2\cdot V_{DC}$	$2\cdot V_{DC}$		

According to Table I, $C_a = C_c$ (because of the structural symmetry of the cells), which leads to

$$i_{CM} = \frac{\mathrm{d}}{\mathrm{d}t}\left(C_a\cdot(s_a+s_c)+C_b\cdot s_b\right). \tag{19}$$

Then to cancel i_{CM} the term $C_a\cdot(s_a+s_c)+C_b\cdot s_b$ should be equal to a constant in relation to the time t. There are a lot of ways to reach this result because of the 2^n degrees of freedom of the PCA control scheme, but in this article only some conditions will be deduced for the sake of simplicity and universality.

First, it is interesting to rewrite s_c as

$$s_c = -\sum_{i=1}^{n}\left(i-\frac{n}{2}\right)\cdot v_{cell,n-i+1}, \tag{20}$$

which, by injecting (15) and (20) in (19) leads to

$$i_{CM} = C_a\cdot\frac{\mathrm{d}}{\mathrm{d}t}\left(\sum_{i=1}^{n}\left(i-\frac{n}{2}\right)\cdot\left(v_{cell,i}-v_{cell,n-i+1}\right)\right) + C_b\cdot\frac{\mathrm{d}s_b}{\mathrm{d}t}. \tag{21}$$

If $v_{cell,i} = v_{cell,n-i+1}$ (condition number 1) it comes that $s_a + s_c = 0$ which results in

$$i_{CM} = \frac{\mathrm{d}}{\mathrm{d}t}\left(C_b\cdot s_b\right). \tag{22}$$

In other word, the symmetry of each cell output voltage in reference to the mid-point of the series string ensure the cancellation of the CM noise that flows through parasitic capacitances C_a and C_c.

Second, to cancel i_{CM}, s_b should be equal to a constant. According to (16) the easiest way to achieve this result for whatever number of cells n is to impose the condition number 2 such as

$$\forall i\in[\![1,n]\!],\ v_{a(n-i+1)}+v_{ci}=K, \tag{23}$$

with $K\in\{0,\ V_{DC},\ 2\cdot V_{DC}\}$. That way (16) becomes

$$s_b = K\cdot\sum_{i=1}^{n}\left(\frac{n}{2}-i\right) = -\frac{n}{2}\cdot K, \tag{24}$$

which is a constant. As a consequence, $i_{CM} = 0$ if both condition 1 and 2 are met. In order to better understand the meaning of this last sentence, the Table II provides an example. In this table, two cells are considered: the first and the last. Only the combinations of states of these two cells that respect condition 1 (here $v_{cell,1} = v_{cell,n}$) are listed in the table. The two first cases leads to: i) $K = V_{DC}$ for both of them, so they respect the condition 2, ii) they allow two states for the output voltage of the cells $-V_{DC}$ and V_{DC} (PWM bipolar control scheme of each VSI possible). It is also possible to use the set of the four first cases because: i) $K = V_{DC}$ for all of them, and ii) they allow 3 states for the output voltage of the cell $-V_{DC}, 0\ V$ and V_{DC} (PWM unipolar control scheme with both positive and negative parts). In other words, if the state of the a_i leg is opposed to the state of $c_{(n-i+1)}$ leg (antisymmetric with the mid-point of the series), then CM noise currents that flow through C_{bi} and $C_{b(n-i+1)}$ compensate each other's. This fact constrains the number of cells to be even otherwise the middle cell output voltage should always be 0 V.

The last two cases give $K = 0\ V$ and $K = 2\cdot V_{DC}$ respectively. Since there is only one case for each it means that all the cells have an output voltage of 0 V with both leg a and c at 0 V or at V_{DC}. These two cases are not compatible with a PWM control scheme, so here $K = V_{DC}$ is assumed for the condition 2 to be satisfied.

As a summary, the design guidelines for the control scheme of the DC-AC PCA that cancels CM current are:

- Symmetry of the output voltage of the cells with respect to the mid-point of the series string.
- Anti-symmetry of the leg states (a_i against c_{n-i+1}) with respect to the mid-point of the series string.

B. Modelling of the current ripple of an interleaved converter

According to the previous sub-section the paired operations of the cells is one way to respect the two conditions that lead to CM cancellation. This kind of operation has an impact on the current ripple seen by the inductance by doubling the voltage step and halving the apparent switching frequency. The goal is here to express in a general way the current ripple for an IPOS interleaved DC-AC multi-cell converter of n cells with or without paired operations of the cells.

The pattern of the current ripple in the inductance of an IPOS interleaved DC-AC multi-cell converter is the same of the one of a buck converter. Its current ripple Δi is well-known and defined as

$$\Delta i = \frac{D\cdot(1-D)\cdot V_{in}}{f\cdot L}, \tag{25}$$

with V_{in} the input voltage, D the duty cycle, L the inductor value and f the switching frequency. This equation is then

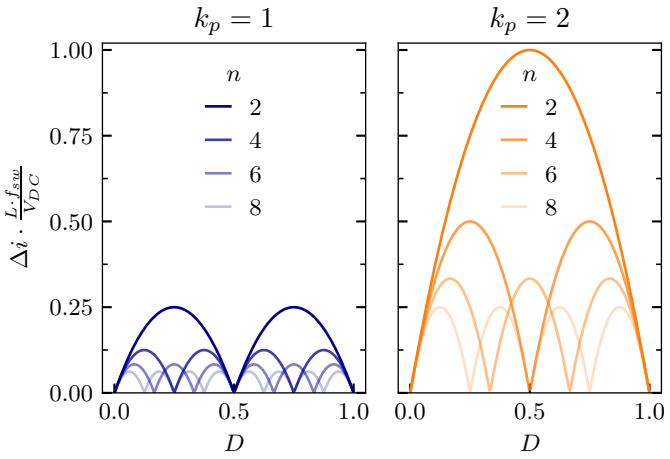

Figure 10. Normalized amplitude of the AC side output current ripple as a function of the duty cycle D when the cells are not paired (left plot $k_p = 1$) or paired (right plot $k_p = 2$).

modified to describe the current ripple of the multi-cell converter. First an effective duty cycle is defined as

$$D_{eff} = \left(D \bmod \frac{k_p}{n}\right) \cdot \frac{n}{k_p}, \tag{26}$$

with $\bmod$ the modulo operator and k_p the pairing coefficient (equal to 2 if the cells are paired and to 1 if not). Second, an effective voltage step which is the full voltage span on the AC side divided by the number of the cells over the pairing coefficient :

$$V_{eff} = 2 \cdot k_p \cdot V_{DC}. \tag{27}$$

Third, an effective frequency is defined as

$$f_{eff} = \frac{n}{k_p} \cdot \ f. \tag{28}$$

Finally, the substitution of D, V_{in}, f by D_{eff}, V_{eff}, f_{eff} in (25) leads to

$$\Delta i = \frac{2 \cdot \left(D \bmod \frac{k_p}{n}\right) \cdot \left(\frac{k_p}{n} - D \bmod \frac{k_p}{n}\right) \cdot n \cdot V_{DC}}{f \cdot L}. \tag{29}$$

The maximum of Δi happens for $(D \bmod k_p/2) = k_p/2n$, hence

$$\Delta i_{\max} = k_p^2 \cdot \frac{V_{DC}}{2 \cdot f \cdot L \cdot n}. \tag{30}$$

According to the two previous equations, the current ripple amplitude is inversely proportional to the number of cells whatever the pairing coefficient. When the cells are paired ($k_p = 2$) the current ripple amplitude is 4 times higher and the pattern as a function of D is halved accordingly as shown in the Fig. 10.

C. Comparison of the control strategies

The first control strategy studied is the Interleaved Bipolar (IB). The leg voltages of a PCA of 4 cells in IPOS configuration are shown in Fig. 11. The interleaved operation minimizes the AC side output current ripple by keeping voltage transition low and by increasing the effective switching frequency. At

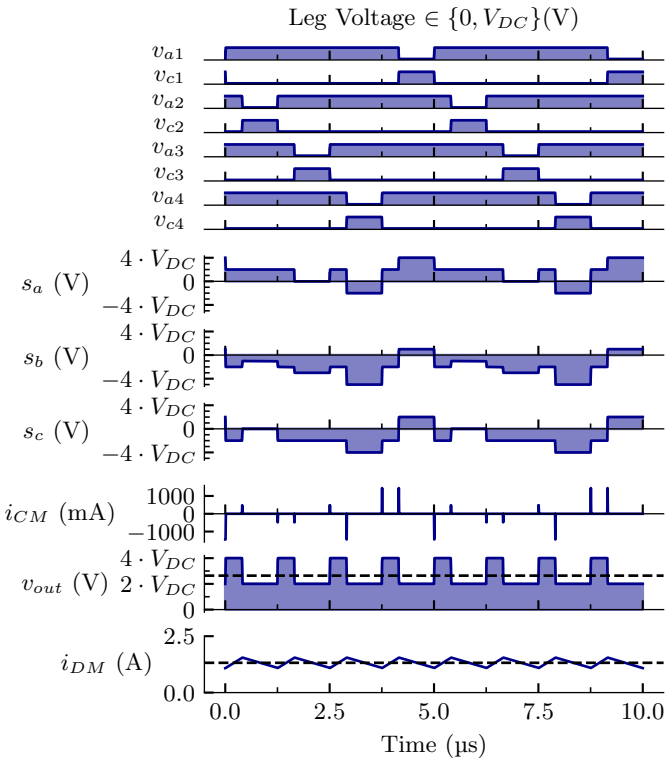

Figure 11. Results for a 4 cell PCA in IPOS configuration with IB control strategy (frequency of 200 kHz, duty cycle of 83%, no deadtimes and rise time and fall time equal both to 8 ns).

the same time S_a and S_c transitions are not opposed, and S_b shows voltage steps of $3 \cdot V_{DC}$. So, the resulting common mode current I_{CM} will be high. The voltage transition of v_{out} are equal to $2 \cdot V_{DC}$ and the current ripple Δi_{DM} for this point of load is around 400 mA as illustrated and depicted in Fig. 11

The second control strategy studied is called Interleaved Symmetrical Bipolar (ISB) and shown in the Fig. 12. That time, the lower half of the conversion cells are controlled symmetrically to the upper half as explained in [16]. As shown in Fig. 12 the s_a and s_c are now perfectly opposed and the common mode currents should cancel each other if C_{ai} and C_{ci} are similar. At the same time s_b sees no variations so the CM currents that flow through the C_{bi} are cancelling each other. These lead to a low CM current, almost 0 in theory (here a difference of 0.1 pF between C_a and C_c have been retained to show that because of some imperfection in the symmetry a small level of CM current remains, in that case 2000 smaller than previously). It has to be mentioned that the symmetry of the control signals among conversion cells has divided the interleaving degree of freedom by 2. Indeed, the voltage transitions are multiplied by two and the effective frequency is divided by 2 in comparison to the IB case, as seen on the subplot of v_{out}. This results in a higher ac side output current ripple of approximately 2 A as depicted in Fig. 12

The last control strategy is called the Interleaved Symmetrical Unipolar (ISU). It benefits from the cancellation of the CM currents between the Ca and C_c capacitances as shown in Fig. 13, thanks to anti-symmetric operation of the legs of each cell with respect to the midpoint of the string. And

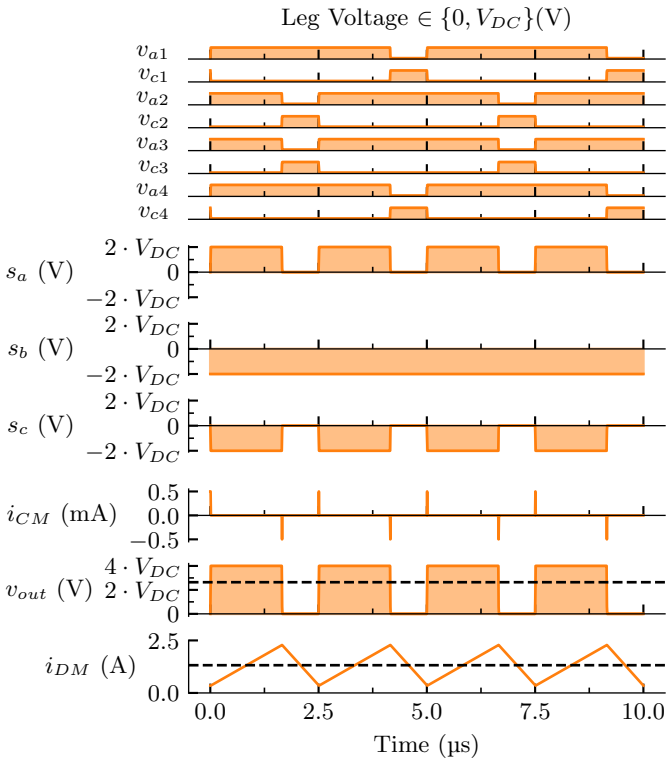

Figure 12. Results for a 4 cell PCA in IPOS configuration with ISB control strategy (same operating point as IB in Fig. 11).

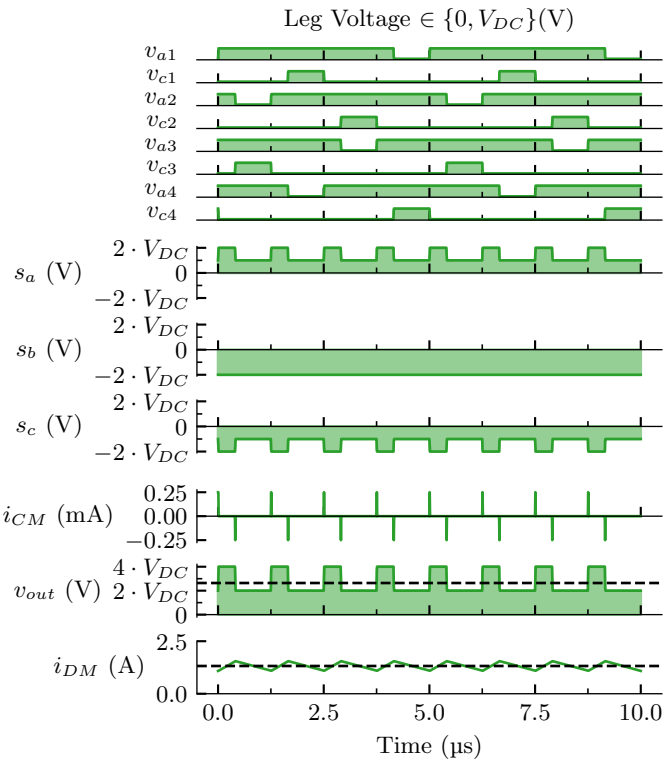

Figure 13. Results for a 4 cell PCA in IPOS configuration with ISU control strategy (same operating point as IB in Fig. 11).

at the same time the voltage transition v_{out} is kept low as the classical interleaved bipolar control strategy thanks to the unipolar approach which allows unpaired operation of the cells while keeping the output voltage of the cell symmetric with respect to the midpoint of the string. In this case, the current ripple is exactly the same with the one for the IB case. This result is expected because the sums of the voltages of the legs are exactly the same than for the IB case, only their order in the string of cells has been shuffled in comparison to the IB case.

The Fig. 14 compares the current ripple of each strategies as a function of the duty cycle D. As explained in the previous subsection the ISB strategy by pairing the operations of the cells increases the maximum current ripple by 4 times in comparison to the IB and ISU which do not pair the cells and have the same current ripple. This figure shows also that the maximum of current ripple is not located at the same duty cycle. This enables a fair comparison between the strategies and confirm that the ISB control strategy has always a higher current ripple than the IB and ISU control strategies.

Finally, the Table III provides a comprehensive comparison of the studied control strategies. With same number of converter levels, the proposed strategy ISU provides low current ripple like the classical IB strategy does thanks to unpaired operation ($k_p = 1$) while cancelling the CM like the ISB strategy [16] thanks to antisymmetric operation of the legs of the converter cells and symmetric output voltage of the converter cells.

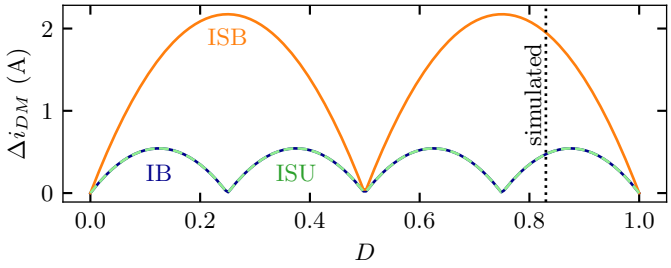

Figure 14. Current ripple of each control strategy as a function of the duty cycle D.

Table III
COMPREHENSIVE COMPARISON OF THE CONTROL STRATEGIES.

Control Strategy	Pairing coefficient k_p	Maximum current ripple $\Delta i_{\max}$	CM cancellation
IB	1	$\frac{V_{DC}}{2 \cdot f \cdot L \cdot n}$	No
ISB	2	$4 \cdot \frac{V_{DC}}{2 \cdot f \cdot L \cdot n}$	Yes
ISU	1	$\frac{V_{DC}}{2 \cdot f \cdot L \cdot n}$	Yes

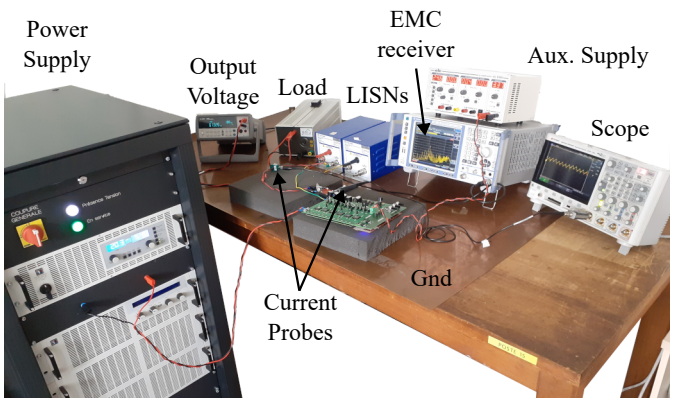

Figure 15. Photograph of the experimental setup.

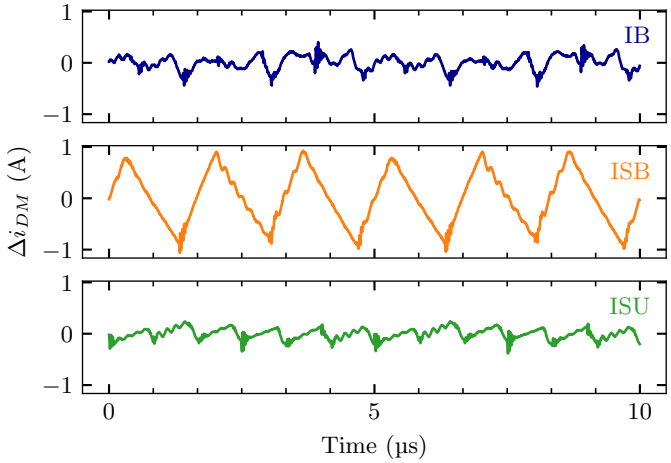

Figure 16. Current ripple at the AC side for the three control strategies.

IV. Experimental Validation and CM Filter

For the experimental validation of the control strategies, the setup described in the Fig. 8 is realized in the Fig. 15. with a *Person 2877* current probe plugged to a *R&S ESRP EMI Test Receiver 10Hz…3.6GHz* for the EMC measurements, a *Tektronix P6022* current probe plugged to a scope for the current ripple measurement and two *LI325-C* LISNs. The converter under test is a PCA of 6 cells with $V_{DC} = 20V$ operating at a fixed point of load at the AC side. Indeed, the duty cycle is fixed at 80%, and the grid is modelled by a resistive load of 40 Ω. An auxiliary supply of 3.3V is necessary to power up the control card of the PCA. This control card generates 6 phase-shifted PWM signals for the a legs. The signals for the b legs are generated from the a signals thanks to an inverse logic gate to ensure perfect synchronization. These signals are routed to the drivers through jumpers set according to the antisymmetric behaviour necessary for the CM cancellation.

A. Experimental comparison of the control strategies without filter

The measured current ripple at the AC side for the three control strategies is shown in the Fig. 16. As expected the greatest current ripple amplitude is for the ISB case and the apparent frequency has been halved. Concerning the CM current, the results without filter are shown in the 17 and compared to the DO160G category B standards level known for its stringent requirements. The ISB and the proposed ISU control strategies show a reduction of the measured CM current of roughly 40 dBµA from 100 kHz to 5 MHz in comparison to the classical IB strategy.

The hypothesis that the DAB part of the cells is not the biggest emitter on the AC side is confirmed as can been seen on the IB case where no harmonics of 98 kHz appears. These harmonics appear only when the noise produced by the full bridge inverter is low enough to unmask them as in the case of the ISU control strategy.

Even with the proposed control strategy a CM filter would be required in this particular case, but most of the effort has been made thanks to the control strategy and since the current ripple is the same as a classical IB strategy no increase of

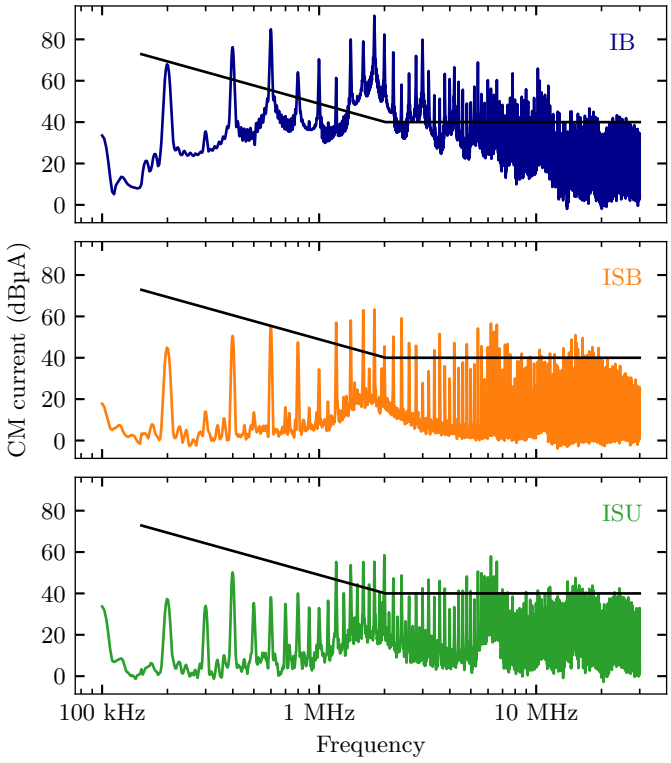

Figure 17. CM current measured at the probe with different control strategies and compared to the DO160G category B standard level (in solid black).

the output inductance is necessary as in [16]. In the next subsection, a common-mode filter will be designed for the two compared control strategies that are IB and ISU (ISB has a similar CM noise spectrum than ISU).

B. Sizing of the Common Mode Filter

The goals of this section are to provide a CM filter to the converter chain, and to show that even without CM filter optimization there is a substantial volume gain of the filter thanks to the proposed control strategy.

Table IV
COMPARISON OF THE COMMON-MODE CHOKES.

Control	f_{corner}	L_{CM}	Volume
IB	62,3 kHz	1.5 mH	2.0 cm^3
IUS	481,7 kHz	25 µH	0.5 cm^3

The corner frequency approach is used to size the CM filter. First the required attenuation Req_{dB} is computed thanks to

$$\forall f \in \mathcal{F}_{std},\ Req_{dB}(f) = I_{CM,dB}(f) - Std_{dB}(f), \quad (31)$$

with f the frequency, $Std_{dB}(f)$ the standard value in dBµA at f, $\mathcal{F}_{std} = [f_{bot}, f_{top}]$ the standard interval (here between $f_{bot} = 150\ kHz$ and $f_{top} = 30\ MHz$), $I_{CM,dB}(f)$ the measured noise in dBµA at f.

Then knowing that the filter is here a LC topology, the corner frequency of the filter f_{corner} is evaluated thanks to

$$f_{corner} = \arg \min_{f \in \mathcal{F}^+_{Req}} \left(f \cdot 10^{-\frac{Req_{dB}(f)}{\alpha_{LC}}} \right), \quad (32)$$

with $\mathcal{F}^+_{Req}$ the frequency interval where $Req_{dB}(f) > 0$ and the slope of the filter attenuation $\alpha_{LC} = 40\ dBA/decade$.The capacitance value C_Y is chosen by the designer, therefore the CM choke inductor value is

$$L_{CM} = \frac{1}{8\pi^2 {f_{corner}}^2 C_Y}. \quad (33)$$

This methodology is applied hereafter for the IB and ISU cases. The C_Y capacitances chosen for both cases are 2x2.2 nF X7R class X1/Y2 from Würth Elektronik, referenced *885352213015*.

For the IB case an inductor has been chosen in the design kit *Würth Elektronik 744 998*. For the ISU case a custom common mode choke has been designed with the cores available at the lab: a N49 ring core of dimension 10x6x4.5 mm^3 with 8 turns. The Table IV compares the corner frequency, the inductance value and the volume of the CM chokes (without plastic holder). The volume ratio of ISU in comparison to IB case is 4 times smaller. The considered chokes are characterized thanks to an impedance analyser to check that the required attenuation is obtained as it can be seen in the Fig. 18 for the IB case. Then the filter is built using a PCB from the kit 744 998 and set up inside the converter chain. The measured noise with the filter is compared against the standard and against the noise without the filter for the IB case and the proposed ISU case respectively in Fig. 19 and in Fig. 20. These two figures show that the filters designed are able to mitigate the noise produced by the PCA. The filters are shown in the Fig. 21. The left one is for the IB case and the right one for the ISU case. Even without proper optimization of the filter stage it is possible to see that the volume of the common mode choke is much smaller in the ISU case due to lower common-mode noise emissions.

V. CONCLUSION

In this paper, the inherent symmetrical layout of the multi-cell converter has been used to cancel common-mode noise

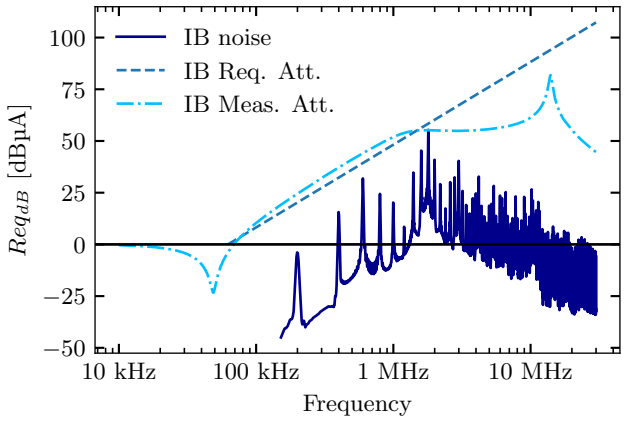

Figure 18. Required and measured attenuations of the filter for the IB control strategy.

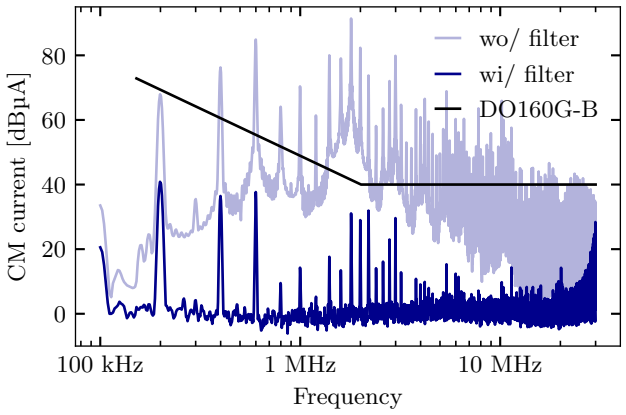

Figure 19. CM current measured with and without filter for the IB control strategy.

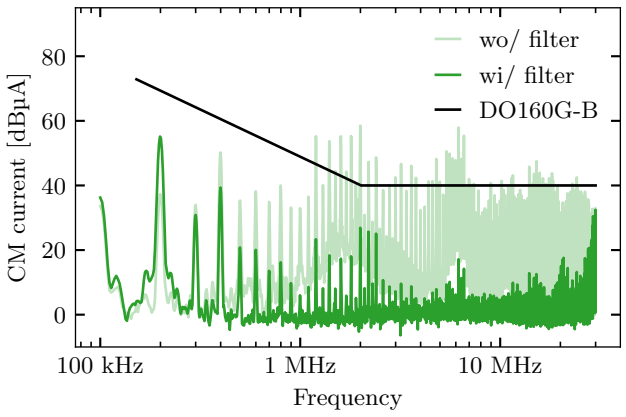

Figure 20. CM current measured with and without filter for the ISU control strategy.

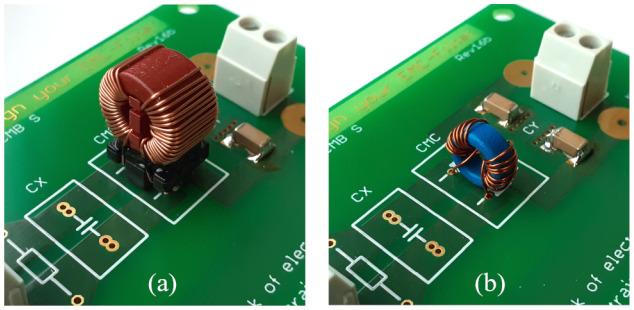

Figure 21. Comparison of filters and CM chokes size for (a) the IB control strategy and (b) for the proposed ISU.

by balancing switching events between the upper cells and the lower cells of the converter. Due to the series combination of the cells at the output terminals, the parasitic capacitance on the DC side of each conversion cell plays a great role in the common-mode generation as it was shown without symmetrical operation of the converter.

An interleaved symmetrical unipolar (ISU) control strategy has been proposed to cancel the CM noise while at the same time keeping the current ripple low thanks to unpaired operation of the cells.

The proposed ISU control strategy and the inherent symmetrical layout of the PCA show a lower noise level that is easier to filter than for a conventional IB control strategy. This demonstrates the advantages of a multi-cell approach, even from an EMC point of view.

A more accurate and quantitative model of common mode currents is needed to assess, at the design stage, more precise requirements of the filter. This work paves the way toward a filter-less PCA. The impact of the inductance value uncertainty, and of the sensing circuitry on the symmetry of the system and way to compensate it will be studied in future work.

REFERENCES

[1] V. Forti, C. P. Baldé, K. Ruediger, and G. Bel, *The Global E-waste Monitor 2020: Quantities, flows and the circular economy potential*, united nations university (unu)/united nations institute for training and research (unitar) – co-hosted scycle programme, international telecommunication union (itu) & international solid waste association (iswa) ed., 2020. [Online]. Available: https://ewastemonitor.info/gem-2020/

[2] M. Kasper, D. Bortis, G. Deboy, and J. W. Kolar, "Design of a highly efficient (97.7%) and very compact (2.2 kW/dm ^{3}) isolated ac–dc telecom power supply module based on the multicell isop converter approach," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7750–7769, 2017.

[3] J.-C. Crébier, T.-H. Phung, V.-S. Nguyen, T. Lamorelle, A. Andreta, L. Kèrachev, and Y. Lembeye, "Dc-ac isolated power converter array. focus on differential mode conducted emi," *Electronics*, vol. 8, no. 9, 2019. [Online]. Available: https://www.mdpi.com/2079-9292/8/9/999

[4] M. Kasper, D. Bortis, and J. W. Kolar, "Scaling and balancing of multi-cell converters," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, 2014, pp. 2079–2086.

[5] M. Rio, K. Khannoussi, J.-C. Crébier, and Y. Lembeye, "Addressing circularity to product designers: Application to a multi-cell power electronics converter," *Procedia CIRP*, vol. 91, pp. 134–139, 2020, enhancing design through the 4th Industrial Revolution Thinking. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S2212827120307964

[6] M. Shoyama, G. Li, and T. Ninomiya, "Balanced switching converter to reduce common-mode conducted noise," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 6, pp. 1095–1099, 2003.

[7] L. Xie, X. Ruan, H. Zhu, and Y.-K. Lo, "Common-mode voltage cancellation for reducing the common-mode noise in dc–dc converters," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 5, pp. 3887–3897, 2021.

[8] S. Wang, P. Kong, and F. C. Lee, "Common mode noise reduction for boost converters using general balance technique," *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1410–1416, 2007.

[9] L. Xing and J. Sun, "Conducted common-mode emi reduction by impedance balancing," *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1084–1089, 2012.

[10] J.-C. Crébier and J.-P. Ferrieux, "Pfc full bridge rectifiers emi modeling and analysis-common mode disturbance reduction," *IEEE Transactions on Power Electronics*, vol. 19, no. 2, pp. 378–387, 2004.

[11] A. Videt, M. Messaoudi, N. Idir, H. Boulharts, and H. Vang, "Pwm strategy for the cancellation of common-mode voltage generated by three-phase back-to-back inverters," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2675–2686, 2017.

[12] M. C. Cavalcanti, K. C. de Oliveira, A. M. de Farias, F. A. S. Neves, G. M. S. Azevedo, and F. C. Camboim, "Modulation techniques to eliminate leakage currents in transformerless three-phase photovoltaic systems," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 4, pp. 1360–1368, 2010.

[13] A. K. Gupta and A. M. Khambadkone, "A space vector modulation scheme to reduce common mode voltage for cascaded multilevel inverters," *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 1672–1681, 2007.

[14] W. Li, Y. Wang, J. Hu, H. Yang, C. Li, and X. He, "Common-mode current suppression of transformerless nested five-level converter with zero common-mode vectors," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4249–4258, 2019.

[15] Y. Qi and X. Wu, "Impedance-balancing-based modulation strategy for common-mode noise elimination of chb converter," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 374–378.

[16] Y. Qi, X. Wu, and F. Muhammad, "Mirror-bridge phase-shift modulation with low common-mode noise for single-phase chb pfc," *IEEE Transactions on Power Electronics*, vol. 36, no. 12, pp. 13 716–13 725, 2021.

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