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Reading reliability in 1S1R OTS+PCM devices based on Double-Patterned Self-Aligned structure

R. Antonelli^{a,b}, G. Bourgeois^a, V. Meli^a,
Z. Saghi^a, T. Monniez^a, S. Martin^a, N. Castellani^a, M. Bernard^a,
L. Fellouh^a, A. Salvi^a, S. Gout^a, F. Andrieu^a, A. Souifi^b, G. Navarro^{a,*}

^a CEA-Leti, Univ. Grenoble Alpes, 38000 Grenoble, France

^b Univ. Grenoble Alpes, CNRS, LTM, 38054 Grenoble, France

* Email: gabriele.navarro@cea.fr

Abstract

This study investigates the reliability of the reading operation in 1S1R devices based on Ovonic Threshold Switching (OTS) selector and Phase-Change Memory (PCM) co-integrated in a Double-Patterned Self-Aligned (DPSA) structure targeting Crossbar applications. Upon reading, the SET state can face a threshold voltage (V_{th}) increase of more than 20% dependently on the reading current and on the number of reading operations, which can lead to a soft failure. We separate the contributions to this increase coming respectively from OTS and PCM, finally providing an assessment protocol for the reading reliability. We show how the reading performances allow to determine the maximum Crossbar array size depending on the target voltage Read Window Margin and current Memory Window.

1. Introduction

The 1S1R cell (one selector, one resistor), co-integrating at the same time the memory and the selector device and used as main block of 3D Crossbar arrays, is considered an excellent solution for high-density Back-End-of-Line (BEOL) memories [1, 2]. The 1S1R implemented by combining Phase-Change Memory (PCM) and Ovonic Threshold Switching (OTS) selector, demonstrated its high potential in Storage Class Memory (SCM) and cache replacement [3]. PCM is the most mature among emerging memory technologies, offering a small footprint, and non-volatility [4] making it suitable for embedded applications [5]. The OTS selector provides low leakage current, fast switching speed, and stackability in the BEOL of the integration [6, 7]. The significant advantage of integrating OTS with PCM is the possibility to implement a self-aligned integration approach, reducing lithographic mask requirements and enhancing overall yield [8]. In this study, we based our analyses on a Double Patterned Self-Aligned (DPSA) OTS+PCM device [9]. We investigate the impact of the reading operation, critical for OTS+PCM devices reliability. We propose a protocol based on consecutive reading operations, at

different reading currents and durations, to assess the reduction of the effective voltage Read Window Margin (RWM) and current Memory Window (MW). When the PCM is programmed in the SET state (i.e. crystalline phase), a repeated reading is responsible for an increase of the threshold voltage (V_{th}) up to more than 20% with respect to the starting SET threshold voltage ($V_{th,SET}$), leading to possible soft failures.

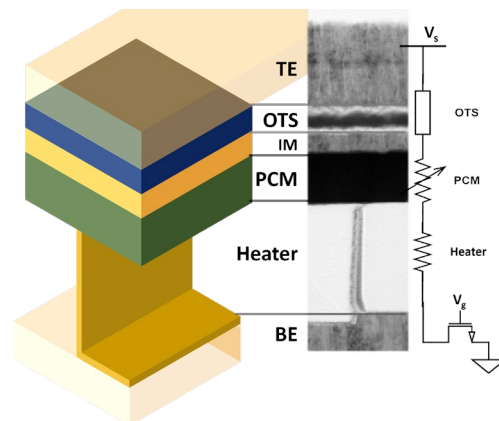


Fig. 1. 3D scheme and Transmission Electron Microscopy (TEM) image of a DPSA 1S1R OTS+PCM device, with a simplified circuit scheme of the device on the right.

By comparing the results obtained from 1S1R, 1S OTS and 1R PCM devices, we are able to study the different contributions to the V_{th} increase. We find a correlation between the V_{th} shift, the SET read current ($I_{read,SET}$) and the number of reading cycles, showing that the RWM reduction (soft bit fail) is caused by repeated reading of the cell, independently from the value of the read current. Finally, we show how the reading reliability in 1S1R cells, without considering smart reprogramming strategies, can affect the choice of the maximum Crossbar array size based on the target MW and RWM.

2. OTS+PCM device reading reliability protocol

2.1. 1S1R DPSA device

The DPSA device structure is depicted in **Fig. 1** and previously described in detail in [9]. The cell is fabricated through two patterning steps (“Double-Patterned”), allowing at the same time the PCM alignment with the heater element and the definition of the OTS dimensions (“Self-Aligned”). The phase-change material considered in our study is $Ge_2Sb_2Te_5$, and the OTS selector is based on a $GeSbSeN$ alloy [7]. The OTS layer was integrated between two thin carbon layers to hinder intermixing with electrodes. The Top Electrode (TE), Bottom Electrode (BE), Intermediate Metal (IM), and heater are made of titanium nitride (TiN). We tested devices integrated in kb arrays, with critical dimensions ranging from 80 nm up to 300 nm.

2.2. Reading reliability test protocol

When PCM is co-integrated with a two-terminal nonlinear selector as the OTS, the read current (I_{read}) depends on the state of the memory and the voltage partition between the two [10]. The common 1S1R reading principle involves the switching of the device to exploit its high I_{ON}/I_{OFF} current ratio (**Fig. 2**). If the PCM device is in the low resistance state (SET), the reading voltage (V_{read}) chosen inside the RWM allows the switching of the OTS and a significant current flow in the device ($I_{read,SET}$). If the PCM device is in the high resistance state (RESET) both the OTS and the PCM do not reach the threshold condition and the device does not switch providing a low current flow ($I_{read,RESET}$) that depends on both PCM and OTS resistances. Therefore, the reading relies on the current MW that is defined as the ratio between $I_{read,SET}$ and $I_{read,RESET}$. A reading fail can be generated if the cell does not switch at V_{read} due to an unwanted increase of the $V_{th,SET}$ (SET failure), or if the cell switches at V_{read} when programmed in the RESET state (RESET failure).

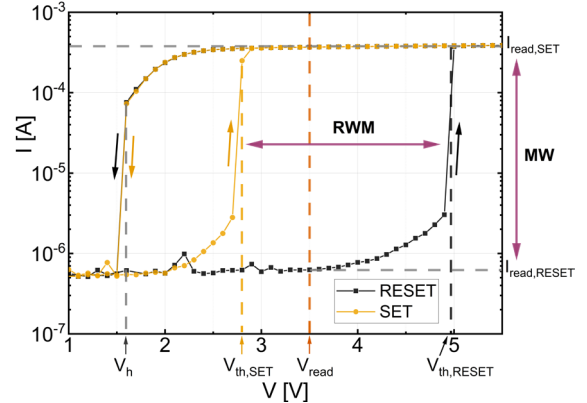


Fig. 2. Typical IV curves of a DPSA 1S1R OTS+PCM in SET and RESET states. The main electrical parameters are highlighted. The MW is calculated as the ratio $I_{read,SET}/I_{read,RESET}$ and the RWM as the difference between the V_{th} when the device is programmed in the RESET state ($V_{th,RESET}$) and the SET state ($V_{th,SET}$). The curve is obtained as the median of about 300 devices.

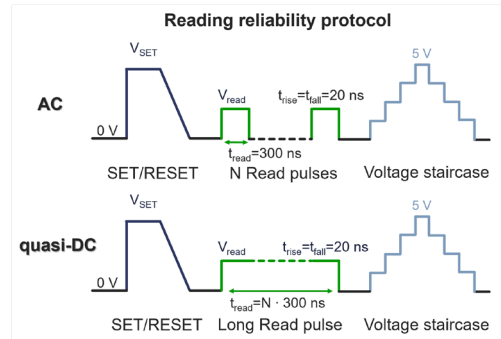


Fig. 3. AC and quasi-DC protocols description.

We devised two test protocols to investigate the impact and reliability of the reading (**Fig. 3**). The AC protocol consists of a programming pulse (SET or RESET), followed by a fast sequence of multiple reading pulses of duration $t_{read} = 300$ ns each. The quasi-DC protocol involves the same programming pulse, with a subsequent long read pulse of duration equivalent to $N \cdot t_{read}$, where N corresponds to the number of read cycles performed in the AC protocol. In both cases, a staircase-up sequence records the IV curve of the device and detects its V_{th} . We selected a V_{read} of 3.5 V and a $I_{read,SET}$ ranging from 60 μA up to 400 μA . The $I_{read,SET}$ is limited by a series NMOS transistor.

3. 1S1R reading reliability

3.1. RESET state reading

The PCM in RESET state is highly resistive with a V_{th} close to 2 V, in series with the OTS V_{th} of 3 V, resulting in an overall $V_{th,RESET}$ of approximately 5 V. When employing the quasi-DC protocol, the I_{read} is

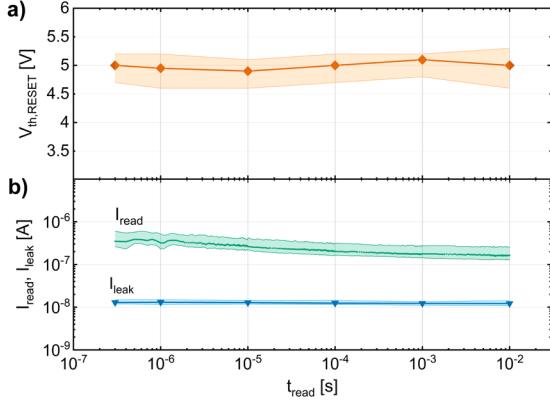


Fig. 4. $V_{th,RESET}$ (a); I_{read} measured at $V_{read} = 3.5$ V and I_{leak} at 1.75 V (b) for different read pulse duration t_{read} during *quasi-DC* protocol (*AC* showed equivalent results). The graphs report the median values and the Interquartile Ranges (IQR) of about 150 1S1R devices.

sampled during the read pulse, followed by the measurement of the leakage current (I_{leak}) at $V_{read}/2$ and of the V_{th} . **Fig. 4a** presents the median V_{th} over multiple t_{read} intervals. $V_{th,RESET}$ remains constant independently from the reading pulse duration and no switching occurs. Indeed, I_{read} remains below 1 μA (**Fig. 4b**). I_{leak} is more than one order of magnitude lower than I_{read} confirming the good preservation of the OTS selecting performances. The RESET state confirms to be stable under the reading protocols used, with no failures detected during our tests.

3.2. SET state reading

By applying the *AC* protocol to the device in the SET state, the threshold voltage increases (**Fig. 5**) shifting from the as-programmed $V_{th,SET}$. There is both a marked dependency on the number of reading cycles as well as on $I_{read,SET}$. Performing the test on a 1R PCM cell (**Fig. 6a**) highlights a direct link between the resistance of the PCM cell and the SET read current. On the other hand, in the OTS alone there is no apparent trend linked to the read current amplitude while the number of cycles produce a threshold increase of more than 200 mV (**Fig. 6b**). Comparing the results of the *AC* and *quasi-DC* protocols on 1S1R cell (**Fig. 5**), V_{th} significantly increases in *AC* reading protocol, up to more than 20% (i.e. ~ 0.4 V), while with the *quasi-DC* protocol, as the width of the pulse increases, we observe a first increase of V_{th} followed by a decrease down to the initial $V_{th,SET}$. We correlate such difference to the number of the switching events, which occur at each reading pulse in the *AC*, and once in the *quasi-DC*. In both protocols, the shift increases with $I_{read,SET}$.

We approximate the V_{th} evolution along the *AC* reading cycles number with the following empirical relation:

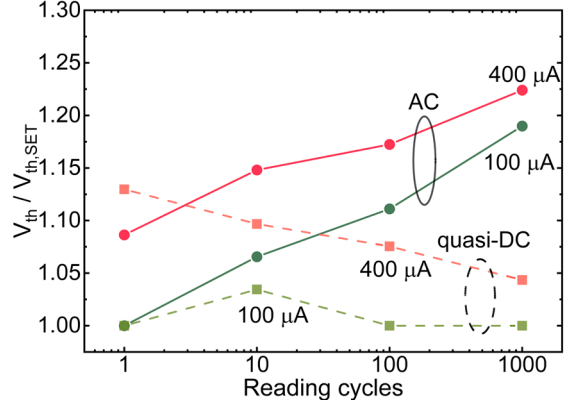


Fig. 5. V_{th} over $V_{th,SET}$ as a function of the applied reading pulses in 1S1R devices for *AC* (solid lines) and *quasi-DC* (dashed lines) protocols at different $I_{read,SET}$. The median values are obtained from about 200 1S1R devices.

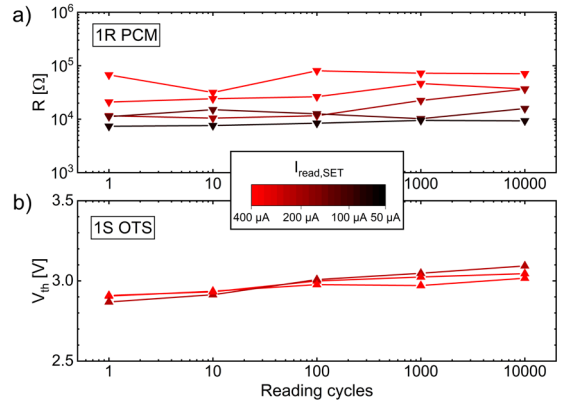


Fig. 6. a) Resistance of PCM. b) OTS V_{th} for increasing number of reading cycles at multiple $I_{read,SET}$. Median from 30 devices each.

$$V_{th}(N) \approx V_{th0} + \log_{10}(N) \cdot \Delta V_{th-N} \quad (1)$$

Here the slope ΔV_{th-N} represents the increase in threshold voltage due to the total number of cycles (i.e. number of switches), while the intercept V_{th0} corresponds to the starting V_{th} (i.e. after the first reading). **Fig. 7a** reports ΔV_{th-N} as a function of the reading current. The V_{th} shift wrt $V_{th,SET}$ is almost independent from $I_{read,SET}$ and it is constant at about 150 mV for the *AC* protocol and about zero in *quasi-DC* case. The intercept V_{th0} appears linearly correlated to $I_{read,SET}$, describing $\Delta V_{th-Iread}$ as the increment over $V_{th,SET}$ due to reading (**Fig. 7b**):

$$\Delta V_{th-Iread} = V_{th0} - V_{th,SET} \propto I_{read,SET} \quad (2)$$

The obtained results show that ΔV_{th-N} depends only on the switching events of the selector (**Fig. 5, 6, 7a**). Such a shift is attributable to the evolution of the OTS material induced by the current density spike happening at the switching event. Indeed, it can lead

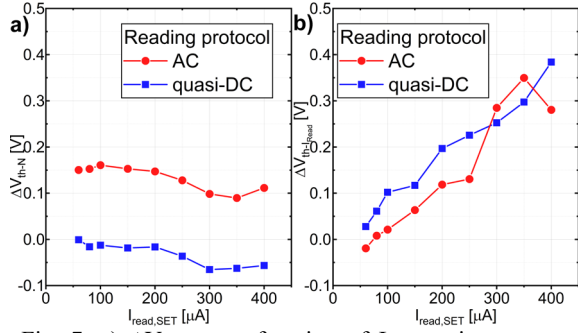


Fig. 7. a) ΔV_{th-N} as a function of $I_{read,SET}$ in agreement with (1). b) $\Delta V_{th-Iread}$ shift as a function of $I_{read,SET}$ in agreement with (2). The median values are obtained from about 200 1S1R devices.

to an increase in the localization of defects in the conductive path, thereby increasing the resulting V_{th} [11]. On the other hand, $\Delta V_{th-Iread}$ increase can be correlated to a partial PCM amorphization due to an increasing $I_{read,SET}$, approaching a programming condition, independently from the number of reading cycles N . Both $I_{read,SET}$ and N decrease the RWM (Fig. 8). Limiting $I_{read,SET}$ may not be sufficient to avoid SET soft failures when multiple readings are performed without reprogramming, due to the switching event effects on OTS. A possible strategy to mitigate $\Delta V_{th-Iread}$ could be to increase the read pulse fall time (i.e. re-programming).

In light of these findings, it is possible for Crossbar design to select the appropriate density of an $M \times M$ matrix which maximizes the RWM, MW, and N before refresh (inset of Fig. 8) considering the worst-case MW (I_{leak} when all unselected cells are in SET):

$$MW = \frac{I_{read,SET}}{2(M-1)I_{leak} + I_{read,RESET}} \quad (3)$$

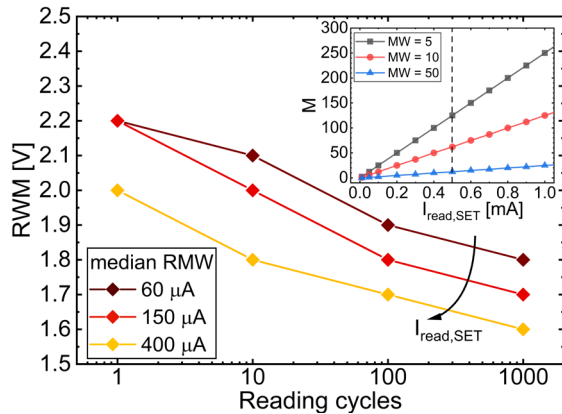


Fig. 8. Voltage RWM evolution over repeated reading cycles for different $I_{read,SET}$. The inset shows the maximum number of rows (cols) in a $M \times M$ matrix for different MWs calculated from (3). The dashed line in the inset separates the reading and the programming current regions.

4. Conclusions

In this article we assess the impact of reading operations on the reliability of the programmed states in DPSSA 1S1R OTS+PCM devices. RESET state showed high stability to reading, while SET state faces a V_{th} increase up to more than 20% of the starting $V_{th,SET}$. We evidence a double dependency of V_{th} shift: a gradual increase due to the switching event generated during the reading operations into the OTS device (ΔV_{th-N}); and a constant increase proportional to the reading current $I_{read,SET}$ ($\Delta V_{th-Iread}$) likely related to the PCM partial amorphization. By reducing $I_{read,SET}$ the number of allowed reading cycles increases (before triggering a first SET soft failure), and the SET V_{th} shift decreases, enabling a higher voltage RWM. However, a high $I_{read,SET}$ is important to preserve the reading current MW, therefore we justify how in Crossbar array design it should be carefully selected in order to maximize RWM, MW and the number of possible reading cycles.

Acknowledgments

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