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Preliminary SiC MOSFET Gate-Cracking Modeling under Short-Circuit Based on Rankine's Damage Energetic Approach Using a Wide Temperature-Range Elastoplastic 2D Simulation [Abstract]

M. Shqair, E. Sarraute, F. Richardeau

LAPLACE, University of Toulouse, CNRS, INPT, UPS, Toulouse, France

Abstract

For the first time, a structural physical modeling of the Intermediate-Layer-Dielectric (ILD) cracking in a planar-gate SiC MOSFET under short-pulse short-circuit is proposed. This new approach is based on Rankine's damage energetic description, relying on the SiO₂ mechanical properties. Using a complete 2D high-temperature range electrothermal-metallurgical and elastoplastic-mechanical SiC MOSFET model, Rankine's sub-model is successfully implemented. The first results allow the extraction of crack penetration depth in a single pulse, prefiguring the average critical cycles number estimation to a possible complete destructive ILD fracture.

1. Background, Methodology and Targets

SiC MOSFET technology is among the most interesting power devices in terms of application for combining high efficiency and high switching frequency in on-board power inverters. Short-circuit (SC) withstanding time (t_{scw}) and the maximal number of cycles (N_{cycles}) capabilities are essential features for obtaining operational certifications. Although much research has been conducted on the standard t_{scw} [1], N_{cycles} and SC life capabilities have received much less attention. Only classical, time-consuming and costly experimental approaches have been attempted [2]. Today, there is a lack of a full physical approach that modelizes the Intermediate Layer Dielectric cracking (ILD), which is clearly the weak gate region in short-pulse or medium-pulse periods in SiC MOSFETs [3]. To fill this gap, for the first time, this abstract investigates a new preliminary approach based on a complete 2D structural and physical modeling of the ILD gate-corner damage. Crack Modeling of SiO₂-type ILD is new and challenging due to its rigid and brittle nature. This material-type is clearly confirmed in SC experimentation by the occurrence of a very singular abrupt failure mode where cracks accumulate, leading to fracture damage and sharp-like gate-leakage that abruptly arises after a threshold number of cycles, as summarized in Fig.1. The crack modeling in SiO₂-type ILD also requires accurate and specific Finite Elements Modeling (FEM) of the local stress-strain distribution in all geometric singularities at the gate's areas. The Cohesive Zone Modeling (CZM) approach was previously introduced and used to analyze the crack formation

and evolution at the topside wire-metallization contact, depending on Al's grain boundary reconstructions, which cause the wire lifting-off [4, 5]. Although the CZM is suitable for modeling the damage at the interface between two boundaries, this method does not seem to be suitable for cracking problems within an isotropic and homogeneous solid material such as a SiO₂-type ILD domain. Therefore, a new approach is suggested in this paper based on Rankine's model. Such a model allows calculating the progressive partial damage quantity that reflects the effective local crack positions in the SiO₂ material, typically near the ILD's corner in SC operation, based on an energetic deformation model.

The abstract is organized as follows: Section 2 presents an update of our previous multiphysics modeling; Section 3 shows the implementation of the new Rankine's sub-model in Comsol™ FEM software and its verification; finally, Section 4 displays the first crack penetration results at the ILD-corner during a single and short-pulse SC.

2. The Complete Temperature Wide-Range Multiphysics Model of SiC MOSFET under SC Operation Condition

A static and transient electrothermal model including SiO₂-gate/SiC-channel fixed-charge and trapping-charge effect was previously developed by authors [6] and implemented in Comsol Multiphysics™. This model was extended, including the dynamic Al-source melting [7] and elastic-type thermo-mechanical simulation, considering deformations at wide-range temperature gaps at the ILD-Ti-Al region [8].

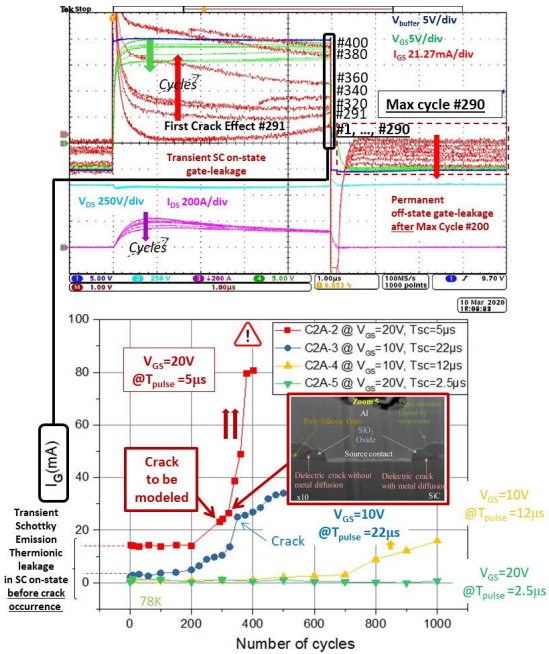


Fig.1. 3-Lead TO247 case-type planar-gate gen. II 80mΩ - 1.2kV device, $t_{scw} = 8\mu s_{600V-25^{\circ}C}$, type 1 SC cycling signature under: $V_{DS} = 600V$, $R_{Gate\ on/off} = 47\Omega$, $T_{Case} = T_{Room}$. Experimental results highlighting brittle-type first complete crack #291 and sharp-type gate-leakage through the ILD-corner as shown in the inserted SEM photo (Laplace Lab. database not published previously).

However, the latter did not take into account the elastoplastic behavior of the thick Al source layer and the Ti barrier around the ILD, especially as large thermal stress and strain are likely to occur under high amplitude SC. In order to obtain a more accurate model and precisely predict the crack-path progression, new Ti and Al deformation laws are proposed in this section. Fig.2 (a) shows the initial 2D symmetrical half-cell device's geometry and the doping applied to this model; Fig.2 (b) highlights the SC simulation after considering a channel-mobility fitting from an extension to Arora's model, including electrical and thermal temperature-dependent laws respecting the high temperatures in SCs, which appears physically consistent with experimental results from authors.

In-depth, bibliographical work enabled us to extend this previously published model, including now elastoplastic (Ti-Al) stress-strain laws as defined in Fig.3 [9]. A bilinear kinematic elastoplastic behavior is used as schematized in Fig.3 (a). Parameters are: Young modulus (E) representing the first linear elastic behavior, the isotropic plasticity tangent modulus (E_t) reflecting the second affine plastic behavior, and the yield stress (σ_{ys}) which is the stress-limit separator between both behaviors. As one can see in Fig.3 (b), it is critical to consider the wide temperature range dependency of these parameters, at least until the melting temperature of

Al is attained. The new plasticity laws assigned for both materials are highly temperature-dependent (except for E_t of Al). It should be noted that the relative sensitivity of Ti is much greater than that of Al, especially at temperatures below the Al melting [300K - 600K].

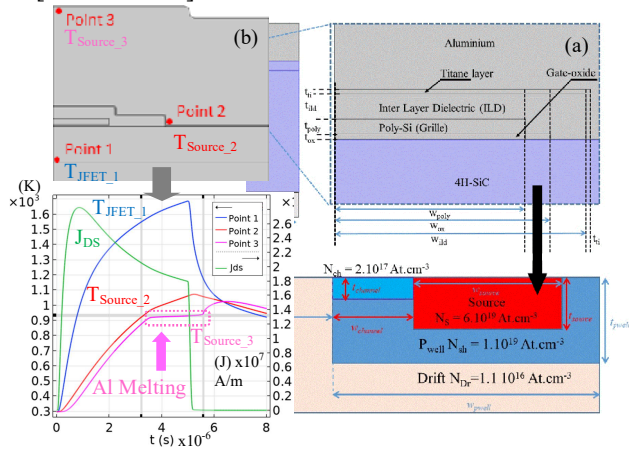


Fig.2. (a) Parametric 1.2kV-80mΩ, active area 6mm², half-cell gate-planar SiC MOSFET, (b) channel-mobility fitting completed by the Al phase-change modeling and temperature simulation for $V_{DS} = 600V$, $V_{GS} = 20V$, $T_{CASE} = T_{ROOM}$ [7] at points 1, 2 and 3.

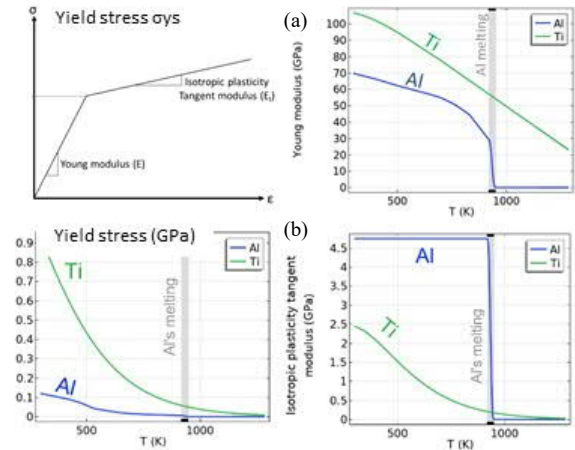


Fig.3. Temperature-dependent bilinear kinematic elastoplastic behavior of Ti barrier around the ILD-SiO₂ region and the thick Al source-layer [10-12].

3. Rankine's damage description and its implementation in Comsol™

The basis proposed in Rankine's theory is illustrated in Fig.4 at the gate-region ILD-SiO₂-Ti boundary [13]. The mechanical behavior is physically and locally modeled using a stress (σ) - displacement (δ) law. (σ) is the principal component representing the maximal sustainable stress by the material before its fracture [14]. State "1" in Fig.2 reflects the stiffness of the material, where the deformations are reversible. If stress reaches $\sigma_{fracture}$, state "2" arises, where the irreversible deformations of the material

begin. In state "2" ($\delta > \delta_s$), the stress decrease is sharp in the softening region for brittle materials such as SiO₂. Note that at this stage, due to the irreversible displacement nature, a proportional damage variable (D) is introduced: D = 0% for $\sigma \leq \sigma_f$ ($\delta \leq \delta_s$) and D = 100% for a stress-free state ($\delta = \delta_f$). State "3" appears when $\delta \geq \delta_f$, evidencing the formation of a crack. Rankine's theory suggests an energetic criterion: $G_f = \frac{1}{2} \cdot \sigma_f \cdot \delta_f$ where G_f is the energy density of the material up to fracture ($G_f = 4.5 \text{ J.m}^{-2}$ for SiO₂ [15]), σ_f is the fracture stress ($\sigma_f = 0.8 \text{ GPa}$ for SiO₂ [16, 17]), and δ_f is the elementary crack opening displacement of the material, derived from G_f and σ_f [13, 14]. If a linear-type softening is considered in the "2" interval, the SiO₂ crack opening is 11.25nm.

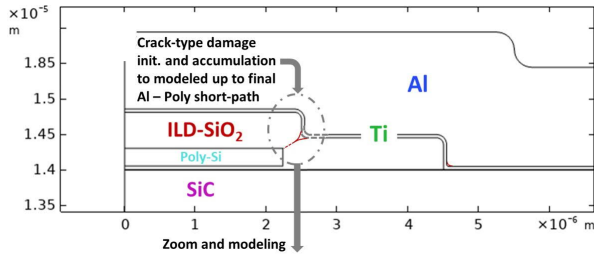


Fig.4 Rankine's theory applied to ILD-SiO₂ corner crack formation and effective crack. Introduction to local Damage formation (D < 100%) and effective Damage (D = 100%) defined by $D(\delta) = (\delta_f/\delta) \cdot (\delta - \delta_s) / (\delta_f - \delta_s)$ [14].

Fig.5 shows the validation in cycling mode of the proposed Rankine model in Fig. 4 applied on a simple case existing in Comsol Multiphysics library, which is a virtual brittle material [18] stressed by two cyclic loadings. It can be observed that the implemented model exhibits a more physical exponential stress-displacement behavior in the softening-unloading interval "2" as defined in Equation (1). Equation (2) gives the expression of the global energy G_f (covering intervals "1" and "2"). Equation (3) shows the formula of the analytical damage progression D_δ . These relations existing in Comsol Multiphysics™ [14] are to be considered to model the SiO₂ damage in the SiC MOSFET model.

$$\sigma = \sigma_s e^{-\frac{\delta - \delta_s}{\delta_f - \delta_s}} \quad (1) \quad G_f = \sigma_s \left(\delta_f - \frac{\delta_s}{2} \right) \quad (2)$$

$$D_\delta = 1 - \frac{\delta_s}{\delta} e^{-\frac{\delta - \delta_s}{\delta_f - \delta_s}} \quad (3)$$

This fine modeling finally allows calculating an effective crack opening from Equation (2): 5.6nm. This result is important for setting the mesh size at the ILD-SiO₂ region during the damage modeling.

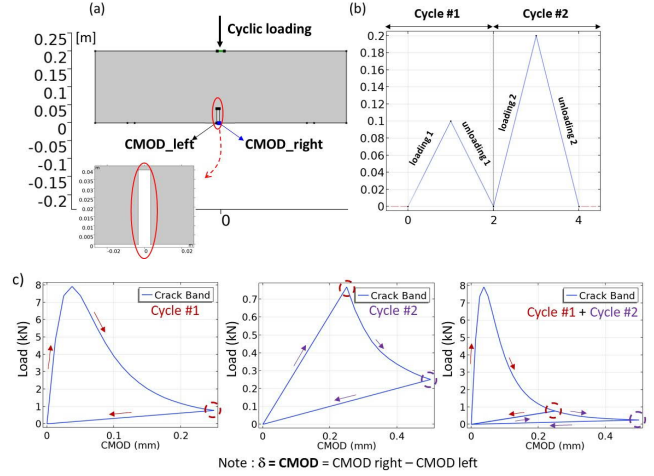


Fig.5 Rankine's model implementation validation in Comsol Multiphysics™ (a) notched beam model [18], (b) cyclic loading definition, (c) #1 and #2 cycle sequence. For: $G_f = 85 \text{ J.m}^{-2}$, $\sigma_f = 3.9 \text{ MPa}$, based on Young modulus $E = 37 \text{ GPa}$, Poisson's ratio $\nu = 0.21$ and density $\rho = 2400 \text{ kg.m}^{-3}$.

4. Analysis of the First Extracted Results (Critical Times and Energies, Crack Penetration Path, Cycles Number Withstanding Capability)

Rankine's model introduced in section 3, Fig.4, and validated under its physical form in Fig.5, is now implemented for the ILD-SiO₂ material in the complete 2D Multiphysics SiC MOSFET model depicted in section 2. An overview of results is presented in Fig.6 considering a top-side constrained surface above the metallization Al as a boundary condition to reflect the presence of a thermal-resistant epoxy resin (in full paper a boundary condition-type of free-displacement at the top-side of the metallization Al will be considered in another simulation as if a silicone gel a standard soft plastic coating exists). According to Equation (3), the simulations include deformations-adaptative meshing, depending on the progress of the displacement and damage at the ILD-SiO₂ corner. Results in Fig.6 show a damage concentration (D = 100%) positioned at the ILD-SiO₂-Ti corner region, around point "A", where the maximal stresses are localized across a quasi-linear preferred direction, consistent with the cross-section SEM analysis (see Fig.1).

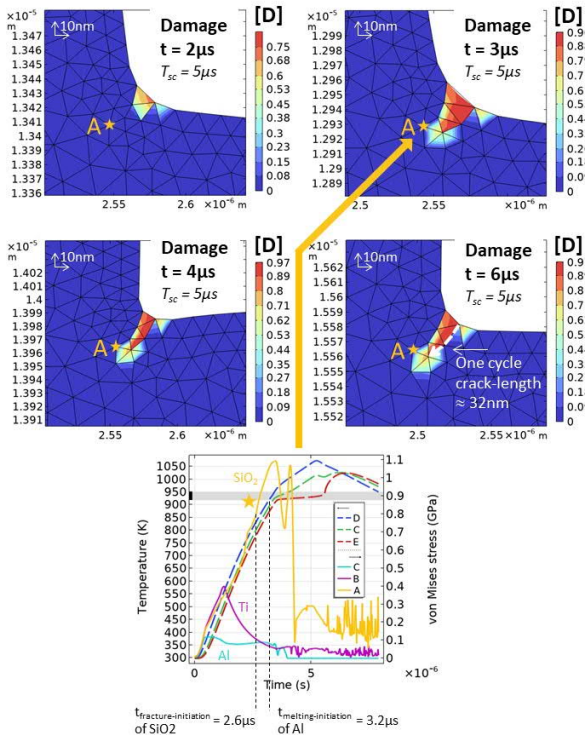


Fig.6 ILD-SiO₂ crack damage modeling for a short-pulse SC (5 μ s), based on Rankine's theory, with boundary condition of a constrained-topside. $G_f = 4.5\text{J}\cdot\text{m}^{-2}$ and $\sigma_f = 0.8\text{GPa}$. Specific meshing range: $8\text{nm} < \text{SiO}_2 < 30\text{nm}$, $5\text{nm} < \text{Ti} < 15\text{nm}$. The critical time necessary to reach σ_f is $2.6\mu\text{s}$ ($32\% \cdot t_{\text{scw}}$; $E_{\text{SC}600\text{V}} = 3.69\text{J}\cdot\text{cm}^{-2}$) and the critical time to reach the melting temperature of Al is $3.2\mu\text{s}$ ($40\% \cdot t_{\text{scw}}$; $E_{\text{SC}600\text{V}} = 4.46\text{J}\cdot\text{cm}^{-2}$). Crack opening is less 10nm as calculated by (2) for one-cycle. Note : $E_{\text{SC}} = V_{\text{DS}} \int J_{\text{SC_channel}}(t) \cdot dt$

In Fig.6, for $t < 3\mu\text{s}$ damage is not yet present at point A because σ_f is not reached. For $t = 3\mu\text{s}$, when SiO₂ stress around point "A" reaches the σ_f , the crack clearly penetrates point A, governed by the damage relations (Equations 1-3). It is remarkable to point out that the damage mapping exhibits a visible crack opening displacement consistent with that predicted based on Equation (2). For $t > 3\mu\text{s}$, the cracking shape is frozen because the stress collapses caused by the melting of the Al layer. In this simulation when considering a topside-constrained boundary condition at the upper part of the Al layer, a total crack depth of 32nm is resulted. This value has to be related to the straight-line distance between the corners of the ILD-SiO₂ and poly-Si gate (315nm), giving a consumption of 10% of the total crack length. If the hypothesis of linear accumulation of damage is accepted as with Miner's rule, the critical number of cycles required to crack the entire distance between the corners of ILD-SiO₂ and the poly-Si gate will be $315/32 \approx 10$ cycles. However, such an estimation is clearly the most pessimistic, imposed by the choice of the topside-constrained boundary

compared to experimental results in Fig.1. Certainly, a higher number of cycles is required to allow the complete crack formation, permitting the Al-source metal to penetrate through the SiO₂ material, as observed in Fig.1.

5. Conclusion and future work

A new extended SiC MOSFET 2D Multiphysics model, including Rankine's crack-damage theory applied to the ILD-SiO₂ layer in harsh SC operation, is introduced, implemented, and analyzed. The simulated damage localization and crack-path direction are consistent with the transient 2D stress maps and the SEM cross-sections. Critical time and energy of crack formation in SCs can also be extracted showing that a margin of at least 40% below the t_{scw} must be respected to avoid simultaneously crack initiation and melting triggering. Future work will focus on estimating the critical cycle number range to a possible complete destructive ILD fracturing, depending on the SC pulse time.

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