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Low-Voltage Schottky p-GaN HEMT Properties under Extreme Repetitive Short-Circuit Operation Conditions : 2DEG Pinch-off, Stability, Aging, Robustness and Failure-Modes Analysis [Abstract]

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Abstract

The authors proposed in-depth experimentation and physical analysis showing the extreme robustness capability of low-voltage GaN HEMT in single and repetitive short-circuit. A 2DEG pinch-off behavior is analyzed depending on V_{DS} voltage and charges' trapping / de-trapping relaxation time. A new drain-gate leakage-current mechanism at turn-off is suggested to explain the ultimate thermal-runaway failure-mechanism.

1. Context and purpose of the article

Power lateral GaN HEMT with low voltage (LV) rating are gaining popularity for various new applications. The main ones are future 48 V DC-link automotive power distribution and power electromobility like torque assistance for electric bikes and motor control for light e-scooters and e-motorcycles [1-3]. LV GaN HEMT devices are also increasingly preferred for space applications as a substitute for expensive and limited Rad-Hard silicon MOSFET [4]. So far, except for specific cases like multilevel converters [5], LV GaN HEMT device has not been a significant part of the power conversion stages in power-chain. These are typically the high-voltage network side stage, also named "Active Front-End Converter (using Power Factor Controller)", and the motor-inverter side stage, also named "Active Back-End Converter". These two conventional power stages require at least medium voltage (MV) or high voltage (HV) devices and must endure harsh environmental and operational conditions such as short-circuits (SC) events. Hence the LV GaN HEMT devices have not been extensively studied in extreme operation than their MV and HV counterpart. However, with the anticipation of future 48V power applications and the importance of "embedded distribution and actuator" applications, it appears crucial to explore the specific properties of LV GaN HEMT in SC events with the same attention as for MV counterparts. Ref. [6] in 2013, is probably the first on SC-LV GaN HEMT but no physical analysis were included, and repetitive SC was not performed. Today in 2024, the bibliography appears limited : partial and non-

exhaustive data are available in manufacturer reliability reports [7] and seem to show a higher level of robustness than MV/HV devices rating. Over the past two years, however, two articles have caught our attention in repetitive SC-100 V GaN HEMT : [8] focuses on the AlGaN barrier – p-GaN stack interface defects impact on the drift – recovery behavior under 48 V-70 V bias stress and [9] investigates the possible hot-electron induced permanent defects at high electric field (60 V-70 V bias stress). This submission presents our contribution from dedicated intensive in-depth experimentation protocol "on-line stress - off-line monitoring on curves tracer" and physical analysis. The abstract is organized as follows: section II covers the dedicated test bench and the LV DUTs used; in section III the special 2DEG pinch-off property is analyzed in low energy SC; in section IV the 2DEG drifts will be depicted for repetitive long-time pulse and high energy SC including the special transient drain-gate leakage current at turn-off; in this last section a thorough analysis of the de-trapping charges relaxation-time and possible aging effect using a dedicated single ultra-short-pulse SC is presented; finally in Section V, destructive operations and failure-mechanisms are investigated in ultra-long-time pulse / high energy proving the exceptional robustness capability of LV GaN HEMT in all short-circuit conditions.

2. Test bench, DUT stressed, and Protocol used

Fig. 1 (a) shows an overview of the designed "easy-to-use modular plug-in" boards to perform SC: a generic motherboard includes the film capacitors bank and the

electronic fuse-breaker safety stage, a daughter board was designed to reduce the stray inductance of the downstream switching loop using ceramic capacitors and including a wide bandwidth / current range sensor (10 mΩ / 2 GHz). DUTs are soldered on a dedicated plug-in board as shown in Fig. 2 (b), including measurement vias for the scope on the top side and leads on the bottom side for off-line and off-bench measurements using a B1505A curve tracer. The gate-driver board and DUT's board are soldered edge-to-edge using two metalized half-cut vias on each board. DUTs ref. are recent 100 V-7 mΩ@25 °C commercial devices, enhancement-mode Schottky p-GaN gate-type and mains features/gate drive parameters are depicted in Tab. 1. Note that main stresses are performed at $2/3 \times BV_{DSSmin}$ (100 V) = 67 V as is commonly specified by end-users and/or datasheet for SC practical qualification test.

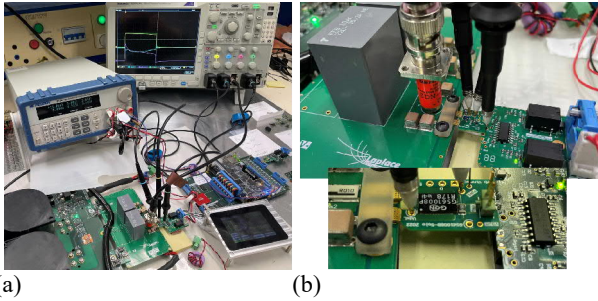


Fig. 1 (a) SC test bench overview, (b) modular easy-to-use and single-use DUT PCB plug-in with gate-driver for Ref. A (below) and B (above).

Table 1 DUTs description (a dozen of each are used, Ref. B are divided into two sets: first and second set)

DUT	Ref. A ⁽¹⁾	Ref. B ⁽²⁾
I_D (25°C)	90 A	16 A
Active area	7.32 mm ²	3.75 mm ²
Case type	Epoxy-based PCB material	Naked die with solder bumps
Gate voltage	+6 V/-3 V	+5 V/0 V
Gate resistors	$R_{GON}/R_{GOFF-SSD} : 10 \Omega/100 \Omega$	

Note: SSD is an acronym of (SC) Soft-Shut-Down

3. 2DEG pinch-off property in low-energy single-pulse SC (abstract)

Preliminary, to avoid thermal influence and to guarantee safe testing, a 200 ns short-time pulse under incremental drain-source voltage bias is performed in Fig. 2 (a) and (b) for DUT ref. A and B. A 2DEG pinch-off effect is highlighted depending on V_{DS} bias : the SC current decreases for higher V_{DS} . In Fig. 2 (c), to confirm this original property, a permanent pulse is applied under low energy storage and a continuously decreasing drain-source voltage. The 2DEG pinch-off depending on $V_{DS} \geq (V_{COSS_knee} + V_{GS})$ is clearly visible, just like the transition to the quasi-ohmic conduction for $V_{DS} < (V_{COSS_knee} + V_{GS})$, leading to a stronger 2DEG current

density as a bell-like shape as seen in quasi-static $I_{DS}(V_{DS})$ curve [8]. In Fig. 2 (c) the device's self-heating cannot be neglected given the long-pulse used, however our background analysis regarding the pinch-off effect is preserved as graphically marked in dashed-line on $I_{DS}(t)$ waves. Finally, the 2DEG pinch-off intensification caused by the lateral-field plate HEMT structure at high drain-source voltage bias tends to mitigate the power density and then the temperature rise. As long as the p-GaN gate stack edge is protected from the electric field peak, this behavior appears to be favourable overall for LV GaN robustness, as it will be presented in §5. This property is clearly opposed to what is known for classical vertical power devices. In addition, the high current rise through the stray inductance of the switching loop at turn-on leads to a strong relative value drain-source voltage drop which reduces the local transient power density and the thermal stress in LV GaN much more than in the case of HV Si, SiC and GaN power devices in same operation conditions. This property contributes to avoiding early thermal runaway, as will be illustrated in §5.

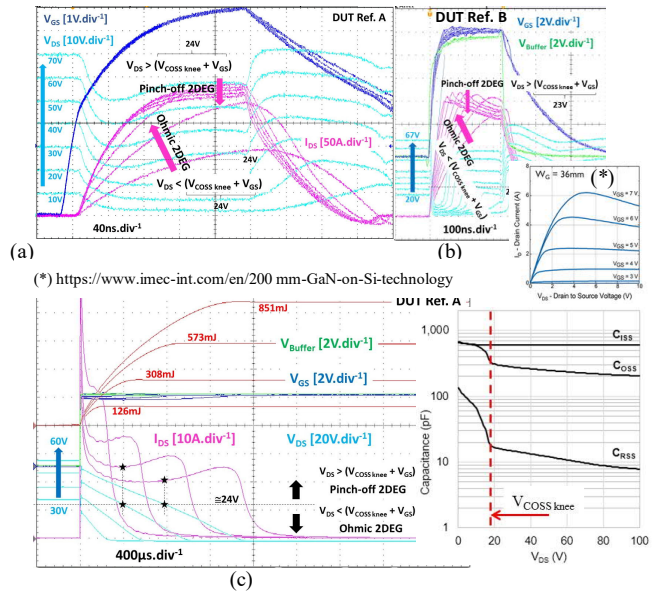


Fig. 2 2DEG's pinch-off transient behavior in SC operation, under (a) 200 ns short-pulse for DUT ref. A [$6.2 \text{ kA} \cdot \mu\text{s}^{-1}$, $1.7 \text{ kW} \cdot \text{mm}^{-2}$], (b) 200 ns short-pulse for DUT ref. B [$8.8 \text{ kA} \cdot \mu\text{s}^{-1}$, $3.8 \text{ kW} \cdot \text{mm}^{-2}$] and (c) permanent-pulse with low energy storage on the motherboard (the external DC power supplied is disconnected). Note: V_{COSS_knee} ref. A and B $\cong 18 \text{ V}$ and from the datasheet, then from Tab. 1 giving the gate voltage drive, $V_{COSS_knee} + V_{GS} \cong 24 \text{ V}$ for DUT ref. A and $V_{COSS_knee} + V_{GS} \cong 23 \text{ V}$ for DUT ref. B.

4. 2DEG drift and de-trapping relaxation delay-time, aging and drain-gate transient leakage under long-time high-energy repetitive-pulse SC (abstract)

Single and repetitive pulses under long-time SC ($\sim 10 \mu\text{s}$) at high-energy operation conditions are now analyzed in Fig. 3 (a) and (b). The saturation current exhibits a strong decrease caused by the electrons'

mobility decrease at high-temperature rise and amplified by the source-contact ohmic drop-voltage of the lateral structure. In addition, a strong Metal/p-GaN Schottky-barrier gate leakage-current arises, leading to a slight gate-source voltage-drop through the external gate-resistor and then reinforcing the decrease of the saturation current. The power-density and temperature self-limiting properties lead to an impressive SC withstand time capability (T_{SCW}) higher than the 10 μ s standard value: $T_{SCW, REF.A [67V]} > 300 \mu$ s, $E_{critical, REF.A} > 6.8 \text{ J.cm}^{-2}$ and $T_{SCW, REF.B SET 1 [67V]} = 22 \mu$ s, $E_{critical, REF.B SET 1} \cong 2.7 \text{ J.cm}^{-2}$. Such extreme SC robustness can also be obtained for an HV device as long as the first transient power-peak over the first few hundred ns analyzed in §3 is withstood [11]. This condition is not required for LV devices. Note that the extreme robustness of Ref. A can also be explained in part by its Epoxy-based PCB material case where internal copper layers and vias act as thermal spreaders. In addition, gate-leakage monitoring provides a relevant thermal diagnosis [12] and a means of SC detection [13].

Repetitive SC-pulses reveal a continuous decrease of the 2DEG conductivity, probably caused by bulk electrons trapping, leading to a further decreased saturation current clearly visible at the beginning of the SC after the 2DEG peak but just before the temperature effect becomes dominant. To confirm this hypothesis, a $C_{OSS-RSS}(V_{DS})|_{V_{GS}=0}$ curve in the off-bench is suggested in Fig 4 (a) for Ref. B, highlighting a positive drift of the $V_{COSS, 2nd \text{ knee}}$ (24 V to 27 V) with a field-plate influence, which could be caused by a trapping effect around the AlGaIn gate-region. $I_{DSS}(V_{DS})$ curve shows a spectacular leakage decrease by repetitive SC annealing-effect (Fig. 3 (e), $I_{DSS} > \mu$ A to nA at 100 V) for Ref. A. $I_{GSS}(V_{GS})$ curve highlights also a hole injection decrease in Fig. 4 (b) for Ref. B, as in Fig. 3 (a) and confirmed in [8]. In the full paper, the authors will show that trapping and leakage signatures are not regular as a function of the number of SC cycles: it occurs essentially after the first cycles, probably rapidly saturating traps.

In Fig. 3 (c) and (d), re-using an SC ultra short-time single-pulse to avoid thermal influence as in §3, it is interesting to realize that a quasi-complete device restoring by de-trapping effect can be performed on Ref. B after a 1 month relaxation time at $V_{GS}=V_{DS}=0$ V and at T_{ROOM} , as analyzed in [8]. In contrast, Ref. A does not exhibit restoring, which leads us to believe that the 2DEG pinch-off drift could be more attributed to an aging mechanism caused by hot-electron under high electric field [11] and not directly to a trapping effect as Ref. B. In Fig. 3 (a), it can also be seen a gate-source leakage decrease. As suggested by [8], channel electrons are captured but the Metal/p-GaN/AlGaIn interface defects, elevating the potential barrier and reducing the gate-stack hole injection, leading to a slight reduction of the transient gate leakage-current.

Finally, a last important property is now visible at the SC turn-off: a drain-gate transient leakage-current

tail over some tens μ s is clearly visible in Fig. 3 (b) for a long-time SC-pulse and at high energy. This leakage could come from the p-GaN/AlGaIn PIN diode reverse conduction under the electric-field peak, gate's field-plate side, at high-temperature conditions. Deeper analyses are in progress. This reverse gate-current flows from the gate to the source electrodes across the external gate-resistor and leads to a gate-source voltage increase which tends to maintain the 2DEG not fully pinched-off with a residual drain – source leakage (some amps) : $0 \text{ V} + R_{GOFF} \cdot |I_{GS}(t)| \cong V_{GSTH}$ or $> V_{GSTH}$. As it will be seen in §5, this mechanism can initiate a fatal thermal runaway of the device at the SC turn-off.

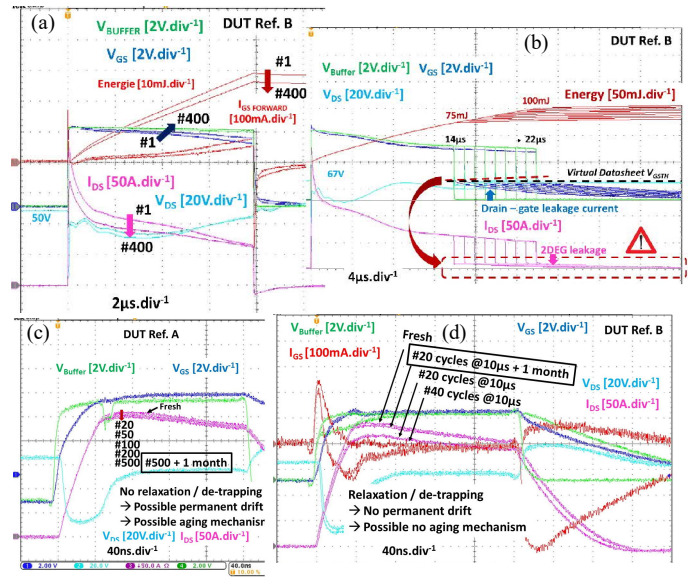


Fig. 3 2DEG behavior under long-time repetitive-pulse at high-energy (a) DUT Ref. B 2DEG pinch-off drift from #1 to #400 cycles at 8 μ s medium-time pulse SC (b) DUT Ref. B incremented SC-pulse and drain-source leakage at turn-off (c) DUT Ref. A probable aging effect (no de-trapping relaxation after #500 cycles at 10 μ s SC-pulse) (d) DUT Ref. B de-trapping relaxation after #20-40 cycles at 10 μ s SC-pulse (e) DUT Ref. A SC annealing-effect after #600 cycles at 10 μ s SC-pulse.

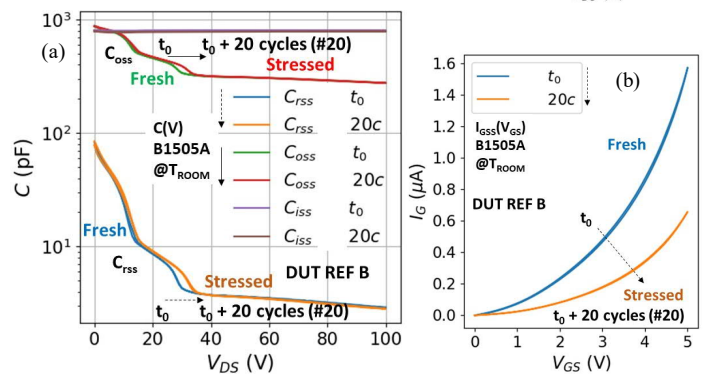


Fig. 4 DUT Ref. B curve tracer signatures from #0 (t_0) to #20 cycles at 10 μ s SC-pulse (a) all C(V) behavior (b) gate-source leakage $I_{GSS}(V_{GS})$.

5. Robustness and failure-modes in ultra-long-time or permanent-pulse SC (abstract)

Finally, SC in ultra-long-time (ms range) or permanent-pulse is performed and analyzed in Fig. 5, including possible destructive modes. In Fig. 5 (a), Ref. A is specifically stressed in permanent-pulse mode due to its extreme SC energy robustness, as seen in §4. This device exhibits hard gate-damage at 7.2ms, leading to a current overload of the gate-driver's auxiliary supply and the gate-source voltage collapse below the threshold: a spectacular 2DEG soft and self-turn-off appears. Unfortunately, this 2DEG secure pinch-off effect is not fully performed, and a residual drain-source leakage leads to a delayed thermal runaway and the destruction of the device. Future work is planned to isolate the self-turn-off property and to perform gate-region failure analysis. In Fig. 5 (b), Ref. B (second-type set stressed) is now stressed with an incremented ultra-long-time to reach its T_{SCW} and to reveal the failure-mode. As it will be discovered previously in §4 at the SC turn-off, a strong transient drain-gate leakage-current maintains the gate-source voltage near the threshold ($R_{GOFF} = R_{SSD} = 100 \Omega$) and does not provide a uniform and effective 2DEG cut-off, leading to a quick thermal runaway and the final destruction of the device. Using a lower R_{GOFF} value ($R_{GOFF} < 100 \Omega$) this failure-mode could probably be delayed but with an unacceptable practical over-voltage at the SC turn-off.

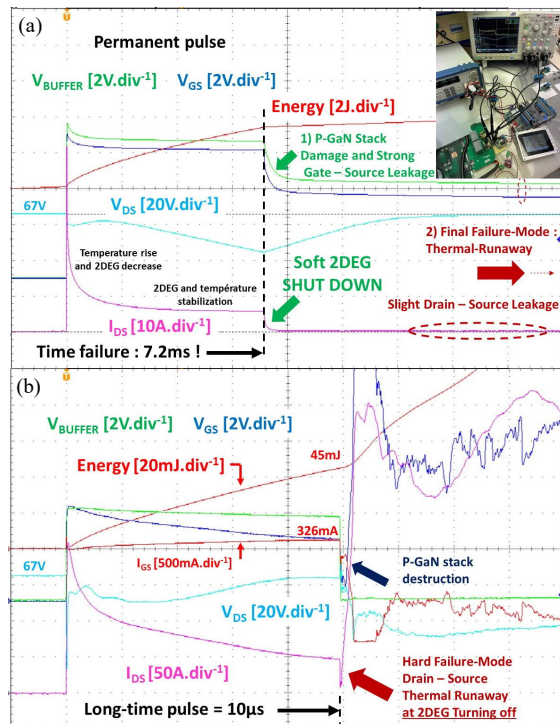


Fig. 5 Failure-modes analysis in high-energy SC (a) DUT Ref. A permanent pulse showing hard gate-damage and soft self 2DEG turn-off at 7.2 ms afterward, giving a residual drain-source gate leakage and a delayed final destructive thermal runaway (b) DUT Ref. B quick and hard thermal runaway at turn-off by drain-gate transient leakage.

6. Conclusion (abstract)

Intensive in-depth experimentation and physical analysis demonstrate the extreme SC robustness capability of LV HEMT GaN in single and repetitive SC operation conditions mainly performed at $2/3 \times BV_{DSSmin}$ on a dedicated, modular and integrated test bench. The 2DEG pinch-off behavior, depending on the $V_{COSS\ knee}$ value and the electrons trapping, was studied using the $C_{OSS}(V_{DS})_{V_{GS}=0}$ curve in off-bench. A drain-gate transient leakage-current tail is also highlighted at SC turn-off, maintaining the gate-voltage near the threshold, leading to the 2DEG not fully cut-off and a destructive quick thermal-runaway failure-mode.

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