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The detection capability of GaN-based nano-diodes is measured up to 110 GHz in two configuration schemes: voltage and current responsivity. The ratio between both figures of merit allows to extract the AC resistance of the diode, showing a very flat value in all the frequency span. An optimization on the geometrical parameters is performed, finding that the narrower the channel, the higher the voltage responsivity, and the higher the number of channels in parallel, the higher the current responsivity. The expected dependence of the noise equivalent power with the width and number of channels is confirmed. The proposed configuration for best performance of these devices as RF detectors is to allocate the maximum number of channels in parallel and operate in current responsivity mode.

Nowadays, as mature technologies are reaching their limits, as an alternative to traditional devices, the electronics community is exploring other topologies or materials to push their operation to higher frequencies. In the case of RF and THz detectors at room temperature, state-of-the-art III-V FETs are being used in the last years to operate as detectors showing a voltage responsivity $\beta_V$ of 8.5 kV/W at 300 GHz for a GaAs HEMT[1], 2.2 kV/W at 1 THz for a dual-grating-gate InGaAs/InAlAs/InP[2] or 15.5 kV/W at 0.14 THz for a GaN HEMT[3], just for giving some examples. In (the references) 4 and 5, a complete review of the state-of-the-art FET-based THz detectors is presented. However, despite the advances made in recent years with FETs, the classical technology for THz detection is still based on passive Schottky barrier diodes (SBDs). Among them, the GaAs SBDs commercialized by Virginia Diodes (VDI) are the benchmarking reference for THz devices.[6] The state-of-the-art of high frequency response corresponds to a zero-bias detector working up to 5.56 THz based on a SBD produced by ACST GmbH.[7]

As an alternative, in this contribution we explore a planar structure that can favor the coupling with free-space radiation and the operation at high frequencies due to reduced parasitic capacitances,[8] the *Self-Switching Diode* (SSD) proposed by A. M. Song in 2003.[9] In the top of Fig. 1 a drawing of its geometry is presented. Its working principle resembles the FET operation, but in an asymmetric planar structure where a lateral field-effect modulates the width of a nanochannel and generates a non-linear behavior. SSDs provide significant detection responsivities, confirmed experimentally in the sub-THz and THz ranges at room temperature in several semiconductor materials, like GaAs,[10] InGaAs,[11] InAs,[12] GaN,[13] Graphene,[14,15] ZnO,[16] SOI,[17] or poly(3-hexylthiophene).[18] At cryogenic temperatures, their broadband power detection capability can even be improved, reaching 2.5 THz below 60 K, as shown in Ref. 19 for InGaAs SSDs. However, less attention has been paid to the potential reduction of the other key figure of merit of power detectors, the noise equivalent power (NEP), corresponding to the lowest power level which can be detected over the noise generated by the detector itself. Thanks to the fabrication of SSDs consisting in arrays of multiple channels in parallel,[20] the value of the NEP can be decreased, thus enhancing the sensitivity of the detection. In this work, we focus on the optimization of the NEP at zero bias, where the generation of excess noise is minimized, as well as power consumption. The analysis of the improvement of the detection with SSDs by means of the optimum choice of the device geometry was already presented in Ref. 21, but without paying attention to $\beta_I$ (in A/W) and relying just on DC measurements. As novelty, we will show measurements up to 110 GHz, and not only for the voltage responsivity, $\beta_V$, but also for the current responsivity, $\beta_I$, which has so far only been examined in single SSDs.[22]

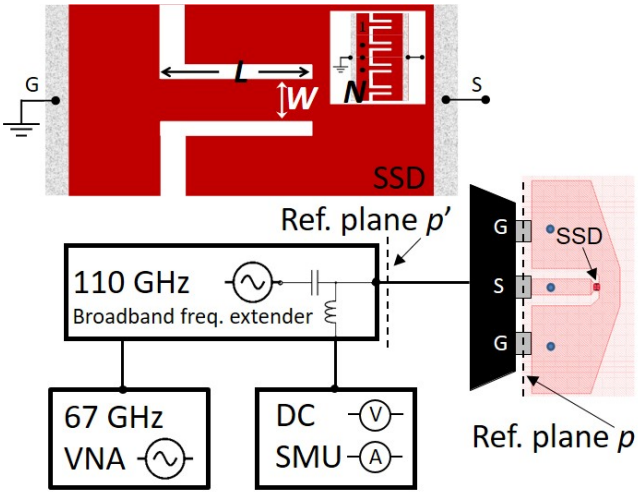


FIG. 1. Geometry of the SSD with length $L$, width $W$ and $N$ channels in parallel. Experimental setup to carry out the GSG (100 $\mu$m pitch) on-wafer measurements up to 110 GHz.

In the case of GaN-based diodes, which will be the mate-

rial system used in the devices under test in this paper, the best results for SSDs are $\beta_V$ of 2 and 0.3 V/W at 0.30 and 0.69 THz, respectively,[23] which can be much improved in gated-SSDs, providing 600 V/W at 0.3 THz.[24] Similar gated nanowire field-effect rectifiers (NW-FERs) also exhibit an excellent value of 3 kV/W, but at lower frequencies of 10 GHz.[25] However, in both cases their performance should be compared to that of other active devices, like the previously commented FETs. Compared with higher mobility semiconductor competitors, GaN SSDs may handle superior power levels due to its wide bandgap.

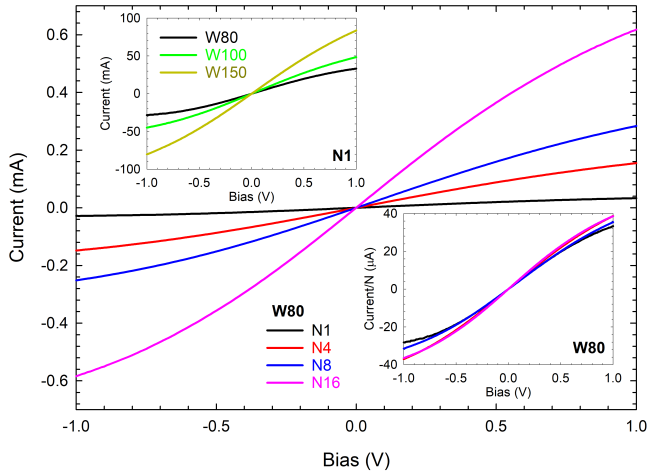


FIG. 2. DC $I$-$V$ curves for arrays of $L$=2 $\mu$m long and $W$=80 nm wide SSDs. The number of channels in parallel are $N$=1, 4, 8 and 16. The bottom right inset shows the current per channel. The top left inset shows the $I$-$V$ curves in the case of $N$=1 for three widths $W$=80, 100 and 150 nm.

The devices under analysis, whose $I$-$V$ curves are shown in Fig. 2, consist in diodes with multiple channels in parallel, $N$, all of them with the same length, $L$=2 $\mu$m. Six devices will be compared in this work to extract the impact of $N$ and channel width $W$ on $\beta_V$, $\beta_I$ and NEP: SSDs with a single channel, $N$=1, and different widths, $W$=80, 100 and 150 nm; and devices with the narrowest width, $W$=80 nm, and with different number of parallel channels, $N$=1, 4, 8 and 16. The SSDs were fabricated on a commercial AlGaN/GaN heterostructure grown on a Si substrate by EpiGaN, consisting of 25 nm of $Al_{35}Ga_{65}N$ on top of 1.5 $\mu$m of GaN (and passivated with 3 nm of SiN). More details about the fabrication can be found in Ref. 13. Fig. 2 confirms the quality of the technological process, the current showing almost perfect scalability with $N$ and $W$.

While the physics of SBDs is known in detail and an analytical model for their $I$-$V$ curve is well established in the literature, in the case of SSDs few works deal with a physical-based interpretation of their behaviour.[26] Only A. Westlund et *al.* analyze in Ref. 27 and 28 how the geometrical and material parameters affect the key figures of merit of SSDs as detectors, such as $\beta_V$ and NEP. In such work, the non-linear behaviour of SSDs was conceptually explained through the analogy with an enhancement-mode MOSFET in the triode region by imposing $V_{GS} = V_{DS}$. In fact, the regions surrounding the channel of the SSDs act like the gate in a MOSFET (in lateral position in this case, with the trenches acting like the gate dielectric), and since the voltage applied to the anode reaches those regions, it is like if $V_{GS} = V_{DS}$. The flow of electrons along the nano-channel is controlled by such lateral field effect, thus leading to a non-linear $I$-$V$ curve. Within this model, the resistance, $R$, and the bowing coefficient, $\gamma$, of the $I$-$V$ curve can be expressed in terms of characteristic parameters of the semiconductor and of the geometry of the SSDs as follows

$$R = \left(\frac{\partial V}{\partial I}\right) = \frac{L}{q n_s \mu_n W_{eff} N} \propto \frac{1}{W_{eff} N}, \tag{1}$$

$$\gamma = \left(R \frac{\partial^2 I}{\partial V^2}\right) = \frac{2C}{q n_s W_{eff}} \propto \frac{1}{W_{eff}}, \tag{2}$$

where $q$ is the electron charge, $n_s$ the sheet electron concentration, $\mu_n$ the electron mobility and $C$ the capacitance of the "gate" (related to the geometry of the trenches). It is to be noted that to be correct, instead of $W$, the appropriate parameter is the value of the effective channel width $W_{eff}$, that takes into account the lateral width $W_d$ of the area depleted by surface charges at the channel sidewalls ($\approx$ 25 nm at each side).[29] Applying the general theory of square-law detectors,[30] it is straightforward to express the zero-bias optimum responsivities as

$$\beta_I^{opt} = \frac{1}{2}\gamma; \quad \beta_V^{opt} = -\frac{1}{2}\gamma R. \tag{3}$$

It is important to note the sign change between voltage- and current-detection schemes, not typically explained in the literature. It comes from the change in the curvature of the $I$-$V$ with respect to the $V$-$I$ curves, related to whether the device is biased with zero-current or with zero-voltage.

In a general case, the SSD in not impedance-matched with the RF source (with characteristic impedance $R_0$=50 $\Omega$), so that the power reflection factor $(1 - |\Gamma|^2)$ must be taken into account in order to calculate the practical responsivities (which are much lower than the optimum ones). In our case, as the SSD is in strong mismatch $R(k\Omega) \gg R_0$ (see Ref. 21), we obtain

$$\beta_I = 2\frac{R_0}{R}\gamma \propto N; \quad \beta_V = -2R_0\gamma \propto \frac{1}{W_{eff}}. \tag{4}$$

Concerning the value of the NEP, it can be estimated by using the Nyquist theorem (neglecting any excess noise) as

$$NEP = \frac{\sqrt{4k_B T/R}}{\beta_I} \propto \sqrt{W_{eff}/N}, \tag{5}$$

being $k_B$ the Boltzmann constant and $T$ the ambient temperature. Note that a definition of NEP using $\beta_V$, leading to the

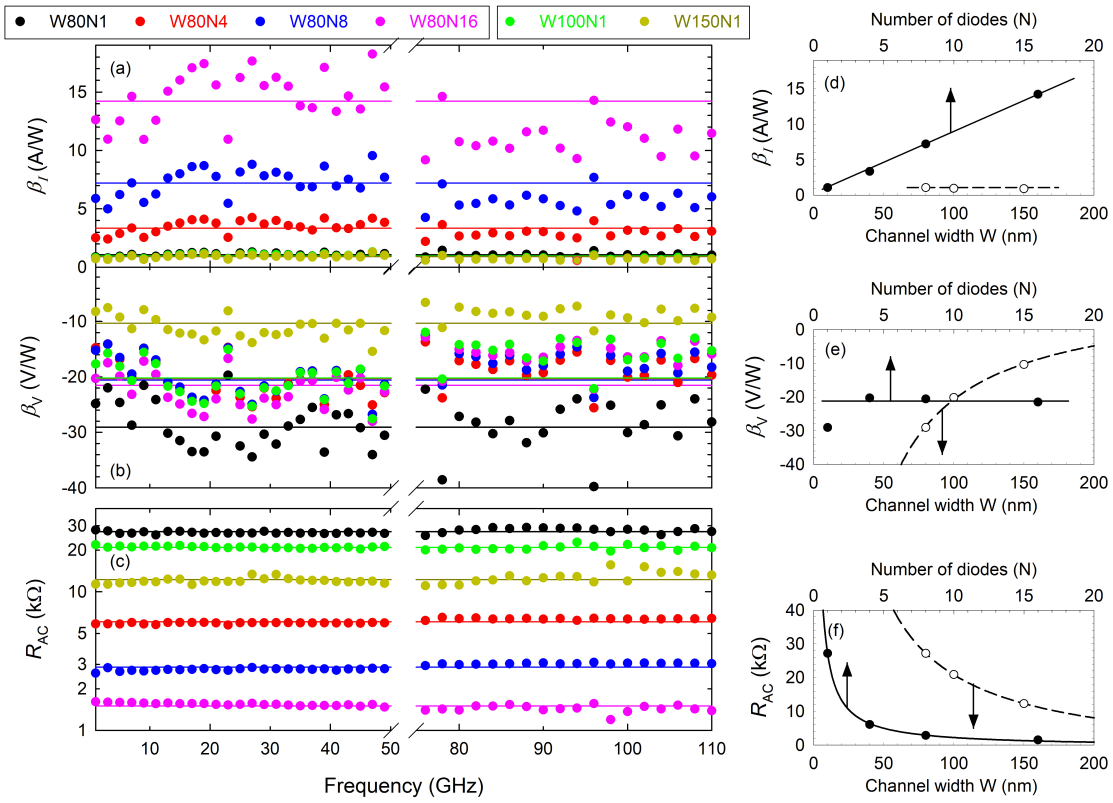


FIG. 3. Experimental responsivities: (a) $\beta_I$ at zero voltage and $\beta_V$ at zero current as a function of the frequency of the input signal, reaching 110 GHz. (c) Resistance, $R_{AC}$. In all the cases the average along the whole frequency span has been added for guiding the eye. The 50-75 GHz range has been omitted due to the absence of a power-meter for calibration. Dependence (in empty circles and bottom x-axis) on the channel width, $W$, and (in filled circles and top x-axis) on the number of parallel channels, $N$, of the (d) zero voltage responsivity, (e) zero current responsivity and (f) the AC resistance. Dashed and solid lines show the tendencies according to eqs. 4 and 7

same value, can also be used. Our main objective is to verify the predicted dependencies of eqs. 4 and 5 on $N$ and $W$ in the fabricated structures, providing design guidelines for future improvement of the detection performance of SSDs.

When the diode is zero voltage (current) biased and it is fed with an RF input signal of frequency $f$ and power $P$, a DC current shift $\Delta I$ (DC voltage shift $\Delta V$) appears, which is the measured output signal. The current responsivity $\beta_I$ (voltage responsivity $\beta_V$) is defined as the ratio between the DC output signal and the injected power:

$$\beta_I(f) = \frac{\Delta I(f)}{P}; \quad \beta_V(f) = \frac{\Delta V(f)}{P}. \tag{6}$$

For zero voltage (current) bias, a SMU was used to impose the null excitation voltage (current) and measure the output current (voltage). The RF signal was generated by means of a Keysight N5251A Single Sweep Solution (10 MHz to 110 GHz) Millimeter Wave System, either directly from the internal source of the VNA at base frequency range (up to 67 GHz), or by frequency-multiplying the source with a frequency extender, see Fig. 1. In order to deliver a precisely known power $P$ at the reference plane $p$ of the SSD we perform (i) SOL calibration with 1.0 mm calibration kit at $p'$, (ii) on-wafer SOL calibration with Integrated Standard Substrate at $p$, and (iii) power calibration at $p'$ in the 75-110 GHz band (thanks to a power-meter). Calibrations (i) and (ii) are carried out to determine the losses in the cables and the probes so that the output power of the VNA can be adjusted to assure that a constant incident power reaches the DUT at $p$. The power calibration (iii) is an additional step which allows to precisely know the absolute value of the power reaching $p'$, correcting the uncertainties introduced by the frequency multiplier at the highest frequency band. A macro code was implemented in MATLAB to automate the control of the instruments and set the actual incident power to $P$=-5 dBm. All measurements have been performed in the dark and at room temperature.

The results of the microwave responsivities $\beta_I$ and $\beta_V$ are plotted in Fig. 3(a) and (b), respectively, showing both an almost perfectly flat response. Although the characterization was executed using a 1 GHz step, here we show only half of the points for better visibility. In very good agreement with the theory, $\beta_V$ is almost independent of $N$ but strongly affected by the channel width [see Fig. 3(e)]. The slight decrease of the responsivity with $N$ is due to the improved impedance matching as reported by eq. 5 of Ref. 21. As expected, a smaller $W$ leads to a nearly pinched off channel, which increases the non-linearity at zero bias, thus improving significantly the re-

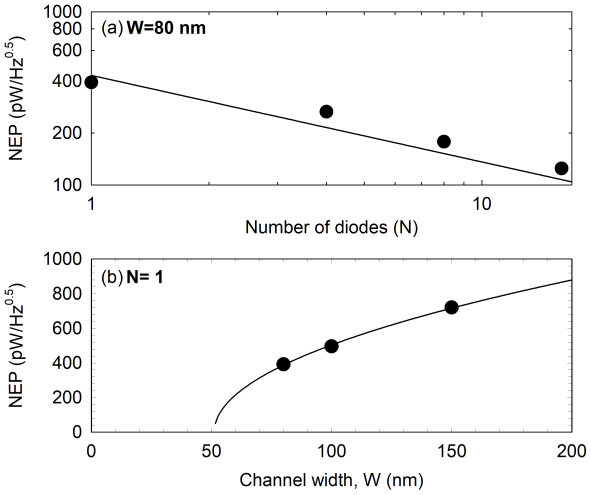


FIG. 4. NEP calculated using eq. 5 as a function of (a) the number of channels in parallel, $N$, and (b) the channel width, $W$. The theoretical dependencies given by eq. 5 are plotted as solid lines, $1/\sqrt{N}$ in (a), and $\sqrt{W-2W_d}$ in (b).

sponsivity. However, in the case of $\beta_I$ the preferred option is to accommodate several channels in parallel, which, by decreasing the impedance, improves the input power mismatch and provides a larger output current. Fig. 3(d) clearly demonstrate the prediction of eq. 4. From eq. 3 it is possible to define a frequency dependent output resistance $R_{AC}(f)$ of the diode as

$$R_{AC}(f) = -\beta_V(f)/\beta_I(f). \quad (7)$$

Figure 3(c) shows how $R_{AC}(f)$ presents an extremely flat value, indicating that the typical minor ripples observed in the responsivities are originated by a non perfect estimation of the RF power injected into the device due to the multiple reflections of the RF signal produced by the mismatch of the diode with the 50 Ω source. Again, the expected dependencies from eq. 1 are clear, the resistance goes as $1/N$ and $1/W_{eff}$. We have checked that these resistances are exactly the same as the ones derived from the DC curve. In addition, using the definition of the effective width $W_{eff}$=$W-2W_d$ and from the fitting of both $\beta_V$ and $R_{AC}$ vs. $W$ we can also extract the lateral depletion $2W_d$ to be ∼50 nm, in perfect agreement with previous measurements.[29]

To conclude, in Fig. 4 we compute the NEP with eq. 5 using for $R$ the values previously obtained for $R_{AC}(f)$, shown in Fig. 3(c). The predicted dependencies on $N$ and $W$ are successfully satisfied. And again, from the fitting of NEP vs. $\sqrt{W-2W_d}$ a value of $W_d$ ∼25 nm is obtained. In Ref. 21 we demonstrate that the minimum NEP is achieved when the impedance matching is condition $R$=$3R_0$ is fulfilled. In our case, for W80 the required number of channels in parallel will be $N = R_{N1}/3R_0 = 200$, where $R_{N1}$ is 30 kΩ [see Fig. 3(c)]. This will allow an important decrease of a 4.6 factor of the NEP to reach a predicted value of 85 $\mathrm{pW/Hz^{1/2}}$ with just a slight degradation (1.8 factor) of the $\beta_V$ [see again see Fig. 3(e)] with respect to a single-channel SSD.

In conclusion, a broadband flat response up to 110 GHz has been demonstrated both for zero-bias voltage and current detection with SSDs based on AlGaN/GaN at room temperature. By measuring diodes with different topologies, the expected dependencies of the figures of merit of detection on geometrical parameters have been confirmed. In particular, by increasing the number of channels in parallel the detector performances can be optimized, since a larger current responsivity and a smaller NEP are obtained.

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