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# Test bench and data analysis towards an on-line Health Monitoring for emerging power modules

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**Abstract—** Electrical conversion in aerospace applications faces important issues to gain in reliability, efficiency and profitability. This paper focuses on preliminary analyses towards condition monitoring for new power modules based on 2D interconnection of SiC power MOSFETs for 600V, 90A applications. Power modules are so far lab-scale samples on which failure analyses and ageing have not been covered. Based on literature, a test plan has been established to trigger expected failure modes. Using temperature-sensitive-electrical parameters, it is expected to identify signatures of failures. In a short-term, laws of failures will be evaluated based on signatures for the prognostic of the lifetime consumption of the module. Paper details the experimental setup, calibration steps and data monitoring towards identification of ageing signatures. Data analyses are detailed

**Keywords—** Health monitoring, Remaining Useful Lifetime, ageing, Power Active Cycling, SiC MOSFET power module.

## I. INTRODUCTION (HEADING 1)

More electrical aircraft requires power modules of higher performances especially in terms of reliability with a control of lifetime. Replacing fluidic systems by electric components is also thought as a good way to increase reliability in systems. Reliability is mostly analysed based on accelerated stress cycles [6]. A large volume of data must be obtained in various conditions to assert a pertinent extrapolation of remaining lifetime during normal operation. Unfortunately, information on reliability is expected at the early stage of development of new technologies of power modules. In parallel, a trend is to embed some condition monitoring functions in power modules to help predict, on-line, the remaining lifetime or modulate the module usage to extend its operation [5, 27]. This approach is the field of hardware developments with respect to sensors and decorrelation methods but mainly dedicated to one particular main failure [7, 9]. When the power semiconductor device is considered as mostly reliable like an IGBT, the lifetime of the power module is related to weaknesses in materials and interfaces in the various interconnections. Indeed, the global thermal impedance of the module is a strong indicator of any emerging defect [1, 3, 12], hence a large literature about junction temperature evaluation from temperature-sensitive-electrical parameters (TSEPs) and compact thermal models [11, 15, 23, 26]. Conceptually, condition monitoring may be obtained from combination of three issues [16] [18]: firstly

the temperature cycling is evaluated generally with a rain flow algorithm [20, 24], secondly, some damage accumulation is computed from models [10, 21], and thirdly, the remaining lifetime is deduced from a combining algorithm [14]. However, in the case of power modules with new geometries, new fabrication process and materials or immature power devices like SiC MOSFETs, a different approach must be considered if a practical implementation of condition monitoring is considered along with the slow process of know-how about failure modes of new power modules. Ahead of this perspective, a preliminary analysis is necessary to define the indicators of failure modes, the way to get information about them and prove that a signature of failure modes is available for a future condition monitoring. The paper discusses such a preliminary analysis based on a novel power module technology with SiC MOSFETs, double-side interconnection and a thermal assistance based on phase-changing principle.

An overview of the expected failure modes in the new power module is given first. Then, it is discussed how triggering realistic failure modes in an accelerated way, to be able to work on failure indicators in laboratory conditions. A test plan has been drawn from other studies in literature to realise a learning phase during which many indicators (TSEPs) have been monitored on a dedicated test bench. A failure signature is then identified for several accelerated ageing profiles. The, this signature will be used in normal operating conditions to help determinate the state of health of the power module. Practical data are discussed to prove the feasibility of a condition-oriented approach along with the development of a power module technology.

## II. STATE OF ART WITH RESPECT TO RELIABILITY OF SiC MOSFET BASED POWER MODULES

This section is dedicated to power module description highlighting relations between each part and the expected failure modes in operation.

### A. Power module description

The proposed power module is planar, as shown in Fig. 1. There is no bonding wire interconnection because it is a typical failure mode in modules [4]. The module substrate is composed of a copper baseplate and a Direct Bonded Copper (DBC) that is a ceramic layer between two copper layers to spread the heat flow. The drain side of transistors is sintered on the DBC (Ag). Gate and source are connected with a Cu-coated polyimide layer. Between these conductive elements, space is filled with an insulating resin.

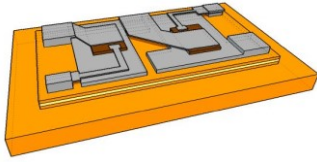


Figure 1: Schematic view of a planar power module composed of a SiC MOSFET phase leg.

### B. Main expected failure modes

This module prevents risks of failure because of lack of wire bonds and also a good choice of materials (DBC) and metallization (Ag, top Cu layer). Main concerns are about Ag promoter on die Al pads, joint cracking [15] and top metallization reconstruction [8] as shown in Fig 2. Concerning the dies, failure modes are related to the gate oxide. The time-dependent-dielectric-breakdown (TDDB) is a stressing way to exhibit gate-related failures as shown in Fig. 3 [2, 19].

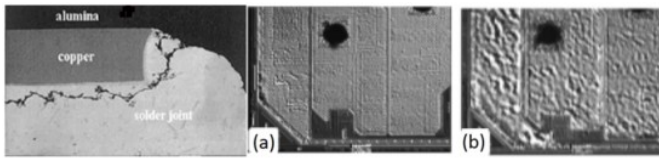


Figure 2: (Left) solder joint cracking [15], (Right) metallization reconstruction (a) healthy sample and (b) damaged sample [8].

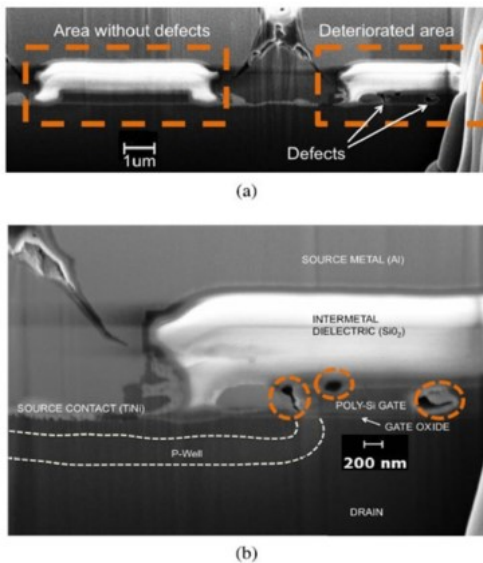


Figure 3: Gate oxide degradation: (a) cells with and without damages, (b) zoom on damages

### C. Failure mode acceleration factors and main precursors

Studies mentioned in Table I have been led on failure mode acceleration factors and indicators. Die temperature is a key element and can be estimated from temperature mapping, thermal models, TSEPs or a combination of latter options. TSEPs have been selected and they are discussed next.

## III. HEALTH MONITORING APPROACH

Fig. 4 pictures the proposed health monitoring approach. In this approach a learning phase is required and will be the main topic of the next sections. For this learning phase,

TABLE I Accelerating factors and indicators of specific failure modes

Failure modes	Acceleration factors	Indicators
TDDB [2, 19]	High temperature Overvoltage on gate Overcurrent between Drain and source	Threshold voltage Gate leakage current On state resistance Drain leakage current
Solder cracks and metallization reconstruction [15, 8]	Active power cycling Passive thermal cycling [27]	Chip temperature Thermal resistance $R_{DS\_ON}$

ageing tests have been chosen. A test plan in two parts has been considered to discriminate die failure modes from general module failure modes and is presented in the following section.

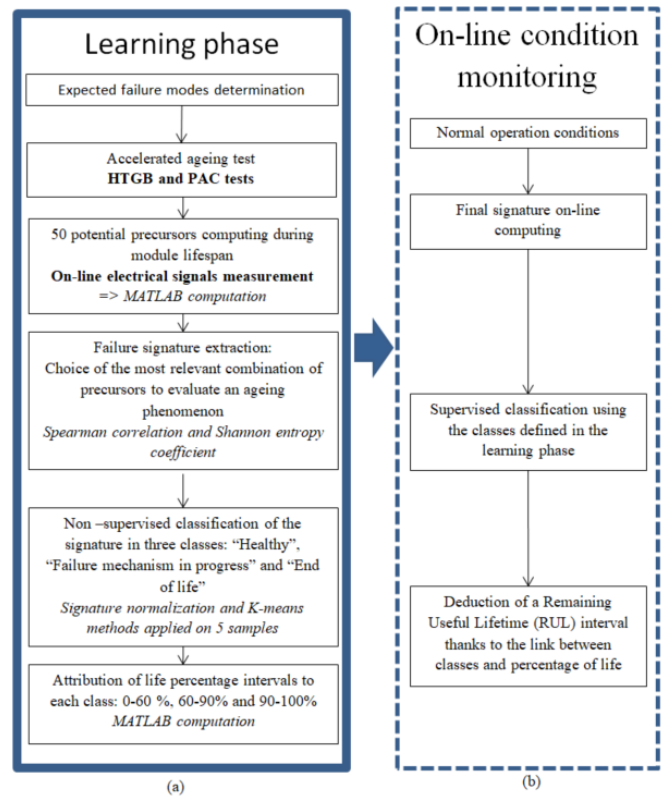


Figure 4: Approach for condition monitoring: (a) learning phase presented in this paper and (b) future work to be implemented

### A. Test plan

The first part of the test plan consists in realizing the JEDEC-standard HTGB test (High Temperature Gate Bias) with a constant gate voltage of 22 V, passive drain-source short-circuit and under an ambient temperature of 200°C. Two characterizations will be performed during ageing to understand and to analyse the drift of indicators. Several potential ageing precursors will be measured thanks to static characterization (B1505 Keysight) and a dedicated Unclamped Inductive Switching (UIS) circuit detailed in section 3.2. The second part is a Power Active Cycling (PAC) presented in Fig. 5, for its realistic approach compared to passive cycling. Only the lower MOSFET in the phase leg will be stimulated (DUT). The upper transistor will be used for its internal diode to close the circuit. The

DUT undergoes alternatively a heating and a cooling phase with a constant drain current between 46 A and 50 A during 1 second and nothing during 4 seconds. The drain current amplitude is related to the temperature swing and so the acceleration level. Full characterization is performed at the end of each cooling phase: TSEP as presented in section 3.3 and a double-pulse test which brings information on MOSFET turn-ON and conduction state, such as threshold voltage or on-state resistance (Fig. 9 and 10). These two phases will allow extracting 50 potential ageing-related parameters that will be described in the last section.

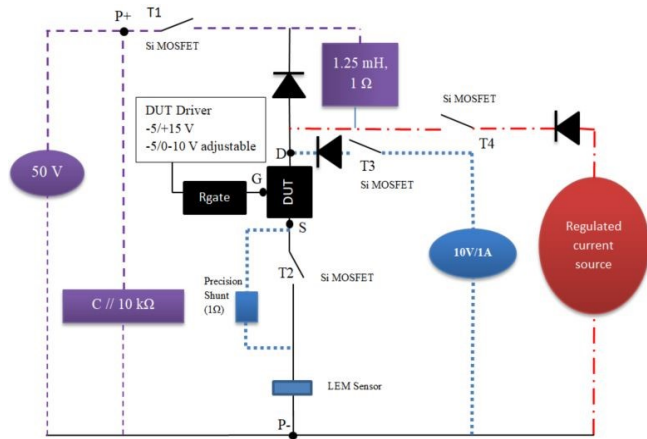


Figure 5: PAC test bench electrical circuit

### B. HTGB test

A test has been set up to impose the same stress to 30 power MOSFETs (a Gate bias of 22 V @ 200°C ambient temperature) in a minimum amount of time. A dedicated UIS test bench [29], has been set up to measure parameters extracted from gate voltage waveform during MOSFET turn-on. The waveform in Fig. 6 is particularly interesting because of the pseudo Miller effect. Miller pseudo-plateau is linked to the threshold voltage which is a good indicator of gate state-of-health.

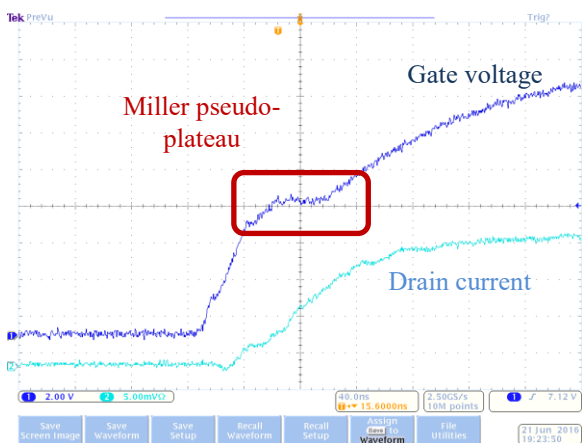


Figure 6: Gate voltage turn-On waveform with a specific Miller pseudo-plateau

Data extracted from this specific ageing test will allow identification of gate failure damage during power cycling tests. Extraction is an automatic script created to find and to isolate the “pseudo-plateau”. Two fittings have been

performed on the de-noised pseudo-plateau, as pictured in Fig. 7. The first fitting is an affine function which gives a slope and an intercept. The second fitting is a 3<sup>rd</sup> order polynomial function which gives 4 parameters. Other parameters as the plateau’s duration, mean level and maxima are also recorded. Finally, calculations of rise times between 0 and 15 V are made. All these parameters have shown a monotonous evolution according to ageing for our three measurements (in healthy state, after 424h and after 664h). After 664h, the threshold voltage has drifted over than 20 %. It has been decided that the degradation was sufficient to select ageing parameters. All the parameters measured on Gate voltage pseudo-plateau will be used in the PAC test bench to discriminate a Gate failure issue from other ones.

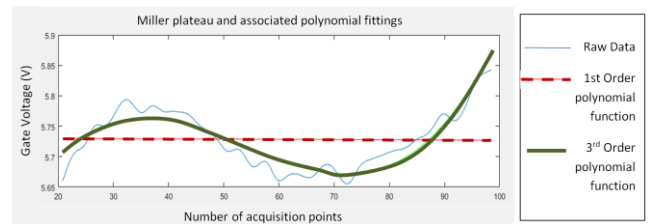


Figure 7: Extraction of parameters from the Miller pseudo-plateau

### C. Junction temperature estimation

So-called die junction temperature estimation is a key element in ageing monitoring. A specific protocol has been presented in [13]. It deals with the estimation of a temperature value: the TSEP calibration and its on-line computation. The chosen TSEP is the transconductance (drain current for a low gate voltage). A new method of temperature extraction thanks to a data map, allows improving accuracy as pictured in Fig. 8. Before the cycling test, a preliminary calibration is realized. A voltage is applied to the gate at a known ambient temperature and the drain current is measured. This operation is repeated for several values of gate voltage and ambient temperature values to obtain the calibration dataset. For on-line computation, the value of gate voltage and drain current are measured and an optimization algorithm places the measured point ( $V_{GS}/I_{DS}$ ) on the previous map. If the couple  $V_{GS}/I_{DS}$  is already known, the corresponding temperature is given (interpolated surface). If the couple  $V_{GS}/I_{DS}$  is not known, the algorithm places the measured point at the most relevant place to estimate the temperature (test points).

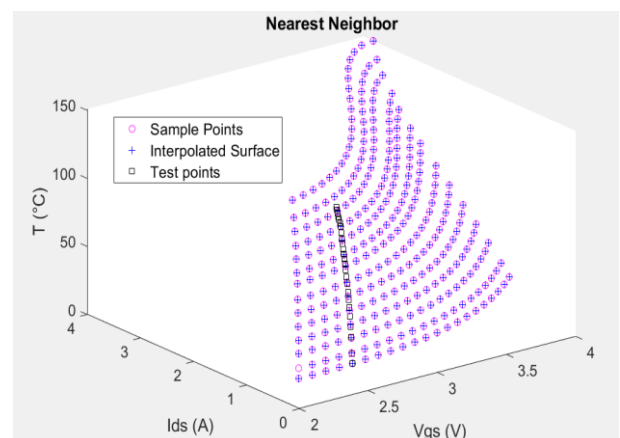


Figure 8:  $I_{DS}$  vs  $V_{GS}$  map for temperature estimation

#### IV. EXPERIMENTAL PAC SETUP

As described in Fig. 5, the PAC test bench allows an accelerated lifetime thanks to an electrical stress which creates successively self-heating and cooling phase in the DUT. During these cooling phases, on-line characterizations are performed. The first one called *TSEP phase* is performed during uneven cycles and the *double-pulse phase* is performed during even cycles. TSEP phase consists in recording successively the couple  $I_{DS}$  and  $V_{GS}$  to estimate the temperature just after the heating phase and during the cooling phase. Three successive values of obtained temperature enable to reconstruct the temperature reached at the end of the heating phase, as detailed in Fig. 9. Double-pulse phase consists in gate voltage and Gate current recording via an oscilloscope but also in on-state characterization with drain current and voltage measurements, described in Fig. 10. With the two latter characterizations, several parameters are recorded along the module lifespan: three couples  $I_{DS}/V_{GS}$  for temperature estimation, the gate voltage and current during turn-On, the On-state drain voltage and current. These parameters will allow calculating 50 potential ageing precursors.

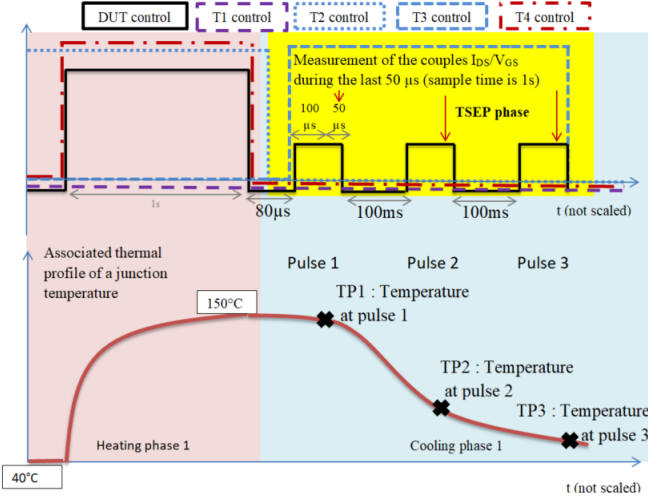


Figure 9: TSEP phase measurement and thermal profile

#### V. RESULTS AND ANALYSIS

##### A. Precursors calculation during module lifespan

Some potential precursors are extracted from the *TSEP phase* and are listed in Table II.

TABLE II: Ageing precursors extracted from the TSEP phase

Precursors	Description
TP(i)	Estimated temperature at pulse 1, 2 and 3
$I_{DS}V_{GS}(i)$	$I_{DS} \cdot V_{GS}$ at pulse 1, 2 and 3
$I_{DS}P(i)$	$I_{DS}$ at pulse 1, 2 and 3
$MI_{DS}$	Mean value of Drain current on the three pulses

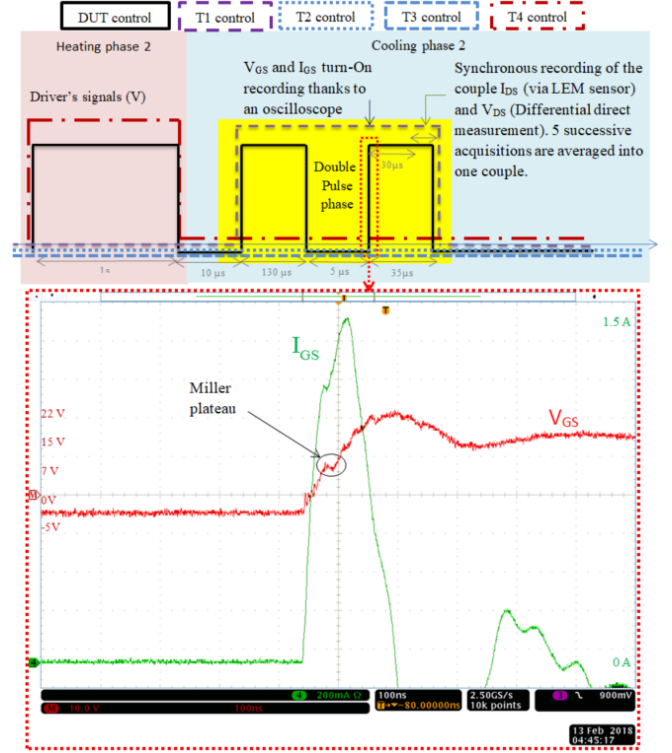


Figure 10: Waveforms during double-pulse measurement

The other precursors are extracted from the *double-pulse phase* and are listed in Table III. These parameters are automatically calculated along the module lifespan from a MATLAB@Mathworks script. The plots of parameters according to ageing are de-noised to obtain exploitable signals. In the next section, it will be shown how these parameters are correlated to ageing to keep the more relevant ones for condition monitoring and how we are able to determine the most informative carriers among them.

##### B. Failure mode signature

Different ageing profiles have led to two practical failure modes: conduction path degradation and a partial perforation of gate oxide. These failure mode occurrences have been described by several parameters' drifts. To detect failure indicators from these drifts, a parameter selection has been made in two steps. First, a Spearman correlation calculation allows detecting parameters linked to ageing [17] and second a Shannon entropy calculation allows determining which parameters are the more informative [22]. Method is illustrated in Fig. 11, gathering the post-mortem analysis to obtain information on failure mode, and the best indicators according to Spearman correlation and Shannon Entropy calculation. Once these indicators are recognised, a combination of them has been found to establish a relevant failure signature of failure mode occurrence.

Among the four common precursors found according to these two profiles, we have chosen the temperature, the On-state resistance and the On-state voltage to have a 3D representation with easy access information.

TABLE III Ageing precursors extracted from the double-pulse phase

Precursors	Description
$R_{DSON}$	On-state resistance
$P_{Miller}$	Instantaneous power during the second pulse
$V_{DSON}$	On-state voltage
$I_{DSON}$	Drain current during the second pulse
$E_{ON}$	Injected energy in the Gate
$E_{ONN}$	Injected energy in the Gate normalized by $I_{DSON}$
$E_{ONN^2}$	Injected energy in the Gate normalized by $I_{DSON}^2$
$I_{Gmax}$	Maximum Gate current
$V_{Gmax}$	Maximum Gate voltage
$AreaI_G$	Area under $I_G$ during turn-On
$fI_G$	Pseudo-frequency of $I_G$ during turn-On
$Rise_{Time(i)}$	Rise-time to reach voltage value "i" from 1 to 15 V
$AreaV_{GS}$	Area under $V_{GS}$ during turn-On
$Area_{plateau}$	Area under $V_{GS}$ plateau during turn-On
$Max_{plateau}$	Maximum point of $V_{GS}$ plateau
$Min_{plateau}$	Minimum point of $V_{GS}$ plateau
$Mean_{plateau}$	Mean level of $V_{GS}$ plateau
$Length_{plateau}$	Length of $V_{GS}$ plateau
$T_{meanPlateau}$	Mean time of $V_{GS}$ plateau
$Coef_{linear}$	Slope and intercept of the linear function fitting on the plateau
$Coef_{poly}$	Parameters of the 3 <sup>rd</sup> order function fitting on the plateau


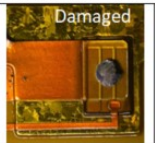
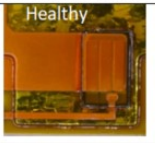
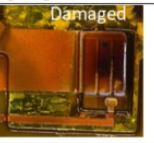
Ageing profile 1 leading to a Gate oxide perforation (Observed with a B1505 Analyzer)	Ageing profile 2 leading to a conduction path degradation (Observed with a B1505 Analyzer)
Views of the MOSFET area before and after ageing	
 	 
Relevant precursors determination with a Spearman correlation (coef 0.8) and Shannon Entropy calculation	
<p><b>Temperature Pulse 3</b></p> <p><math>R_{dsON}</math></p> <p><math>V_{dsON}</math></p> <p><math>P_{miller}</math></p> <p>Temps de montée à 8 V</p> <p>Niveau Plateau</p> <p>Pente Plateau</p> <p>Tmilieu Plateau</p>	<p><b>Temperature Pulse 3</b></p> <p><math>I_{dVg1}</math></p> <p><math>I_{dP1}</math></p> <p><math>R_{dsON}</math></p> <p><math>P_{miller}</math></p> <p><math>V_{dsON}</math></p>

Figure 11: Data analysis for two ageing profiles

To determine a signature evolution with ageing, we build a classification, which is able to determine 3 classes: 1) the module is healthy, 2) a failure mechanism is in progress but we don't know which one, 3) the module reaches the end of lifespan. Data classification begins with a normalization (by the initial value, because for a new module we miss the mean and standard deviation) of parameters evolutions. Indeed, each module has its initial performances and characteristics do not have the same values. Normalization in time is also realized to talk about life percentage and no more of number of cycles. A non-supervised classification is then realized on 5 modules constituting the learning group. The chosen method is the K-Means approach. This method consists here in dividing a group of point in 3 defined groups by calculated centroids of each class and keeping the shorter distance between one point and its centroid and keeping the higher distances between each centroid. Iterations are performed until the centroids do not evolve anymore. Fig. 12 shows the centroids localization for each of the 5 learning modules. A barycentre has then been calculated to be the centroid of the final classes.

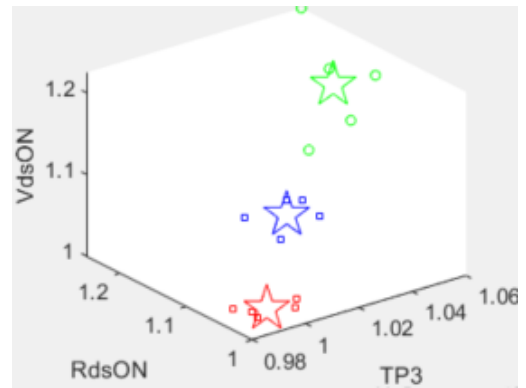


Figure 12: Centroids positions for a 3-class classification (squares for each module centroids, stars for learning group centroids)

An example of a classification has been built for one given module whose failure mode was the Gate oxide perforation. Class attributions seem to work well, as shown in Fig. 13(a). We can see that points of the signature belong successively to class 1, 2 and 3 without any step backwards. When we applied the classification to other modules, whatever the failure mode observed, we have the same succession of classes. However, depending on the module, classes haven't the same repartition in time (Fig. 13(b)). These differences come from the dispersion of initial characteristics of modules (lab-scale prototypes) and also to little variations of signature evolution according to failure modes (two different failure modes listed in Fig. 11). To correct this uncertainty and be able to evaluate a Remaining Useful Lifetime (RUL), we have to calculate emission rate from each class at each time interval. We have also to construct a transition rate between two classes knowing the class of previous signature points.

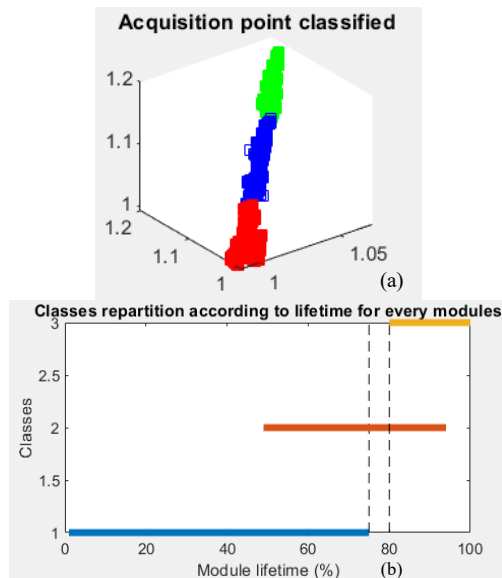


Figure 13: (a) signature classification for a module of profile 1 and (b) spreading of classes (Healthy, Failure mechanism in progress and End of life) for the 5 learning modules.

## VI. CONCLUSION

This study, fed by literature analysis, has allowed creating a specific test plan in order to trigger failure modes in a new power module technology and to identify failure signature with a short learning phase in order to use it later for on-line health monitoring in normal operating conditions.

## ACKNOWLEDGMENT

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