



# Powering AI at the edge: A robust, memristor-based binarized neural network with near-memory computing and miniaturized solar cell

Fadi Jebali, Atreya Majumdar, Clément Turck, Kamel-Eddine Harabi, Mathieu-Couumba Faye, Eloi Muhr, Jean-Pierre Walder, Oleksandr Bilousov, Amadéo Michaud, Elisa Vianello, et al.

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# Powering AI at the Edge: A Robust, Memristor-based Neural Network with Miniaturized Solar Cell



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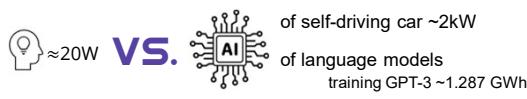
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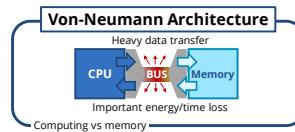


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## Deep Neural Networks

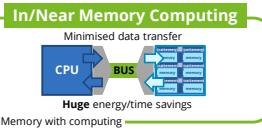


Neuromorphic applications are data intensive:  
Meet the Von-Neumann bottleneck



Operation	Energy
Sum (Fixed Point)	1x
Value Access (onchip cache)	60x
Value Access (offchip RAM)	3500x
Pedram, et al., IEEE D&T 2016	

Inference on edge device:  
Near Memory Computing for energy harvesting



## Our Approach for Inference on edge device

Binary Neural Network based on  $HfO_x$  RRAM (Memristor) Technology

⇒ Limit drastically the memory footprint (binary coding)

General case:  $a_j = f \left( \sum_{i=0}^n W_{ij} \times x_{ij} + b_j \right)$  where  $W_{ij}, x_{ij}, b_j \in \mathbb{R}$

Binary case:  $a_j = sign \left( POPCOUNT \left( XNOR(W_{ij}, x_{ij}) \right) - t_j \right)$  where  $W_{ij}, x_{ij} \in \{-1, 1\}$

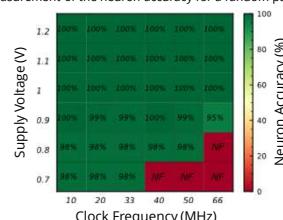
### Desing to a robust solution under low voltages

- Weights  $W_{ij}$  are stationary and programmed-only once
  - Each weight ( $W_{ij}$ ) is stored in a 2T2R bitcell using complementary states
- Augmented PCSA with XNOR operation is named XPCSA
- Mixed design with digital on top
  - 4x8k RRAM array (32k RRAM) & 10k standard cells
- AI digital controller is embedded
- Up to 128 neurons by 128 synapses
- Manufactured on 130nm + CEA-Leti RRAM
  - RRAM between M4 and M5
  - Area = 7.5 mm<sup>2</sup>

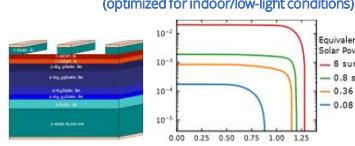
## Robustness Assessment

Functional under a wide range of frequency and voltage w/o any calibration.

Measurement of the neuron accuracy for a random pattern

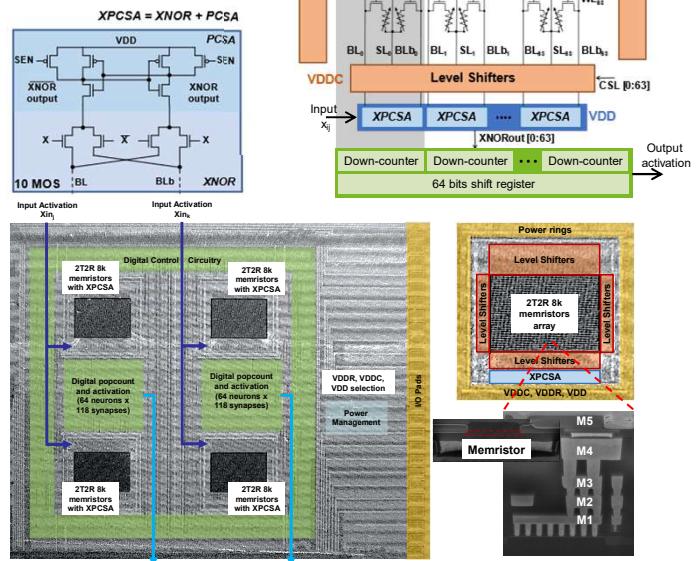


Direct Powering with miniature III-V solar cell (optimized for indoor/low-light conditions)



Under low illumination, little energy is available. AI does not fail, but gradually becomes less accurate.

	This work	Wan et al. Nature 2022	Xue et al. Nat. Electron. 2021	Jung et al. Nature 2022	Khaddam et al. IEEE IJSSC 2022
Device CMOS node	$HfO_x/Ti$ 130 nm	$HfO_x/TaOx$ 130 nm	Proprietary RRAM 22nm	MRAM 28nm	PCM 14nm
Unit cell	2T2R	1T1R	1T1R	2T2R	8T4R
Levels per cell	SLC	SLC	SLC	SLC	SLC
Weight bit width	1	1	1-4	1	1
Read circuit	XPCSA	Sense amplifier	Analog + ADC	Analog + TDC	Analog + ADC
Multi/Accu	Digital/Digital	Analog/Analog	Analog/Analog	Digital/Analog	Analog/Analog
Inference voltage need for calibration	Flexible (0.7-1.2V)	Predet. Yes	Predet. Yes	Predet. Yes	Predet. Yes
Reported energy efficiency (TOPS/W)	2.9 (measured) 22.5 (clock-gated) 397 (28nm-projection)	7 to 43	37 to 126	262 to 405	10.5



## Take away message

- AI at the edge needs near-memory (NMC) or in-memory (IMC) computing solutions
- Analog IMC needs calibration and supports a single operating point: incompatible with energy harvesting.
- Our digital NMC is far more stable on a large range of operating points and is compatible with energy harvesters. When little energy is available (e.g., 0.08 suns), it does not fail but gracefully adjusts its accuracy.

