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***Abstract*—This study focuses on the drain-source breakdown voltage (V_{BR}) of 100 V commercial p-GaN transistors. By presenting V_{BR} values, showcasing device dispersion, and employing failure analysis (FA), we explore various physical degradation mechanisms. Investigating the degradation process from origin to defect manifestation enhances our understanding of GaN transistor limitations. Additionally, the paper highlights the adaptation of FA methodology based on defect nature, providing valuable insights for semiconductor device reliability improvement.**

Keywords—voltage breakdown, reliability, failure mechanism, GaN power transistors.

I. Devices used and stress applied

The devices under test (DUT) are commercial, 100 V, 90 A, 7 mΩ packaged p-GaN gate AlGaN/GaN HEMT of part number 1 (devices δa to δi in Table I) and 100 V, 36 A 16 mΩ packaged p-GaN gate AlGaN/GaN HEMT from the same manufacturer and called part number 2 (devices ωa to ωd in Table II). The ε devices are from another manufacturer their ratings are unpackaged naked die with solder bumps of ratings 100 V, 16 A, 7 mΩ.

The drain-source voltage (V_{DS}) and the gate-source voltage (V_{GS}) are applied with a Keysight™ B1505A power device analyzer/curve tracer connected with probe needles landed on the package electrodes.

V_{DS} is sweeped up until the breakdown voltage value (V_{BR}) is reached which is the V_{DS} value when the drain leakage current I_{dss} increases abruptly (see Fig. 1).

TABLE I. TABLE OF BREAKDOWN VOLTAGE VALUES PART NUMBER 1: 100 V, 90 A, 7 MΩ

Part Num.1 **device n. :**	**Setup**	$V_{DS} = V_{BR}$	**Expected degradation**
δa	V_{GS} = 0 V	154.6 V	DS leakage FP
δb		123.8 V	DS leakage FP
δc		144.5 V	DS leakage FP
δd		165.9 V	DS leakage FP
δe		161.6 V	DS leakage epitaxy
δf		158 V	DS leakage epitaxy
δg		150.4 V	DS leakage epitaxy
δh		162.7 V	DS leakage epitaxy
δi		157.9 V	DS leakage epitaxy

II. Two types of degradations

The δ devices tested in drain source voltage have two different electrical breakdown signatures. One is a complete failure of the device, immediate and not recoverable, the device after the breakdown voltage measurement cannot be used in an application due to very high leakage current at low voltage bias. The other one is only degraded (not severely damaged) after V_{BR}, a second and even more other breakdown voltage measurement can be performed on the device. The leakage current of these device only change for high drain voltage (above 120 V).

A. Immediate degradation, complete failure

The δ devices that failed entirely at first attempt are the devices a to d. The V_{DS} limits in the same range of value ie between 123 V and 166 V as visible in table I. δa was less degraded thanks to the use of a serial resistance that limits the default current after V_{BR} (max of 500 µA) and δb,c and d were more degraded due to a higher current limit after breakdown voltage (8 mA) and the removal of the serial resistance.

The breakdown corresponds to an increase of the DS leakage current. For these four devices the V_{BR} measurement leads to a complete failure of the device in a single sweep. When the drain voltage sweep is done again (V_{BR} 2) on the same device the resistance of the device is severely reduced and therefore the current leakage is significantly increased as it can be seen on the dashed lines of Fig. 1. The backward sweep of the hysteresis of device δa shows a significant reduction of the resistance of the device too.

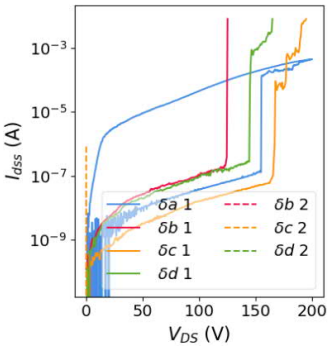

Fig. 1. Electrical signatures of the V_{BR} for devices δa,b,c and d. The drain current leakage increases abruptly at the V_{BR} reached at at 154.6 V, 123.8 V, 144.5 V and 165.9 V for the respective device. The dashed lines show the signature after V_{BR} 1. The blue curve of device a shows with the hysteresis a change of leakage current on the forward sweep (increase by two orders of magnitude). The increase in drain leakage current is expected to be a drain source leakage current.

B. Degradation occurring at higher drain voltage

The other devices of the same part number in the same stress conditions (current limit at 8 mA, no serial resistor), δe to δi did not lead to complete failure after performing a first V_{BR} measurement.

As it can be observed for transistor δe in Fig. 2a,b the curves of V_{BR} 2-4 overlap with the curve of V_{BR} 1 under V_{DS}=120 V. Nevertheless a degradation has appeared after

V_{BR} 1 as the increased of leakage current can be seen at a smaller voltage in the next V_{BR} measurements. A leakage path has then been formed after V_{BR} 1, the resistance of the leakage changes in the subsequent V_{BR} measurements (particularly between V_{BR} 2 and V_{BR} 3 respectively in pink and orange in Fig. 2a above 140 V) due to the addition of other leakage path in the device that will be showed later.

The devices δf-i (Fig. 2c) showed the same degradation behavior that δe. The gate current during V_{BR} did not change at all, the gate stack nor the gate region seem affected in this case, a degradation is expected to be located in the drain region of the device. The device characteristics is still in the ratings, still operate correctly and could be used in a power application according to the manufacturer datasheet despite a change of V_{BR} curve showing a degradation of the device.

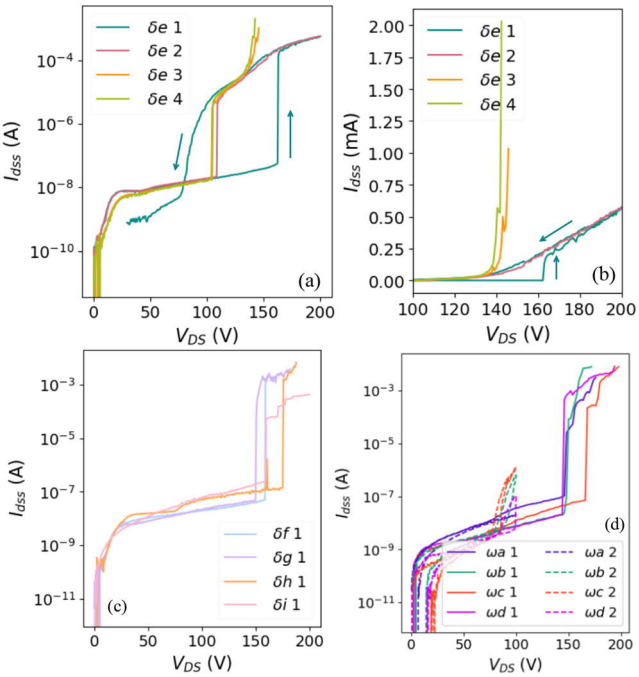

Fig. 2. Electrical signature of the repeated V_{BR} (1,2,3 and 4) for devices δe, other V_{BR} measurements were performed after the first one to study the propagation and evolution of the V_{BR} defect. No degradation was noticed after the first attempt like the devices on Fig. 1 (a) log display, (b) linear display, (c) Electrical signature of the first V_{BR} of the devices δf to δi, (d) Electrical signatures of the ω devices.

The other part number devices (ωa to ωd) did not fail entirely as well after V_{BR} 1 like δf-i, the V_{BR} is in the same range than δ devices (δe to δi), see Table II. However, a steep increase of leakage current occurred at a smaller V_{DS} voltage (see Fig. 2d: 90 V for V_{BR} 2 instead of 150 V for V_{BR} 1). None of the device of this part number showed degradation mechanisms presented in section A with V_{GS} = 0 V (gate-drain leakage current).

TABLE II. TABLE OF BREAKDOWN VOLTAGE VALUES FOR PART NUMBER 2: 100 V, 36 A, 16 MΩ

Part Num.2 **device n. :**	**Setup**	$V_{DS} = V_{BR}$	**Expected degradation**
ωa	V_{GS} = 0 V	146.2 V	DS leakage epitaxy
ωb		146.9 V	DS leakage epitaxy
ωc		165.1 V	DS leakage epitaxy
ωd		141.8 V	DS leakage epitaxy

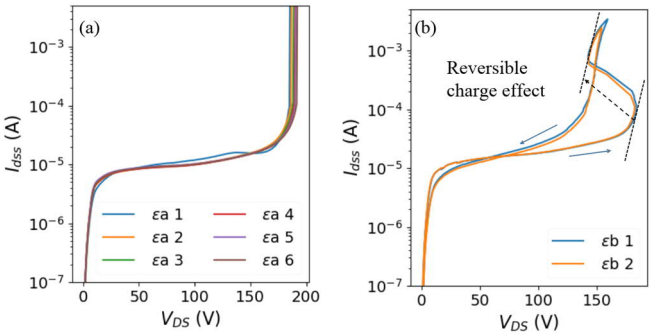

Fig. 3. (a) Electrical signatures of the drain leakage current at high polarization when looking for the V_{BR} of ε devices. No change can be observed after the repetition of the high polarization. The power is limited by the tracer SMU to reach a flagrant degradation. (b) Example of charge leak out at high polarization that generate a shift of the leakage increase knee. The phenomenon does not seem to be related to a degradation as it is reversible.

The other manufacturer's devices (devices ε, 6 devices tested in total) did not fail as the devices of section IIA, the leakage increase knee is stable and does not seem to be affected with the reproduction of the V_{BR} measurement stress (Fig. 3a).

However, some instabilities of the operating point were observed in the increased leakage current part near 180 V as visible in Fig. 3b. As the current increased, some reversible voltage reduction was observed, indicating an avalanche-like phenomenon that is expected to be related to the charge trapping/detrapping effect.

The leakage current is expected to be related to dislocations and as explained in [3], the additional leakage current resulting from trapping/detrapping effects may come from ionized carbon acceptors in nitrogen sites which may favor Poole-Frenkel emission process. The emission process can lead to the discharge of stored charges in the buffer, which add up to the leakage current that goes through dislocation defects.

The energy of the B1505A's Source Measurement Units (SMUs) is not sufficient to produce visible degradation on the device, as compliance is reached very quickly once the leakage rise knee is reached. A higher power current controlled SMU was used to reach the true breakdown voltage. This experiment is performed while measuring the photons emitted with Photon Emission Microscopy (PEM).

The operating point to reach the drain voltage limit of the device is controlled by the current value, which is increased step by step. A first emission spot appears in zone 1 in Fig. 4, which means that the leakage current at high voltage observed in Fig. 3 is more intense locally in the structure.

After increasing the current and then the power in the structure, this spot disappears and another one appears in the lower right corner of the device (zone 2 in Fig. 4b). A defect is now visible in zone 1 near the bump and the whole structure can still be polarized with high voltage (195 V).

The increase in leakage current controlled by the SMU resulted in a complete failure near 20 mA. After this step, high polarization is no longer possible as a few volts resulted in a very high leakage current, indicating the formation of an electrical short within the structure.

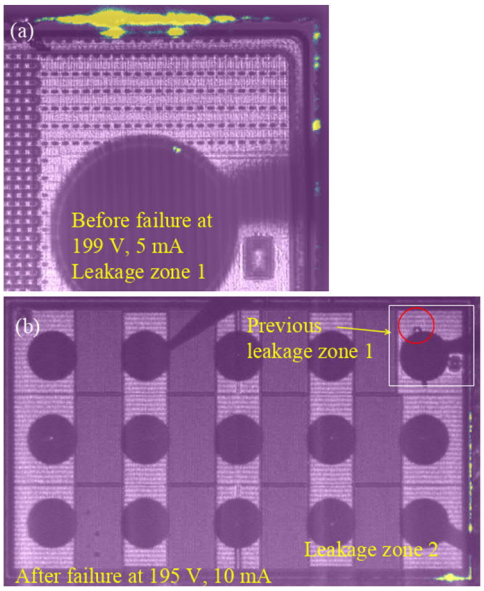

Fig. 4. PEM in frontside during the V_{BR} measurement of ε devices. A first emission spot is visible in zone 1 a the top right corner of the device and a second one appeared at the bottom right corner of the device with the increase of the leakage current after the first one disappeared.

Devices (both δ and ω) stressed with V_{GS}=-3 V have the degradation mechanism of section A which is a gate drain leakage current in the gate area. These stress conditions are interesting to study as this gate voltage is advised in application by the manufacturer at off-state.

III. Nature of Defects

A. *Electrical short in the passivation region*

For the device δa, a backside approach was performed as described in [1]. A focused ion beam (FIB) cross-section (Fig. 5) revealed a metallic shunt that electrically short the drain (the 2DEG) and the source (field plate metal). The melting of the field plate metal is induced by the high electric field, which generates a metal filament.

Fig. 6 shows the consequence of an up to V_{BR} sweep for a device were the limiting serial resistance is removed (δd), which is the situation that will be encountered in a real application. The FP melted on a much larger area due to the higher energy. The consequence is that all electrodes are then shorted together.

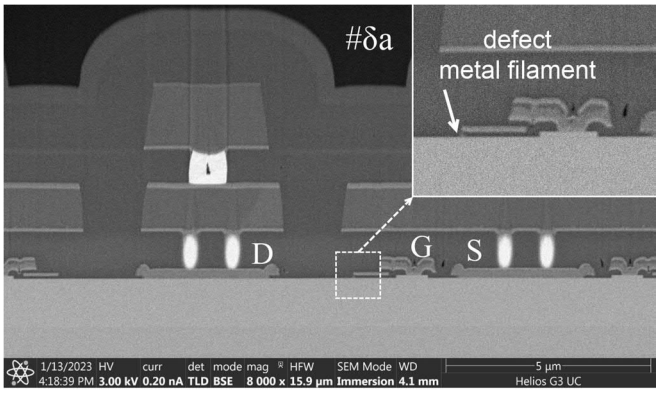

Fig 5. FIB cross-section in the defect region of device δa (breakdown energy limited with the serial resistor). The drain source electrical short seems to originate from the melting of the metal field plate that reached the drain electrode through the 2DEG.

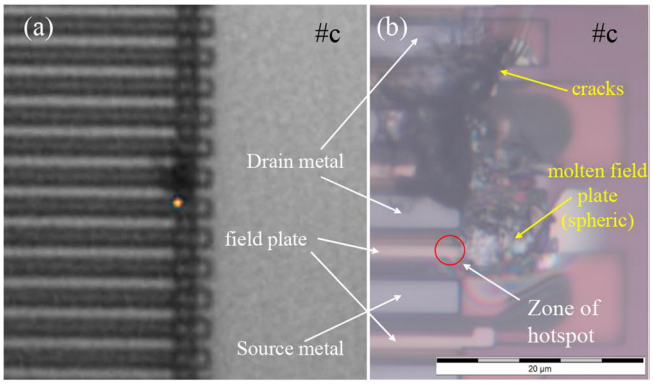

Fig. 6. (a) IR LIT Localization of defect of device δd (no serial resistance during V_{BR}). A hotspot is visible on the field plate metal area near the drain. A black spot start from this point and expand above it which shows the propagation of the defect. (b) Zoom of the defect zone. The metal structure is visible from the backside through the GaN layers. The short led to the melting of the field plate metal.

B. *Failure expected to be caused by dislocations issues*

δ device: leakage through dislocations

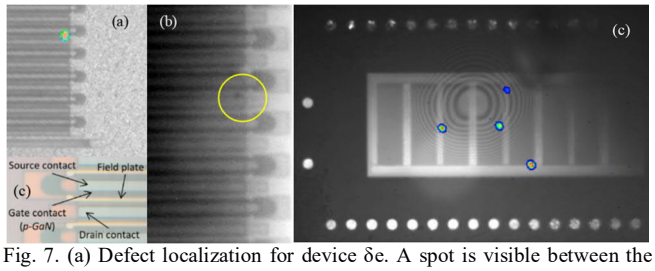

Fig. 7. (a) Defect localization for device δe. A spot is visible between the field plate metal and the drain metallization. (b) IR 71x zoom camera of the defect zone. A black spot is visible on the drain metallization (above the drain contact, probably in the GaN layer as it is a backside observation). (c) Defect localization with 10x magnification of device δe, four emission spots are visible on the edges of the active zones.

The devices that did not break after V_{BR} 1 (δe to δi ; ωa to ωd and ε devices) are suspected to have experienced vertical leakage current degradation through the GaN layer near the drain metal. The failure in the epitaxy compared to the previous case in SiN is attributed to differences in the random layer process quality that selects the stress weak spots within the structure (either SiN or GaN).

Photon emission microscopy (PEM) localization was used to identify the areas of leakage current. The number of observed spots appears to increase with the number of V_{BR} sweeps carried out on a device, particularly with the number of shape changes in the leakage current. A significant change in resistance between two V_{BR} at a certain V_{DS}, such as at 140 V in Fig. 2b, is expected to generate a new leakage path and spot within the device (Fig. 7d). Devices that underwent only one V_{BR} sweep have only one spot.

The first defect produced by V_{BR} 1 does not seem to evolve at V_{BR} 2 or the subsequent ones. Indeed, this defect's is a leakage current and it is still possible to increase the electric field throughout the device and lead to new defects elsewhere in the transistor. This explains Fig. 7c and the four emission spots instead of only one spot that is getting bigger after performing again V_{BR} sweep.

A dark spot is visible with IR microscopy at each emission spot location (see Fig. 7b for δe). A big defect could be expected as the defect is visible at this step, however this spot

is not visible with other microscopes that have a different focal length.

The defect is within the GaN layers and does not seem to affect the metals of the active zone, as observed by changing the focus distance. The defect's electrical signature, previously observed under different stress conditions [1], suggests that the leakage path may be caused by dislocations generated by a sufficient electric field [4].

The observed leakage current is likely due to a Time-Dependent Dielectric Breakdown mechanism [2,3]. The dark spots observed (on IR microscopy images) indicate a visible evolution of the transistor. There may be a change in crystalline properties due to an increase in the concentration of another element such as aluminum for instance near the leakage path.

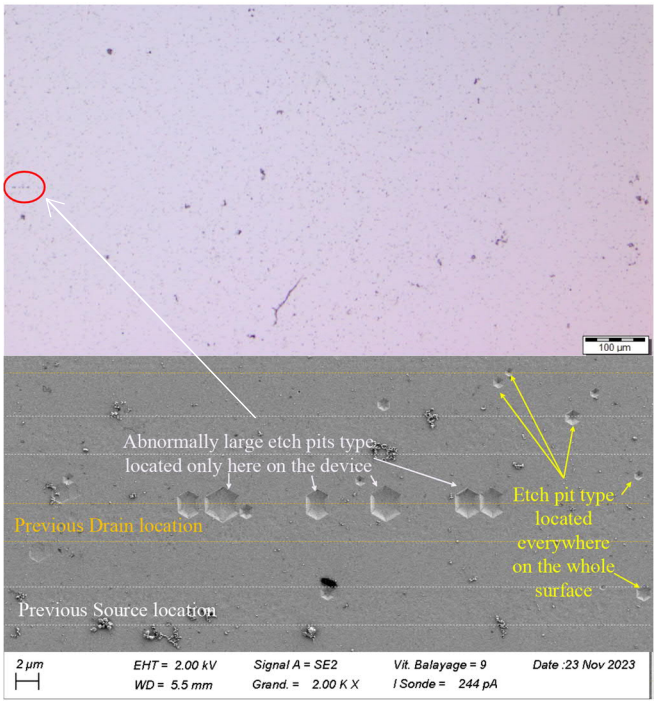

Fig. 8. (a) Optical view of the surface of the transistor after chemical etching with ortho phosphoric acid (H_3PO_4), the small black dots on the whole surface are etch pits of revealed dislocations. On the left of the picture the bigger etch pits aligned of (b) are visible. (b) SEM observation of the GaN layer in frontside circle in red in Fig. 7a. Etch pits of some the dislocations are visible on all the surface (yellow arrows), however on one border of the active zone, the pits are larger and aligned on the edge of the previous drain metal location (white arrows).

In our previous study in [1] we did obtain a similar electrical signature of degradation for a switching voltage stress. We found in this paper that the density of dislocations seemed to increase due to the stress with the observation of TEM lamellae and conductive Atomic Force Microscopy (AFM) experiments. However this paper was inconclusive as many dislocation are already present before stress and differentiate them with stress produced one is complicated.

This paper investigates a less expensive and time-consuming approach to observe defects in the metal location. The device was studied by removing the varnish and the first layer of copper with nitric acid from the front side. The process began with a dip in hydrofluoric acid etching (dip HF) to remove the metal and oxide layers, leaving only the silicon substrate, the GaN buffer, the AlGaN barrier, and the p-GaN cap.

Next, the sample was revealed with heated H_3PO_4 at 130 °C for 10-20 minutes to remove the p-GaN and AlGaN layers. The surface of the GaN buffer revealed some of the dislocations through etch pits that were uniformly observed.

However, a different pattern is observed on the stressed device (device δd that was stressed under the same conditions as δe). The etch pits are aligned on the border of a drain metal edge localization on the border of the active area of the device where the emission spots are often observed (see Fig. 7c). The pits are larger than the others (2 to 3 µm versus 1 µm), as shown in the SEM image in Fig. 8).

The line of different etch pits was observed only on stressed devices and not on pristine ones. The chemical conditions are difficult to maintain as the chemical revelation is a very unstable and variable process. Only a third of the stressed devices tested show this pattern and none of the pristine ones. $V_{GS} = 0$ V

The larger aligned pits may correspond to conductive dislocations. The larger size of dislocations may be attributed to the presence of aluminum impurities brought by Cottrell clouds, which accelerate the etching process locally [6]. The presence of aluminum impurities can reduce the electrical isolation of the buffer layer. Furthermore, deeper dislocations may cause more significant etching [7], resulting in a thinner electric isolation layer and increased leakage current at high voltage drain values.

εa device: high energy defect

The other manufacturer's devices (ε devices) do not lead to the defect presented in Sections IIA and IIIA thanks to a different design choice. In fact, the drain-source electrical isolation is mainly done in two regions inside the structure, under the field plate edge on the drain side and the GaN buffer layer. The electrical isolation varies with the thickness of the materials used, the doping, the type and the doping concentration of the device.

While the voltage boundaries of these two regions are quite close for δ devices, resulting in two distinct failure modes, the addition of a second field plate (FP2 in Fig. 9) further from the channel results in a unique failure mode for ε devices. This failure is in the GaN layer below the drain metal.

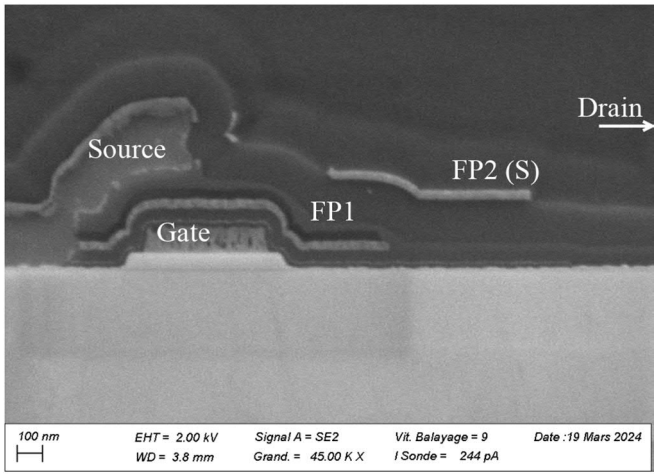

Fig. 9. SEM image of the cross section of the gate region of ε devices. The second field FP2 improve the electrical isolation drain source between the field plate FP1 and the channel region.

The current leakage through the GaN layer is expected to be related to dislocations in the structure, as explained for the

δ devices of B. The appearance of the second emission spot in fig.4 could be the generation of a new leakage path and perhaps new dislocations, as in the case of the δ devices.

The increase of the current in the vertical path originating from dislocations in GaN (new here before stress) can generate an evolution of the defect and could give an idea of the aging of these crystal defects in an application.

The disappearance of the emission spot of Fig. 4b is expected to be the generation of a metallic short in the GaN layer near the current path and caused by the increase in temperature and current coupled to the electromigration phenomenon. The presence of the metal could affect the charge recombination process that makes the spot in PEM. The high current leakage and temperature could cause a local melting of the drain metal as can go through the GaN layer.

The high polarization is possible if this filament does hold the thermal and electric field stress.

Increasing the leakage current caused melting of the drain metal and the filament to propagate through the GaN buffer and reach the AlGaN connected to the source potential. The melting caused by the high energy then propagates to the upper metal level of the structure. An optical front-side view is shown in Fig. 10. Many cracks are visible on the structure metal in the defect in zone 1.

The defect visible with the IR camera in Fig. 6 is expected to be an optical effect caused by the change of the polyimide after being at high temperature.

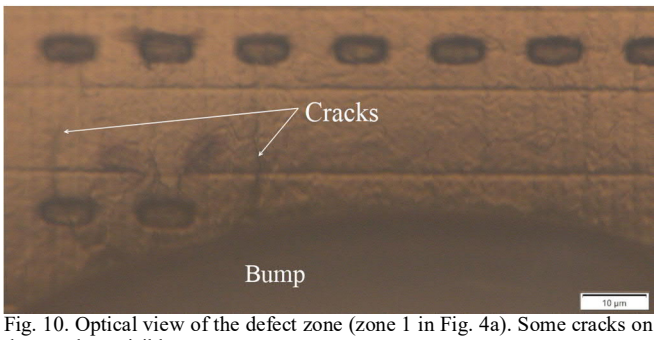

Fig. 10. Optical view of the defect zone (zone 1 in Fig. 4a). Some cracks on the metal are visible.

A FIB cross section in Fig. 11 was performed in the defect zone of this device to verify the failure hypothesis of the GaN layer. The image in Fig. 11 is the FIB Slice&View image when the defect is most significant.

The drain metal has disappeared with the melt propagating to the metal above. However, it can be seen that the void caused by the melting is just below the drain metal and is contained in the GaN layer. The boundary of the void is the AlGaN layer of the buffer superlattice, which is electrically connected to the source.

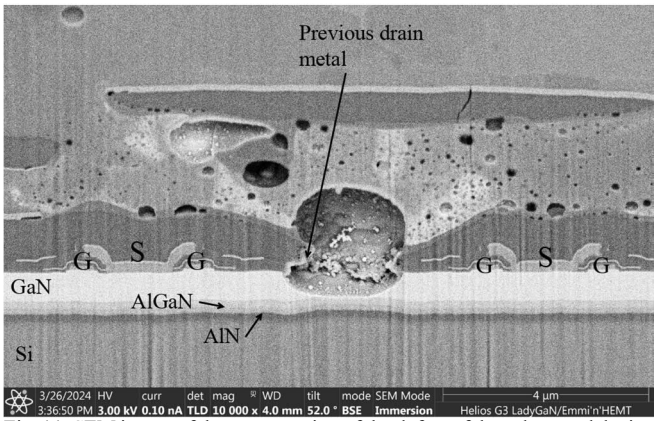

Fig. 11. SEM image of the cross-section of the defect of the ε damaged device a void is expected to be the consequence of the melting of a metal filament under the drain metal where the electrical leakage path was. The image shows that the leakage observed at high V_{DS} polarization is vertical and in the GaN layer, the defect stops at the AlGaN layer connected to the source.

The SEM image of Fig. 11 shows the evolution of the leakage path through the GaN layer and related to crystal defects. The study of both the δ devices of IIIB and the εa device allows to show the origin of the defect and its evolution to a complete failure.

The local high leakage current can come from existing conductive dislocations induced by the manufacturing or the hypothetical dislocations generated by the electric field and the displacement of metal elements in the vicinity of the dislocations, which locally reduce the electrical insulation and create the leakage path in the GaN buffer.

Once the electrical path is in the structure, the high energy can cause it to evolve into a metal percolation with melting of the drain metal above the leakage path. Once this second step has occurred, the device has reached total failure and the drain and source electrodes are electrically shorted. The drain metal melt propagates with the drain via to the upper level of metal connected to the drain and then to the level of metal above conneced to the source and creates a drain source electrical short as visible in Fig. 12.

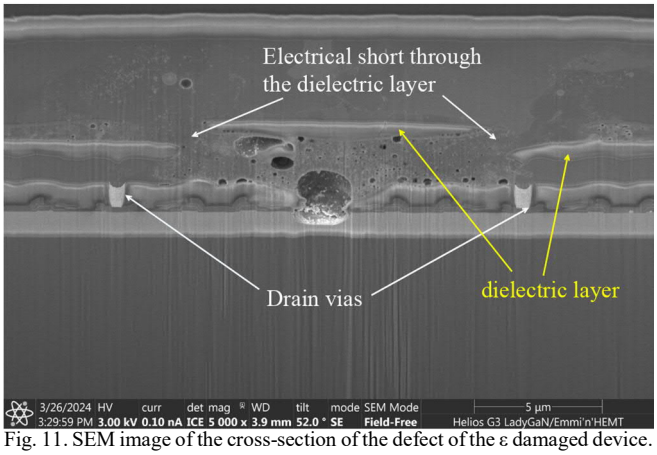

Fig. 11. SEM image of the cross-section of the defect of the ε damaged device. The propagation of the melting of the drain metal to the drain via and then to the upper levels of metal shows the electrical short that traduces the complete failure of the device.

CONCLUSION

The experiment on breakdown voltage revealed two types of defects depending on the location of the weakest spot within the device regarding the choices of design. The first type is located under the field plate metal. The failure analysis is relatively simple, and metallic shunts are expected. The second type is a defect in the GaN buffer layer that appears to be related to dislocations. The failure analysis at this step is much more complicated because the device is degraded but not severely, and the defect is difficult to observe. Some experiments, such as chemical revelation, can provide additional information to understand this second failure mechanism. The increase of the energy in this type of cristalline defects can produce a complete failure of the device. The crystalline defect becomes a metallic defect in the GaN layer due to the melting of the drain metal.

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