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Toward thin GaSb Buffer Layers Grown on On-Axis (001) Silicon by Molecular Beam Epitaxy

A. Gilbert,* M. Ramonda, G. Patriarche, E. Tournié, and J.-B. Rodriguez

The monolithic integration of III-Vs on Silicon (Si) is of great interest for the development of active photonic integrated circuits (PICs). The main challenge is to achieve a high-quality epitaxy of the III-V on the Si substrate, as the differences between the materials are responsible for the formation of crystal defects, in particular threading dislocations (TDs) and antiphase domains (APDs) delineated by antiphase boundaries (APBs), which degrade the device's performance. A new technique is demonstrated to achieve thin APBs-free GaSb buffer layers grown on Si substrates. The original idea presented in this paper is to introduce a GaAs layer into the buffer to promote faster burial of APDs. Two strategies are compared; the first one involves the complete APDs burying in GaAs before growing GaSb, while the second one uses a thin GaAs layer before burying the APDs in the GaSb layer. APB-free buffer layers as thin as 215/400 nm have been obtained using the first method, which represents a factor of 2/4 thickness reduction compared to the previous results for both 0.5° and 0.2° miscut angles.

1. Introduction

Since the 1940s, miniaturization has played a crucial role in microelectronics, driving performance improvements and enabling

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(IC). Silicon (Si) is the material of choice for this technology thanks to its numerous benefits such as low cost, abundance, transparency windows, and high-quality oxide.^[1] However, further reducing the device dimensions faces major technical limitations such as manufacturing physical difficulties, heat dissipation, power consumption, and technology costs.^[2] As a consequence, Si-based photonic integrated circuits (PICs) emerge as a promising solution to address this bottleneck by integrating III-V optoelectronic devices with Silicon.^[3] Nevertheless, the development of the III-V laser source directly on the substrate is a challenge.

the development of integrated circuits

Several bonding techniques have been developed to combine Si and III-V compounds including wafer bonding,

flip-chip, and more recently micro-transfer printing.^[4-7] In parallel, monolithic integration or direct epitaxy is a compelling alternative, potentially offering low-cost and large-scale integration.^[8,9] However, crystal defects generated during the growth^[10] compromise the device's performance and reliability.^[11-13] The high density of treading dislocations (TDs) and antiphase boundaries (APBs) are the main technological issues faced when growing III-V devices on Si-photonic platforms. Antiphase domains (APDs) have long been the most problematic defect because they form electrically charged paths within the active layers, creating shortcuts that kill the devices.^[14,15] The heteroepitaxy of the III-V Zinc-Blende polar structure on the nonpolar Diamond structure of the Si substrate^[10] generally leads to the simultaneous growth of two III-V phases. Low-miscut Si(001) substrates present monoatomic steps, and two dimer orientations can be found on the surface, which is responsible for forming the two III-V phases or domains. Both III-V phases have the same crystal structure but are rotated by 90° around the vertical axis. Because of the partial wetting of the III-Vs on Si, the growth always proceeds through the 3D Volmer-Weber mode,^[16] and the III-V initial island's equilibrium shapes and sizes can be determined with the Wulff-Kaishew construction.^[17] When two islands of different phases coalesce, III-III and V-V bonds are formed at the interface, resulting in an antiphase boundary (APB). A solution proposed by H. Kroemer^[10] to avoid emerging APBs was to use highly misoriented group-IV substrates (>4°), to promote bi-atomic steps at the surface. In this case, only one Si dimer orientation populates the surface, which then translates in a single III-V phase.^[18] However, group-IV substrates with miscut larger than 0.5° are incompatible with the well-established manufacturing processes of the microelectronics industry.^[19] Recently, a new model for forming and burying APDs on low-miscut (001) Si substrates was proposed by Cornet et al.^[20] The initial domain distribution can be inferred from the comparison between the stable III-V islands' size, and the Si terraces' width. When III-V islands are smaller than the Si terraces' width, the local Si dimer orientation imposes the same phase for the numerous III-V islands nucleating on the same terrace, the initial phase distribution is therefore "terrace-driven". This situation occurs, for example, during the low-temperature growth of GaAs on slightly misoriented (<1°) Si substrates.^[21–23] The domains are then organized in a periodic pattern of parallel stripes, whose periodicity corresponds to the terrace width.^[23] Conversely, if the stable islands are larger than the terrace width, monophase islands grow over several Si terraces before they can coalesce. In this case, the domains' distribution is "nucleationdriven", and no longer reproduces the Si terraces' topology. This situation occurs during the growth of GaSb on slightly misoriented (<1°) Si substrates.^[24] The well-organized III-V stepped surface then promotes a predominant density of one type of step (III or V) in each of the two phases, and the group-III adatom diffusion length/incorporation is anisotropic in the two main [110] and [110] III-V crystallographic directions.^[19] In the case of the low-temperature growth used in the "terrace-driven" regime observed for the growth of GaAs, the anisotropy is no longer related to some III-V steps composition (which requires a step-flow growth mode and thus a high growth-temperature) but is instead related to the faster growth of the islands in one of the main in-plane crystallographic directions, resulting in the typical elongated geometry of the III-V islands. In both cases, this anisotropy favors the faster growth of one of the phases, the main phase domain (MPD), which progressively buries the APD.^[20] The miscut direction plays a crucial role in this model as it is the mean by which the higher degree of symmetry of the Si crystal with respect to the III-V crystal is reduced at the surface. This mechanism was experimentally confirmed with both GaSb and GaAs epitaxially grown on low miscut Si substrates. In the nucleation-driven case of GaSb, the minimum thickness required to bury APDs was found to be 500 nm on Si 0.5°, and 1.5 µm on Si 0.2° substrates.^[24] Conversely, in the terrace-driven case of GaAs grown on Si 0.5°, most APDs were covered by the MPD within only \approx 110 nm due to their initial small sizes and spatial organization after the coalescence of the 3D islands.^[23]

In the perspective of Sb-based optoelectronic devices on Si for mid-IR applications, it is crucial to grow an as-thin-as-possible buffer layer to avoid the thermal cracks originating from the thermal expansion coefficient mismatch between the III-V and the Si. In addition, dislocations arising from the relaxation of the lattice mismatch between the III-V and the Si cannot be avoided.^[25–33] Although various techniques for dislocation density reduction have been proposed in the literature,^[34–38] they increase the buffer thickness up to several micrometers, and the overall structure typically exceeds 8 μ m.^[39–41] Hence, it is necessary to suppress APBs as fast as possible in the thinnest buffer. The original idea investigated in the present work is to obtain a thin GaSb buffer by leveraging the rapid burying of APDs in the GaAs terrace-driven regime. We present a first strategy, where the complete APDs burial is achieved in GaAs, before the growth of the GaSb buffer. Next, we explore the possibility of combining the "terrace-driven" initial phase distribution in GaAs and the rapid APDs burying using the step-flow growth mode of the GaSb layer. This study represents a significant step forward, as a reduced thickness for APBs burying facilitates the early implementation of dislocation reduction strategies. Thin buffer layers allowing to simultaneously suppress APBs and cracks hold immense interest in developing compact and high-quality lasers on Si.

2. Experimental Section

All the samples were grown by solid-source molecular beam epitaxy in a RIBER COMPACT 21 system equipped with valved cracker cells for Arsenic and Antimony. Small offcut angles (0.5° and 0.2° toward a [110] direction) Si substrates were used for this study, and the surface was thermally prepared in situ (above 1 000 °C), in a dedicated chamber, to remove the native oxide. The samples studied in this article consisted of either GaSb/Si layers or GaSb/GaAs/Si composite buffers. In the latter case, GaAs layers were grown at 350 °C (thermocouple reading), followed by the deposition of 10 nm of GaSb at the same temperature. Finally, the growth temperature was increased to 450 °C, with the surface left under Sb flux to grow the rest of the GaSb buffer layers. A Ga growth rate of 0.6 MLs⁻¹ and a V/III growth rate ratio of ≈ 2 was maintained for all samples. Table 1 below summarizes the growth conditions for the GaSb/Si and composite GaSb/GaAs/Si heteroepitaxial growth.

Atomic force microscopy (AFM) was used in tapping mode to observe the samples' surface morphology. A Brucker AFM dimension 3100 was used to probe the surface and each layer was mapped at room temperature for different image sizes $(1 \times 1 \ \mu m^2, 2 \times 2 \ \mu m^2, 5 \times 5 \ \mu m^2)$ with nanosensors probes. Small-scale images are provided to visualize the small APDs-MPDs stripes patterns, while $5 \times 5 \ \mu m^2$ images were given when APDs are buried in composite GaSb/GaAs buffer to give a broader view of the surface and demonstrate the homogeneity of the samples. The AFM data were analyzed with the Gwyddion software.^[23] Finally, scanning transmission electron microscopy (S-TEM) was used to study the APDs. TEM lamellas were prepared from the samples using focused ion beam (FIB) ion milling and thinning. The samples were coated with carbon to protect the surface and thinning was carried out in an FEI SCIOS dualbeam FIB-SEM. The lamellas were prepared along the <110> zone axis parallel to the misorientation direction. The samples were observed in an aberration-corrected FEI TITAN 200 TEM-STEM operating at 200 keV.

3. Results and Discussion

3.1. Initial GaAs phase ditribution on Si 0.5° and 0.2° urface

The growth of GaAs in a terrace-driven configuration on a Si substrate with a 0.5° miscut results in the formation of regular 15 nm wide stripes populated with an alternation of APDs and MPDs, as previously shown.^[23] The stripes geometry is directly correlated to the Si terrace width when the surface is prepared in such a way that only regular mono-atomic steps are present. For this www.advancedsciencenews.com

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Table 1. Summary of the growth conditions for GaSb/Si and GaSb/GaAs/Si samples presented in sections III.2 and III.3, with GT_{GaAs} and GT_{GaSb} , the growth temperature of the GaAs and GaSb layers and RMS root mean square roughness. The remaining APDs percentage refers to the percentage of the sample area covered by the APD, extracted from the AFM images with the Gwyddion software.

| Sample | Si 0.5° | | | Si 0.2° | | | |
|-------------------------|-------------------|--------------------------------------|-------------------------------------|-------------------|--------------------------------------|---------------------------------------|--------------------------------------|
| | Nucleation-driven | Terrace-driven | | Nucleation-driven | Terrace-driven | | |
| | | 100 nm GaSb /115 nm GaAs (215 nm) | 450 nm GaSb /50 nm GaAs (500 nm) | 1.5 μm GaSb | 150 nm GaSb /250 nm GaAs (400 nm) | 100 nm GaSb / 100 nm GaAs (200 nm) | 200 nm GaSb /200 nm GaAs (400 nm) |
| GT _{GaAs} (°C) | / | 350 | 350 | / | 350 | 350 | 350 |
| GT _{GaSb} (°C) | 550 | 450 | 450 | 550 | 450 | 450 | 450 |
| APDs (%) | 0 | 0 | 0 | 0 | 0 | 30 | 4 |
| RMS (nm) | 1.14 | 1 | 1 | 0.86 | 0.85 | 1.05 | 0.92 |

reason, larger APDs/MPDs stripes of 41 nm are observed for thin GaAs layers grown on Si 0.2° substrates as shown in **Figure 1a**. This AFM image was taken on a 2-inch sample and shows that the GaAs surface perfectly reproduces the S_a and S_b step morphology of the Si 0.2°,^[18] with alternating straight and indented edges. Similar images were acquired for the whole surface of this 2-inch sample, providing evidence of the high level of homogeneity and efficiency of our pre-growth treatment. The depth difference between the MPD and APD stripes (indicated by the green arrow in Figure 1b) confirms that the two phases grow at different rates.

In this situation, the geometry of the domains is controlled to a very high degree, and the relatively small width of the stripes allows for the rapid burying of the APBs for a GaAs thickness close to 110 nm for a Si miscut of $0.5^{\circ[23]}$ and 200–300 nm for a 0.2° miscut, as shown in **Figure 2**. The thin stripes in Figure 2a are the remaining APDs observed at the surface of a 200 nm-thick layer grown on Si 0.2° , and it is clear from Figure 2b that almost all of these APDs are buried when the nominal GaAs thickness reaches 300 nm. Figure 2c shows the surface morphology for a 400 nm GaAs thickness completely free of APB for comparison. Based on these observations, and to ensure the burying of the

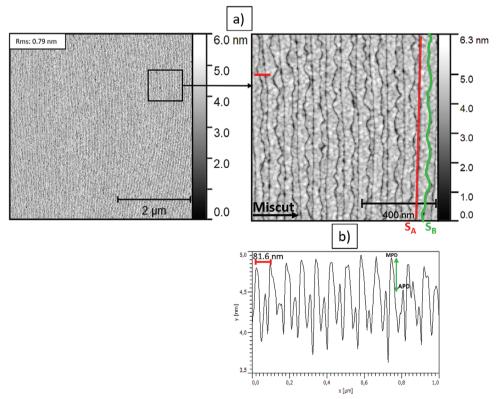


Figure 1. a) 5 μ m × 5 μ m and 1 μ m × 1 μ m AFM images of a 50 nm GaAs layer grown on a 2-inch 0.2° Si substrate showing a regular pattern of APD/MPD stripes and antiphase boundaries reproducing the alternating Si step edges. b) AFM-based average height (y) of the stripes at the sample's surface calculated and plotted with the Gwyddion software. The resulting curve shows periodic oscillations of 81.6 nm corresponding to the expected width of two Si terraces for a miscut of 0.2° (41 nm terrace⁻¹).

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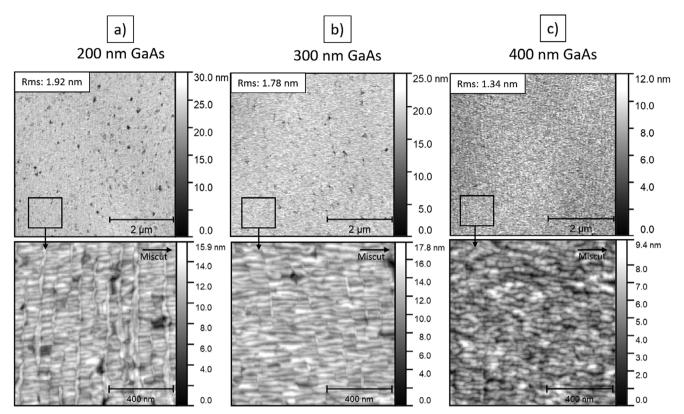


Figure 2. 5 μ m × 5 μ m and 1 μ m × 1 μ m AFM images of GaAs layers grown on a 0.2° miscut Si substrate, with varying thicknesses of a) 200 nm showing thin remaining APDs stripes and elongated MPDs islands parallel to the miscut, b) 300 nm, for which very few APD stripes are visible, and c) 400 nm showing only MPD.

vast majority of the APDs, we chose GaAs thicknesses of 115 and 250 nm on 0.5 and 0.2° substrates, respectively, for the following experiments.

3.2. Composite buffer: complete antiphase domains burying in GaAs terrace-driven initial phase distribution on Si 0.5 and 0.2° and transition to GaSb 2D growth mode

A sample consisting of a 115 nm-thick layer of GaAs grown at 350 °C thermocouple on Si 0.5° followed by 100 nm of GaSb grown at 450 °C was prepared. The GaSb thickness was determined from another set of samples, not described here, aimed at experimentally determining the lowest thickness to smooth the surface down to a root mean square (RMS) roughness of \approx 1 nm. The 5 µm \times 5 µm AFM image of the sample (Figure 3a) shows an APB-free surface with a low root mean square (RMS) roughness of 1 nm and well-defined atomic steps, confirming the step-flow growth mode of the GaSb layer. Compared to our previous result, obtained in a nucleation-driven initial phase distribution (Figure 3b) where the APD burying was achieved after 500 nm, this represents a reduction of the buffer layer thickness by a factor of \approx 2.5. A scanning transmission electron microscopy (STEM) analysis was performed to study the microstructure of the GaSb/GaAs interface. Figure 3a depicts a cross-sectional STEM bright-field (BF) image taken in the direction parallel to the miscut. The APBs appear darker and are confined within GaAs as they do not propagate in the GaSb layer. The regularly spaced and triangular pattern observed in the 115 nm GaAs layer (STEM image Figure 3a) is attributed to the underlying initial APD distribution combined with the annihilation mechanism described above. The interface between GaSb and GaAs is distorted because it is in close vicinity of the APDs, but the growth of the GaSb layer then efficiently flattens the surface as demonstrated by the AFM, showing no residual roughness related to APDs.

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The same strategy was then used on 0.2° Si substrates (Figure 4a,b). This time, a 150 nm-thick GaSb layer was necessary to smooth the surface after a GaAs layer of 250 nm was grown to bury the APDs. Again, the AFM image shows the same APBsfree smooth "step-flow surface" with a low roughness of 0.85 nm (Figure 4a). A slight cross-hatch appears in the AFM topographic images of the 1.5 µm GaSb buffer Figure 4b. STEM images exhibit larger but still regularly spaced APDs (Figure 4a), in sharp contrast with the random geometry of the APDs formed in the "nucleation-driven" initial distribution (Figure 4b). Additionally, the STEM image of Figure 4a confirms that APBs do not propagate in the GaSb layer. The boundaries appear in dark contrast compared to the rest of the structure and are even more visible than on 0.5°. All APDs are contained and buried within 250 nm of GaAs. This composite APB-free, GaAs/GaSb buffer has therefore a total thickness of 400 nm (Figure 4a), which represents an improvement by a factor of \approx 3.7 compared to the results obtained in the nucleation-driven initial APD distribution with 0.2° miscut substrate (1.5 µm, Figure 4b).



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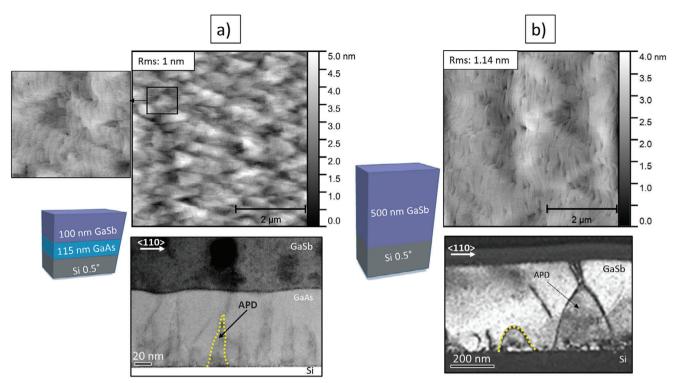


Figure 3. 5 μ m × 5 μ m AFM and TEM images of a) the 215 nm GaAs/GaSb composite buffer layer on Si 0.5°, b) a 500 nm GaSb on Si 0.5° sample where APDs are buried in nucleation-driven initial phase distribution. Examples of APBs are highlighted with yellow dashed lines.

3.3. Ultra-thin buffer layers: control of the nucleation by "terrace-driven" initial phase distribution in GaAs and antiphase domains burying during GaSb overgrowth

We then investigated an alternative strategy consisting in using a thinner (50 nm) GaAs layer before starting the growth of a thicker (450 nm) GaSb layer on Si 0.5°. In this case, the burying process of the APDs is expected to be incomplete when the GaSb growth starts, because the GaAs layer is much thinner than the 110-120 nm required to obtain an APD-free GaAs surface.^[23] The sample's morphology was imaged by AFM, and showed an APB-free surface, with a roughness of 1 nm (Figure 5a). A few straight segments are visible on the sample surface and have been identified as being micro-twins by cross-comparison with STEM data. The formation of these defects could be due to the low growth temperature of the GaAs or from dislocation dissociation at the GaSb on the GaAs interface. However, their density is very low and is not believed to be the most critical factor for the crystalline quality at this stage. Cross-section STEM images reveal the same "triangular" and regularly spaced APDs, with most of the boundaries intersecting and ending at the GaSb/GaAs interface (Figure 5b). This confirms that APDs were not buried when the GaSb growth was started. It is however noteworthy that APBs do not propagate through the GaSb layer, revealing that APBs (such as the one highlighted in yellow) are forced to stop close to the GaSb/GaAs interface.

Although a detailed study of the mechanism accelerating the burying of the APDs is out of the scope of this paper, it is very efficient: APDs are buried within \approx 50 nm of GaAs, which is a further reduction by a factor of 2 as compared to the previous

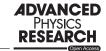
strategy (\approx 115 nm), and a factor of 10 with respect to the direct growth of GaSb on Si (\approx 500 nm).

In addition, TEM images show a well-defined array of regularly spaced misfit dislocations at the GaSb/GaAs interface, as indicated by the white arrows in the inserts of Figure 5c,d, due to the large lattice mismatch (7.8%) between GaSb and GaAs. To clarify the microstructure of the misfit dislocation array, inverse fast Fourier transform (IFFT) analyses were performed on the cross-section image of Figure 5d. The filtered TEM images in **Figure 6** clearly show the dislocation distribution and structure. The lattice fringes were selectively reconstructed by applying an IFFT to the circled spots. This process makes each additional half {111} plane associated with dislocations visible, and the presence of two extra half-planes is characteristic of an edge-type Lomer dislocation core. This relaxation by the generation of a misfit dislocations network at the GaSb/GaAs interface has previously been reported.^[42–44]

The experiment was then repeated for the growth of GaSb/GaAs on Si with a miscut of 0.2° . A first sample, with a 100 nm-thick GaSb layer on top of 100 nm of GaAs grown on Si 0.2° was analyzed. Again, the GaAs thickness was chosen to be much smaller than the previously determined value required for burying the APDs (in the 200 to 300 nm range, see Figure 2). Figure 7a displays a 2 × 2 μ m² AFM image of the resulting sample surface. Two phases can be identified (APD is overlaid in yellow and MPD in blue), and are arranged in a regular APD/MPD pattern, with a periodicity of ≈140 nm. APDs are thus not fully buried in this structure, and the surface morphology reveals that the APD/MPD distribution closely follows that of the underlying GaAs layer. Therefore, transitioning to the growth of GaSb did

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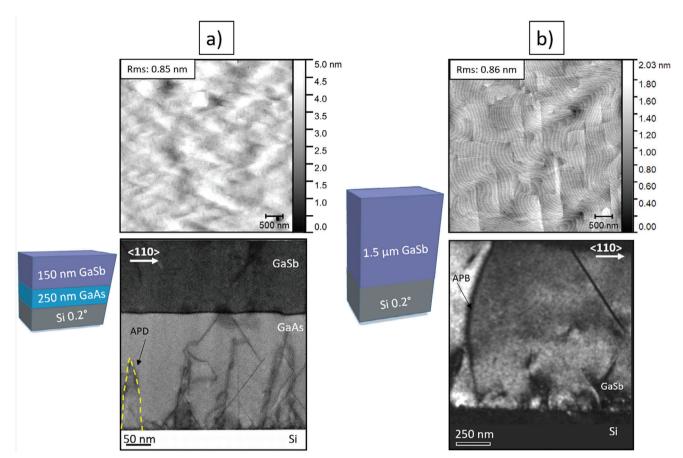


Figure 4. 5 μ m \times 5 μ m AFM and TEM images of a) optimized thin buffer sample of 400 nm on Si 0.2° and comparison with b) buffer of 1.5 μ m of GaSb on Si 0.2°. Example of APBs highlighted with yellow dashed lines.

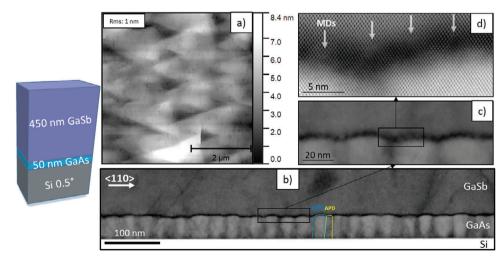


Figure 5. a) 5 μ m × 5 μ m AFM, and b–d) BF-STEM images of the sample with 50 nm GaAs at 350 °C followed by 450 nm GaAs at 450 °C on Si 0.5°. MPD and APD are respectively highlighted in blue and yellow on the cross-section STEM image and misfits dislocations are indicated by white arrows in the insert.



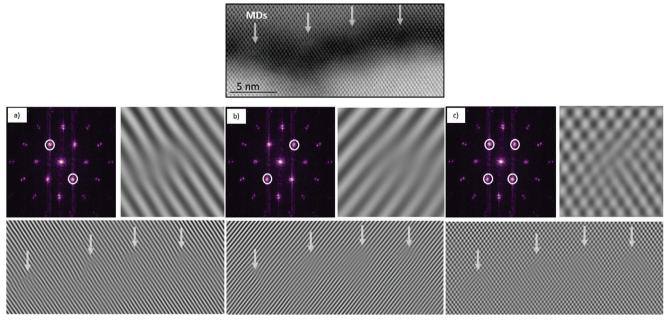


Figure 6. Fast Fourier transform (FFT) and inverse FFT images obtained with the Gwyddion software and associated with the circled spots in white, including enlarged examples of extra {111} half-planes for each case.

not lead to a rapid burying of the APDs, in contrast to the results presented above for a 0.5° miscut. Further inspection of the image allows to elucidate the difference between the two cases: the zoomed AFM image of Figure 7a shows that the GaSb growth within each domain is governed by a spiral growth mode due to the screw component of the many threading dislocations present

in the GaSb layer. This behavior is comparable to what is observed in the case of GaSb growth on GaAs(001) substrates,^[45,46] although here, the pyramids are incomplete due to the limited width of the stripes. The spiral growth mode is allowed by the very small miscut (0.2°), whereas it is forbidden in the 0.5° miscut case.

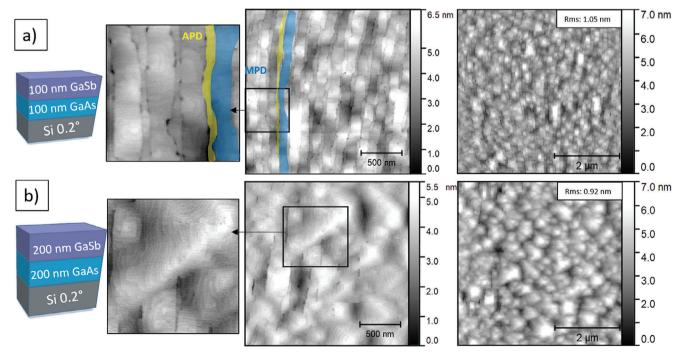


Figure 7. a) 5 μ m × 5 μ m and 2 μ m × 2 μ m AFM image of the surface of a sample with a GaAs layer of 100 nm and 100 nm GaSb on Si 0.2° with enlargement on pyramids, and dislocations contained in APBs, b) AFM image of the surface of a sample with a thinner GaAs layer of 200 and 200 nm GaSb on Si 0.2° with enlargement on pyramids and remaining APDs.

Both GaAs and GaSb layer thicknesses were then increased to 200 nm, to improve the APD burying process within GaAs before starting the GaSb growth. This proved relatively effective, as it resulted in narrower APDs stripes, but APDs were not completely buried yet, despite a total thickness of 400 nm (Figure 7b).

It can be concluded that at very low miscut angles (0.2° and below) completely burying the APDs in GaAs is beneficial for very small miscuts, where GaSb follows a spiral growth mode within the MPD stripes. Between 0.2° and 0.5°, the Si terrace widths become too narrow to allow the spiral formation, therefore leading to a growth mode transition. Hence, initiating the GaSb layer growth before complete burying is more effective for larger miscuts (typically 0.5° and above) due to the step-flow growth mode.

4. Conclusion

In summary, we have studied the APBs annihilation process in the case of composite GaSb/GaAs buffer layers grown on Si(001) with miscut angles of 0.5 and 0.2° in the [110] direction. The original idea introduced in this paper, to achieve thinner buffers, is to take advantage of the terrace-driven initial phase distribution obtained with GaAs on Si (impossible to achieve using GaSb on Si because of the much larger size of the stable island), before transitioning to a GaSb step-flow growth mode to flatten the surface. The complete overgrowth of the APDs was obtained in GaAs \approx 115 nm on 0.5° and 250 nm on 0.2° substrates, and GaSb APB-free surfaces were then demonstrated for a total composite GaSb/GaAs buffer thickness of 215 and 400 nm respectively. This represents a substantial improvement by factors \approx 2 and 4, respectively, compared to our previous results obtained in nucleation-driven regimes with GaSb buffers on Si 0.5 and 0.2°.

Another strategy was then explored, based on starting the GaSb growth before the APDs are completely buried within GaAs. Our findings on 0.5° Si suggest the possibility of reducing the GaAs thickness down to 50 nm because an even faster burying process, which remains to be fully elucidated, occurs at the GaSb on GaAs interface. The pyramidal growth mode of GaSb on GaAs on a 0.2° miscut Si substrate, however, prevents the same mechanism from occurring, as it reintroduces steps in the two perpendicular [110] directions within each polar domain. In this case, both domains grow on average at the same rate because both the APD and MPD have the same number of III- and V-steps.

These results demonstrate the possibility of reducing the overall buffer thickness by combining the advantages of the terracedriven phase distribution obtained with the growth of GaAs and the step-flow growth mode of the GaSb layer, and the potential for simplified growth requirements for APBs-free high-quality III–V integration on Si.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

antiphase domain, gallium antimonide, gallium arsenide, III-V on Si, molecular beam epitaxy, semiconductor

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