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Visualization of P⁺ JTE Embedded Rings Used for Peripheral Protection of High Voltage Schottky Diodes by the Optical Beam Induced Current (OBIC) Technique

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Abstract. This paper presents micro-OBIC measurements performed at different biasing on two power devices protected by a combination of P⁺ rings embedded in a JTE Zone. Thanks to the micro-OBIC micrometer spatial resolution, small gaps can be visible on OBIC profiles. Thus, the spatial variation of the micro-OBIC signal accurately reflects the topology of the periphery protection: combination of JTE and rings and channel stopper. These measurements agree with the electric field distribution (calculated by finite element method) along the structure.

Introduction

In order to take full advantage of the benefits offered by Silicon Carbide (SiC) and to avoid premature breakdown (previous to avalanche) of high voltage devices, it is mandatory to have efficient edge termination such as MESA, JTE, field rings, rings assisted JTE, embedded rings into a JTE or a combination of all these single termination as described by Godignon in [1]. The designer has an almost unlimited choice, as long as he respects the constraints of technological manufacturing. To determine the precise dimensions of the multiple geometrical and process parameters, he can effectively rely on Technology Computer-Aided Design (TCAD), by examining the distribution of the electric field in the semiconductor. However, this requires an enormous amount of computing time.

The Optical Beam induced Current (OBIC) is a non-destructive characterization technique, which has been previously used to characterize High Voltage (HV) Si and SiC devices [2, 3, 4]. When applying a focused UV laser beam into a biased Silicon Carbide device, electron-hole pairs can be generated. Within the space charge region, the electric field drives the collected carriers and a resulting current, called Optical Beam induced Current (OBIC), can be measured. The induced current is directly related to the electrical field in the device. The OBIC characterization can support the technology computer-aided design (TCAD) and the device processing to properly optimize the efficiency of the edge protection by analyzing the electric field distribution in the structure, especially at the junction periphery. In this work, our OBIC test-bench with a micro-meter spatial resolution allowed to characterize the periphery of SiC 1.2kV JBS diodes with a high spatial resolution and compare the results with the electric field distribution calculated from TCAD simulations.

Results and Analysis

Once the reverse bias voltage has stabilized, the diode can be scanned from the edge of the diode anode towards the periphery. Figure 3 exhibits the OBIC current for different voltages (100V and 300V) for both diode A and B. The impact of the implanted rings in the JTE on the OBIC signal can be now clearly seen (zone A) as well as the JTE length (zone B). The current intensity increases sharply with the applied reverse voltage. In zone C, the OBIC signal decreases slowly probably due to the interface charges between passivation oxide and the SiC. The impact of the channel stopper (zone D) is also observed as the OBIC signal is nearly zero.

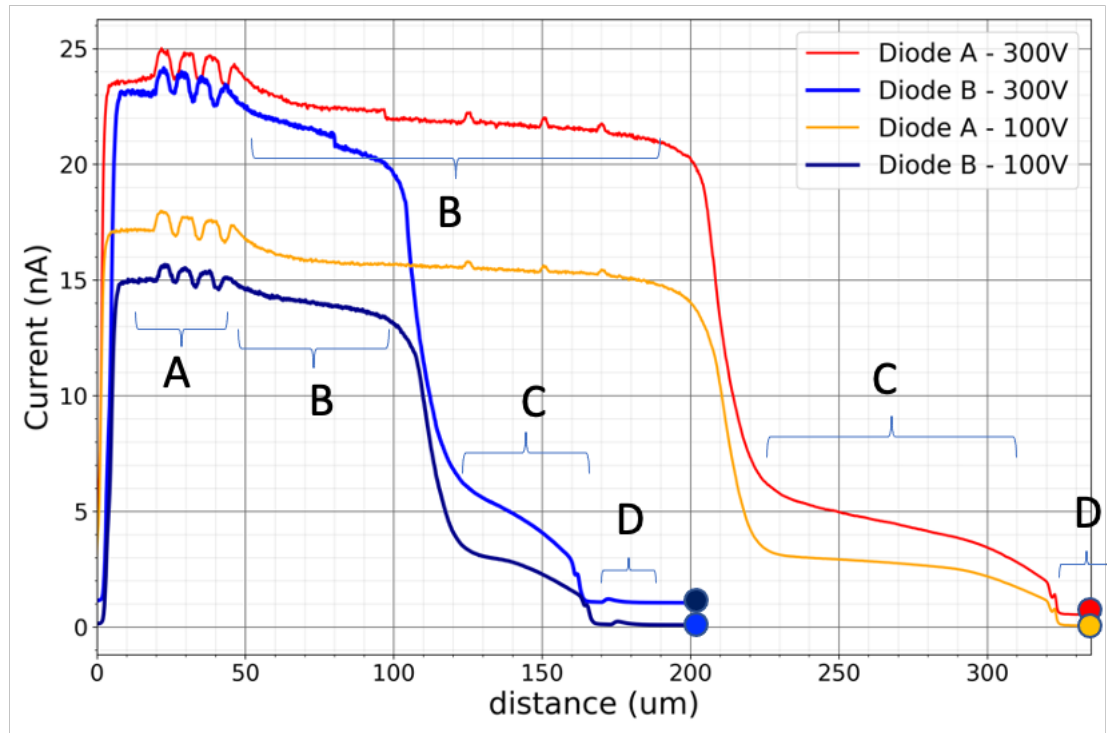


Fig. 3. Micro-OBIC 1D-scans under two biasing voltages for diodes A and B. 4 zones are defined: A: implanted rings, B: JTE, C: margin and D: channel stopper.

For the longest JTE, additional scans have been performed for voltages ranging from 50V up to 300V. As the measurements are performed in air, the reverse voltage is limited. Fig. 4 shows the corresponding scans. In zone A, one can observe 4 peaks which are related to the 3 rings (one peak for each ring and one additional for the P^+ border inside the JTE). At 300V the highest peak is located in the first inner ring.

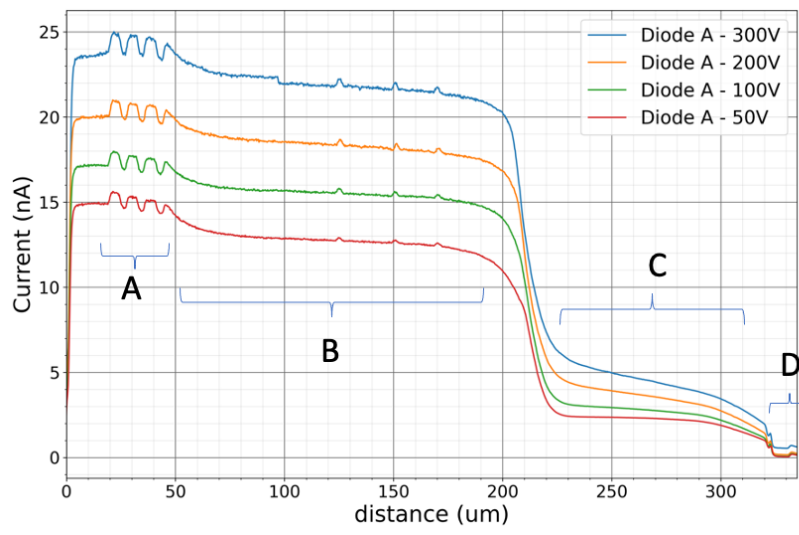


Fig. 4. Micro-OBIC 1D-scans for several voltages for diodes A including the different termination's zones. 4 zones are defined: A: implanted rings, B: JTE, C: margin and D: channel stopper.

To support the idea that simulation is an aid to the design of periphery protection, we have simulated the structure and examined the electric field. TCAD simulation using SynopsysTM [7] have been performed.

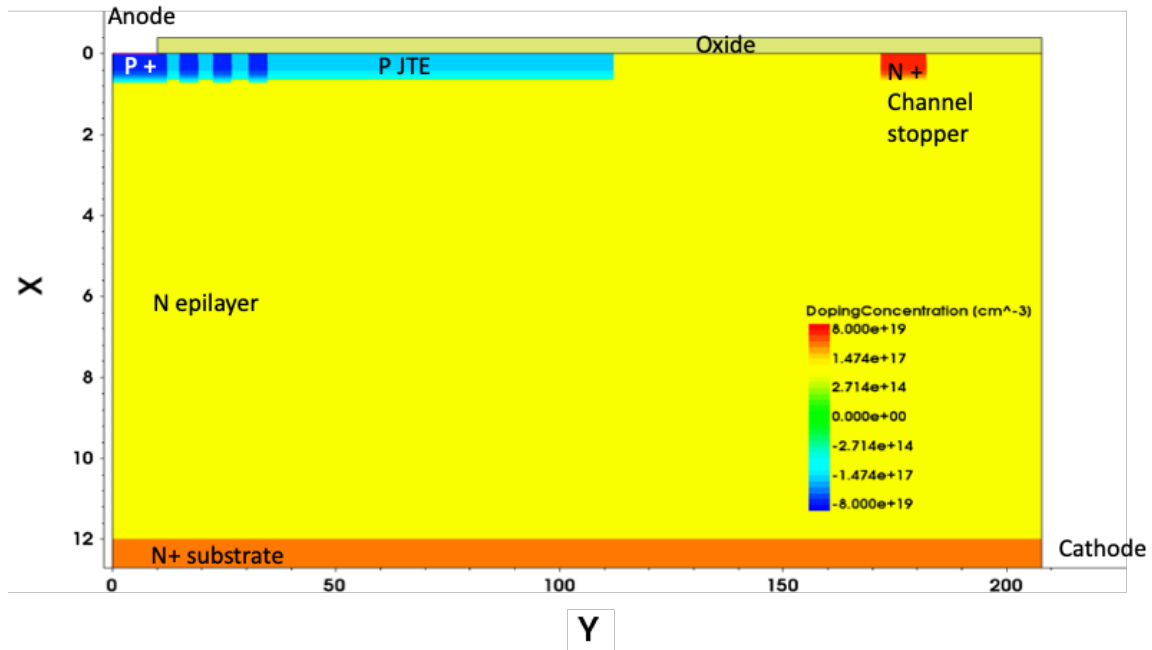


Fig. 5. 2D TCAD diode structure.

Fig. 5 depicts the 2D structure which has been simulated by Synopsys Sentaurus TCAD. The present structure includes all the features of the one shown in Fig.1. Diodes A and B all derive from it by varying the JTE length. Reverse off-state simulations up to 300 V have been performed. To save computing time and memory, the N⁺ substrate has been thinned, as its thickness is will not have a significant impact.

Fig.6 shows the 2D the electric field and the respective isolines computed from TCAD simulations under 50 V, 100 V, 200 V and 300 V. The dimensions of the peripheral termination are from diode A. As the applied voltage is increased, the electric field spreads further into the epitaxial layer. It can be noticed the space charge area depth is about the penetration depth of the laser beam, whose amplitude exponentially decreases. Diode B peripheral termination has also been simulated but, for clarity purpose, will not be shown as similar observations can be made.

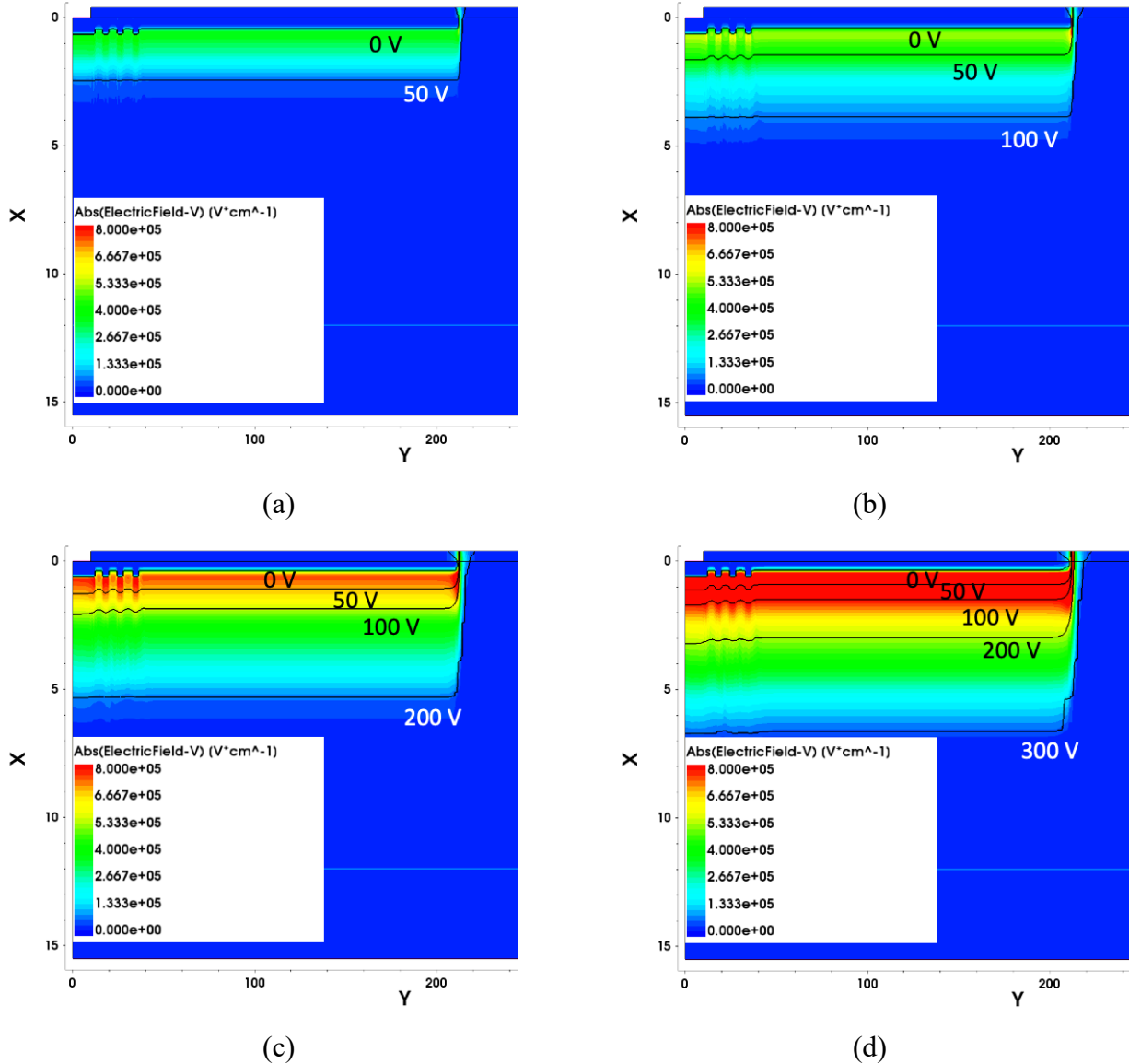


Fig. 6. TCAD Electric Field, and potential isolines of the diode A peripheral protection under several reverse voltages (a): 50 V, (b): 100 V, (c): 200 V and (d): 300 V.

The electric field distribution along the x-axis under a reverse voltage of 200V is presented in Fig. 7a. The impact of the implanted rings is clearly observed in zone A. The JTE length (for diode A and B) is clearly seen in zone B. However, with this electric simulation the electric field remains constant throughout the JTE, and do not show a slow decrease like in the OBIC measurements in Fig. 3 and 4. Interface charges have not been considered for the present simulation. However, even though the charges were included, this would not be enough to explain the difference, as charges alone would mainly cause a shift in the electric field profile. Its decrease along the horizontal axis may be explained by surface leakage currents. Further simulations are then required. The same observation can be made in the C-zone between the edge of the JTE and the channel stopper. Another explanation would be a non-uniform JTE doping profile. This assumption would need to be corroborated with the JTE doping lateral profile characterization. Nonetheless, the electric field profile obtained from TCAD is clearly dependent on the applied voltage as shown in Fig. 7b which show different diode A electric profiles for different voltages. The field amplitude is voltage-dependent, and the same thing can be said for its lateral extension as shown in the inset. Furthermore, the widths of zones B and C which appear in simulations are in line with the experimental results. This corroborates the observations made for Figures 3 and 4.

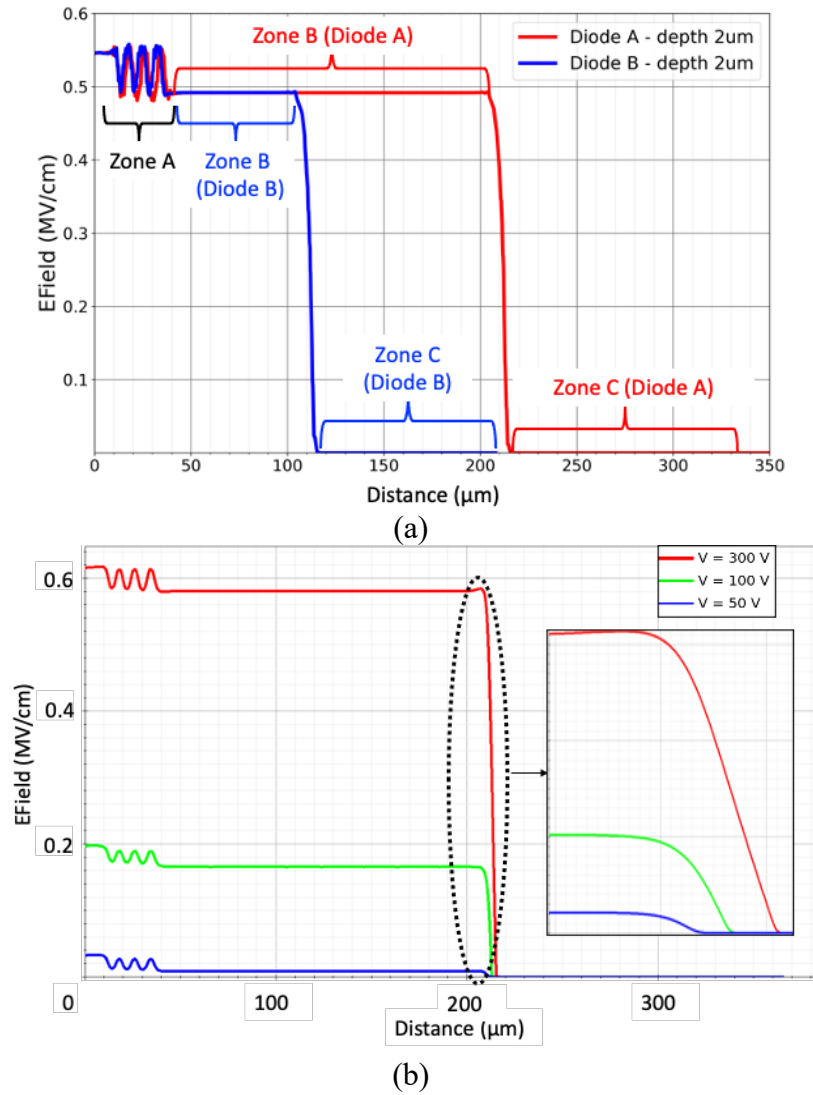


Fig. 7. (a) Electric field distribution along the periphery protection at a given depth of $2\text{ }\mu\text{m}$ at 200 V , (b) Electric field distribution along the diode A periphery protection at a given depth of $2\text{ }\mu\text{m}$ at 50 V , 100 V and 300 V .

Summary

This paper presents OBIC measurements carried out on Schottky diodes protected by a combination of JTE protection and implanted P^+ rings. 2 JTE lengths were defined and 3 rings implanted quite close together. The OBIC measurements show that the good resolution of our test bench is capable of revealing the different zones of the protection and also the impact of the applied reverse voltage. In this particular design, the highest peak is located in the first P^+ ring. TCAD simulations may be used to support the experimental results as there is good agreement between experimental results and simulations with regards to ring and JTE positions and widths. The current simulated structures are still not able to reproduce the same electric field profile as it stays constant within the P JTE region. The explanation may come from the recombination current at the oxide/semiconductor interface that is not simulated. We plan to improve our test bench with measurements in a vacuum chamber, so that we can carry out measurements at higher voltages and close to breakdown voltage.

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