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Investigation of Single-Event Effects for Space Applications: Instrumentation for In-Depth System Monitoring

André M. P. Mattos, *Student Member, IEEE*, Douglas A. Santos, *Student Member, IEEE*, Lucas M. Luza, Viyas Gupta, and Luigi Dilillo, *Member, IEEE*

Abstract

Ionizing radiation induces the degradation of electronic systems. For memory devices, this phenomenon is often observed as the corruption of the stored data and, in some cases, the occurrence of sudden increases in current consumption during the operation. In this work, we propose enhanced experimental instrumentation to perform in-depth Single-Event Effects (SEE) monitoring and analysis of electronic systems. In particular, we focus on the Single-Event Latch-up (SEL) phenomena in memory devices, in which current monitoring and control are required for testing. To expose the features and function of the proposed instrumentation, we present results for a case study of an SRAM memory that has been used on-board PROBA-V ESA satellite. For this study, we performed experimental campaigns in two different irradiation facilities with protons and heavy ions, demonstrating the instrumentation capabilities, such as synchronization, high sampling rate, fast response time, and flexibility. Using this instrumentation, we could report the cross section for the observed SEEs and further investigate their correlation with the observed current behavior. Notably, it allowed identifying that 95% of Single-Event Functional Interrupts (SEFIs) were triggered during SEL events.

Index Terms

Radiation Testing; Radiation Effects; Instrumentation; Reliability; Harsh Environments; SRAM; PROBA-V; Single-Event Latch-up; Single-Event Upset; Single-Event Functional Interrupt.

I. INTRODUCTION

Ionizing radiation induces a plethora of effects on electronic devices, leading to several types of failures that may compromise the operation of entire systems. For instance, in space applications, systems are exposed to various energetic particles (e.g., protons, heavy ions) received from three main sources: Galactic Cosmic Rays (GCR), Solar Energetic Particles (SEP), and trapped radiation [1], [2]. These radiation-induced faults can be transient or permanent depending on the device's architecture, sensitized nodes, semiconductor materials, and degree of damage, triggered either by single interactions, Single-Event Effects (SEEs), or accumulative degradation, Total Ionizing Dose (TID) and Displacement Damage (DD) [3].

In memory devices, as data retention elements, SEEs are usually observed as the corruption of the stored data. However, other effects can be observed, such as the occurrence of damaging current increases in parasitic elements of the circuit and functional mismatches during operation. Since memory elements represent a significant percentage of chip area in modern integrated systems, understanding the radiation effects in these structures is key for assessing reliability. In Static Random-Access Memories (SRAMs),

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using CMOS technology, a single cell is generally implemented with six transistors. Each cell is capable of storing a bit, due to its two stable states (high and low voltage levels of cell nodes). CMOS-based electronics are commonly susceptible to latch-ups due to a parasitic structure (thyristor) that is nominally in high impedance. When an ionizing particle interacts with the thyristor, a latch-up might be triggered, and it is referred to as a Single-Event Latch-up (SEL). During this event, the thyristor enters a conducting state, firstly generating a high-current state in the cell and, just after, in the neighboring circuits. If this high-current state is not blocked, the device may have permanent damage due to thermal runaway (Joule effect) [4], [5].

In order to investigate the system's response to the induced faults, high-reliability systems are subject to thorough characterization under radiation conditions. Testing and applying mitigation techniques are imperative for systems in the space environment with consistent and dependable operation over the mission lifetime. Hence, due to its importance, test methodologies evolved over the years to accommodate the growing complexity of the devices and achieve assertive results. Experimental tests using particle accelerators became a standard step towards reliable electronics, in which developers expose their systems and fault mitigation strategies to radiation using representative fault stimuli [6]. Depending on complexity and requirements, these systems are approached differently to achieve more feasibility during the development process, ranging from simple pass/fail tests to more robust analyses with the investigation of underlying phenomena [7].

Performing simplified screening of systems is a convenient strategy to reasonably assess non-critical elements of a system or perform an initial characterization, reducing project resource utilization and development efforts [8], [9]. The risk of this method is estimated and accepted in the early stage of development. To achieve more accurate results, it is important to provide comprehensive test stimuli [10]. Moreover, to improve the experimental setup capabilities and test coverage, further tests with dedicated equipment are required, in which precise and configurable measurements are possible [11]. Finally, for a better understanding of the SEE response, enhancing observability is an essential aspect to be addressed, as further discussed in this article.

In this work, we present compact experimental instrumentation to perform SEL testing of memories with extended observability to report other radiation-induced faults and synchronization to correlate these faults with the monitored current behavior. Despite focusing on SELs, this study includes the investigation of Single-Event Upsets (SEUs) and Single-Event Functional Interrupts (SEFIs). Here, we present the instrumentation applicability through a case study focusing on an SRAM memory, but the instrumentation and methodology can be applied to different types of memories and even extended to other complex systems (e.g., processors, systems-on-chip). The studied memory is a Commercial Off-The-Shelf (COTS) 4Mib SRAM with a 16-bit parallel interface: Samsung's K6R4016V1D-TI10 [12], from the year 2001 (Rev. D). It was employed on-board PROBA-V [13], a satellite mission from the European Space Agency (ESA). We investigate this memory based on in-flight behavior related to SEL events and through two experimental campaigns with proton and heavy-ion accelerated beams, in which the proposed instrumentation and experiments are discussed in this article, and the characterization results are subject to a complementary publication [14]. For that, we introduce relevant instrumentation enhancements, such as improved test modes, log synchronization, and measurements for achieving more assertive results in comparison to baseline SEL characterization.

The remainder of the paper is structured as follows. Section II introduces related work and key aspects of the testing methodology targeting in-depth analysis. Section III presents the proposed experimental setup. Section IV provides results from the performed irradiation campaigns and examples of analysis exploiting the instrumentation capabilities. Section V discusses the capabilities, limitations, and potential extension of the proposed approach. Finally, Section VI gives conclusions on this work.

II. RELATED WORK

This section describes different approaches and objectives of instrumentation targeting SEL testing in particle accelerators. It does not intend to be an extensive review of the subject but rather provides an

insightful discussion of the practices and solutions found in the literature.

A. Simplified Screening

SEL testing can be primarily simplified to monitoring transients in the supply power of an operating system by measuring overcurrent events. When this transient is detected, the supply power is limited and cycled to prevent permanent damage and enable continuous testing with a single device. Despite a straightforward concept, there are several factors that influence the behavior of a system before, during, and after a SEL, and understanding this may be essential for a specific purpose. For example, an SEL can be functionally recoverable or fully destructive depending on the affected structures and its duration; the system may be functional or not during the overcurrent state; evaluating complex SEL mitigation schemes might be the main test objective rather than counting only event rates; or overcurrent events can even be more subtle and hard to differentiate from dynamic consumption fluctuations.

Thus, a simplified screening of these systems is appropriate for specific purposes, as seen in [8], [9]. In these works, the proposed approach is to perform a preliminary selection of components with respect to their SEE (mainly SEL) sensitivity, reducing testing efforts when multiple device options are available. Similarly, in [15], a simplified SEL testing scheme is used since the objective is to investigate differences in various components with particular architectures, technologies, and manufacturers, instead of deeply investigating the particularities of these devices. These simplified approaches may lead to limited conclusions about the system's behavior and knowledge of underlying phenomena. However, it provides a starting point for later comprehensive and accurate testing in a more effective and direct manner. Thus, it must be consciously applied and analyzed.

B. Comprehensive test stimuli

Representative testing schemes require realistic stimuli to be applied to the Device Under Test (DUT). In this case, monitoring SEL continues similarly as mentioned, but more attention is given to achieving accurate and meaningful cross sections under different test conditions, as seen in [16] for SELs and more generally for SEEs in [17]. With proper stimuli and test modes, the target device's structures are properly sensitized and the entire device is homogeneously stressed over the different runs and modes. Using realistic and diverse test patterns supports later correlation with real behavior due to similar resource utilization. For example, in the case of a memory device, static and dynamic test algorithms should be applied. Static tests consist of writing a fixed pattern in the memory and performing a readback operation after a significant period to check the corrupted bits. In dynamic testing, the memory is constantly written and read following predefined patterns, and the errors are reported when detected. Several classical memory test algorithms can be found in the literature [18] and some were evaluated for radiation testing [19], [10]. In summary, test modes are important to expose and provide proper stimuli for exposing different fault mechanisms, resulting in more comprehensive and accurate testing. Also, it reduces test biases that may be created by simplistic or specific test patterns.

C. Dedicated equipment

In order to perform specific testing and monitor systems in real environments, dedicated equipment is required. In these cases, direct current measurements are preferred and provide better accuracy for SEL detection and classification. The equipment should be accurate, automated, and provide a fast response. In [11], the authors propose dedicated equipment and procedures to perform precise SEL characterization. The proposed setup is robust and designed to be used in challenging testing environments. It is composed of analog front-end components for measurement and conditioning of the DUT current, power switches for handling the supply line, and a flash-based FPGA for controlling signals and logging. In [20], in-flight data is compared with ground estimations based on experiments in particle accelerators. For in-flight monitoring, different approaches can be used, but dedicated equipment is implemented to be integrated with the system and be resilient to the space environment, as demonstrated in [21].

D. This work

The contribution of this work is to enhance the observation of dedicated SEL monitoring equipment by providing synchronized monitoring of the supply current and data errors in the memory, which are generated and observed with static and dynamic algorithms. It is worth noting that the proposed synchronization occurs in the tightly coupled measuring instrument itself and not externally in the monitoring equipment, as previously referred. It is important to acquire precise and coherent timestamps between the various observation points of experimental instrumentation. Enhanced time reporting provides the elements to correlate observed behaviors, find patterns, and elaborate novel hypotheses. For instance, one can correlate current spikes with certain events observed at the logical level in a circuit.

For that, we propose, implement, and analyze dedicated experimental equipment with those characteristics. Similar to [11], we proposed a monitoring system based on a flash-based FPGA for the controller and similar strategies for acquiring the current measurements. However, the monitoring was also extended to the IO lines of the DUT. Moreover, we included in the SEL reporting the simultaneous information regarding the errors (SEUs and SEFIs) dynamically induced in the memory.

III. PROPOSED INSTRUMENTATION

In this section, we describe the proposed instrumentation designed for in-depth analysis of SELs in the SRAM memories used for this case study.

A. Test setup and instrumentation

Figure 1 presents the proposed experimental setup. The system is composed of two main boards: a controller board, hosting an FPGA, and a test board, where the SRAM and measuring components were included. The test board was used to provide the electrical interface for the additional devices and facilitate a stable attachment of the controller board. This board includes the hardware for the load switches, current sensors, serial converters, and the DUT (SRAM) itself. We used dedicated digital current sensors, which allowed precise measuring and a convenient interface with the controller. The serial converters were used to provide the connection with a host computer through a robust protocol for receiving data and sending commands. The host computer continuously saves, manages, and displays the acquired experimental data. When required, the experiment operator can interact with the system using the host computer with a set of commands (e.g., start a specific test, stop a run, perform a functional test, change test parameters). Using this scheme, we achieved a compact, robust, and precise experimental setup, enabling tests in constrained spaces (e.g., the vacuum chamber used for heavy-ion irradiation) with enhanced observability and simplifying the test equipment.

Figure 2 details the architecture of the proposed instrumentation. In the controller board, we implemented: a timing management module for synchronizing all internal modules; two serial interfaces for sending the test data to the host computer; an SRAM controller for handling the memory operations; a test engine to execute various test algorithms; and the necessary logic for handling the measurements and load switches. It is worth mentioning that the controller was implemented in a COTS flash-based FPGA, in which the configuration memory is more robust to radiation effects [22], and the design included Triple Modular Redundancy (TMR) in the most critical elements to ensure proper operation during the tests. Hence, the controlling loop used the test algorithms and current monitoring to define the execution throughout the experiment and trigger the SEL protection and reporting.

This setup was proposed to allow flexibility, precise and coherent measurements, and functionally representative test stimuli. Since the experiments focus on SEL characterization, we designed a test board where current monitoring is done in the memory supply line and inputs/outputs (IOs). This is achieved by placing the current sensors in the supply lines of both the SRAM itself and the IO banks of the FPGA that interface to the memory. This additional IO monitoring and protection was used since these IOs contribute to the current consumption of the memory (as later shown in Figure 5) and could be important to properly suppress ongoing SELs. Thus, the power supply of the FPGA IO banks is cut, and its interface signals are put in high impedance during the cut time to ensure proper power cycling.

With the controlling board simultaneously managing these measurements and the test algorithms, it allowed coherent time stamping of two meaningful parameters during event occurrence, i.e., current variations and detected bit SEUs. In particular, this instrumentation is capable of reporting the actual current during an SEL, with the event ongoing. These features are essential to perform specific analyses that are detailed in Section IV.

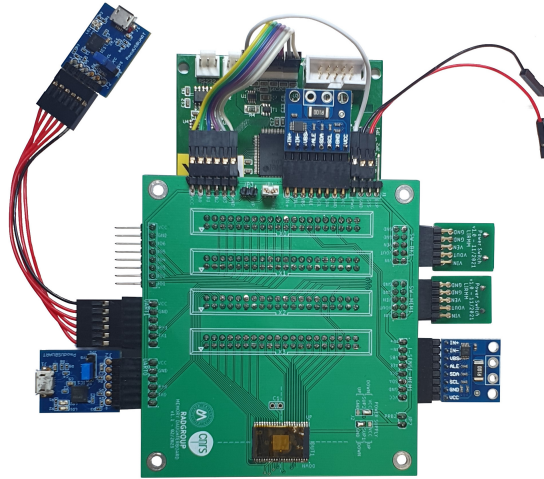


Fig. 1. Proposed experimental setup.

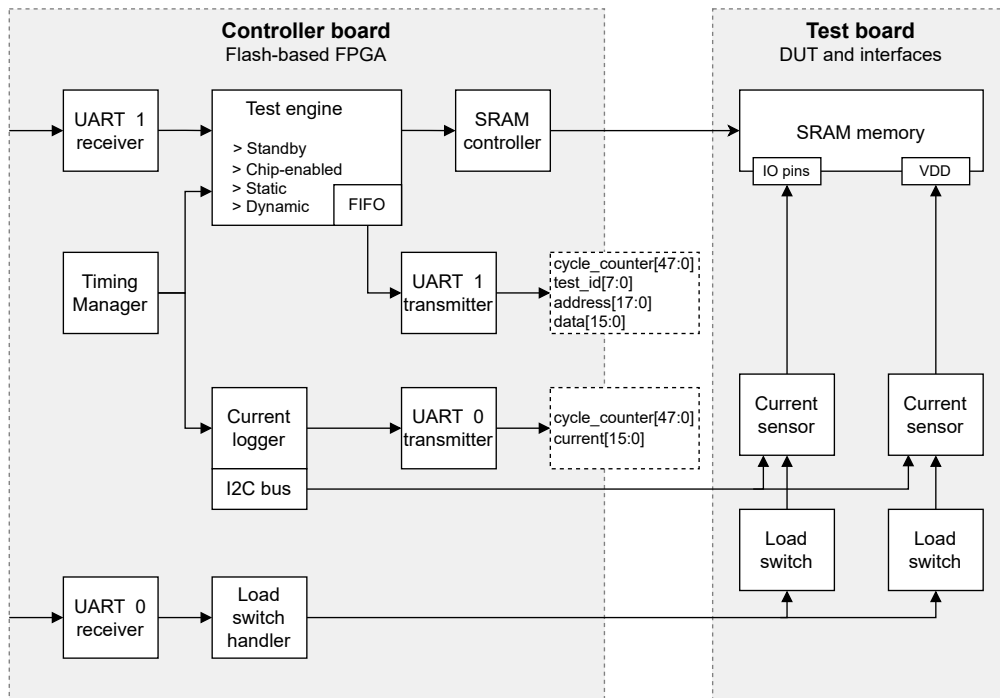


Fig. 2. Architecture of the proposed experimental setup.

B. Test execution and monitoring

The plot in Figure 3 shows the SEL monitoring approach. The power switches feeding the memory are disabled after a hold time following the detected SEL, allowing monitoring of the memory behavior under the initial part of the SEL. The SEL detection is triggered when the current feeding the memory is over

a given threshold value. This current value is reasonably large to ensure the memory function and not trigger false SEL, and, at the same time, small enough to always be triggered with actual SEL as soon as possible. The hold time is short enough to protect the circuit from unrecoverable damage. The power is enabled again after a cut time to recover the memory functionality and continue the test execution. Hold and cut times are configurable prior to the test run and depend on the experimental target. For this work, we defined 50 ms and 200 ms, respectively. The current threshold is also configurable and was set at 80 mA for most of the experiment. Using these configurable parameters, we did test runs at the end of the experiment with different variations to verify the full effect of the induced SELs. It is worth mentioning that the current threshold allowed additional tests without the need to physically access the setup inside the irradiation room since it can be updated in real-time through the host computer using the available commands.

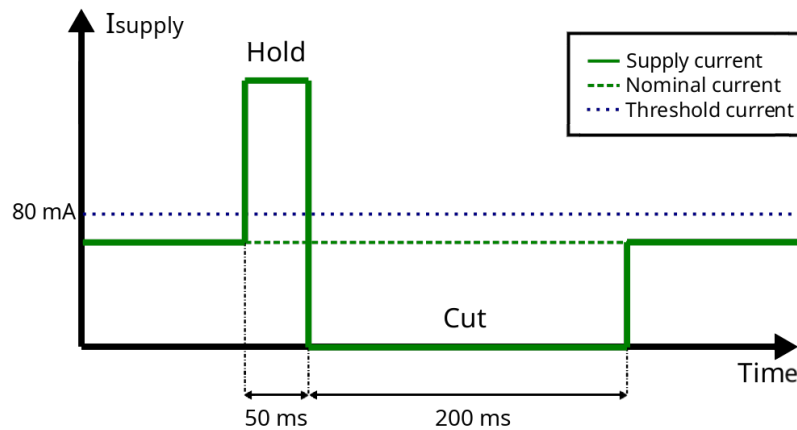


Fig. 3. SEL monitoring method.

Four test modes were used to explore realistic fault models: 1. standby, when no operations are performed, leaving the device in a powered-on state; 2. chip-enabled, similar to standby, but the memory chip-select is set (now, the memory controlling logic is powered); 3. static, the memory is written, then, after a sufficient period, it is read back; and 4. dynamic, in which the memory is constantly written and read using two different algorithms and errors are reported when detected by read accesses. In particular, for the dynamic mode, we applied two algorithms discussed and tested in [10]: March C-, displayed in 1, and March Dynamic Stress, displayed in 2. In dynamic test mode, the algorithms constantly access the memory by employing read and write operations in order to emulate realistic applications and detect functional faults. In the equations 1 and 2, the arrow indicates the addressing order (either ' \uparrow ' increasing or ' \downarrow ' decreasing), 'w' (write), and 'r' (read) indicates the operation, and the following boolean number indicates the data background. The algorithms are composed of elements indicated by the arrow, followed by the operations in parenthesis. In our work, the operations enclosed by the parenthesis are performed in sequence in each memory address. When the addressing order is ' \uparrow ', the operations are executed from the address 0 to N, and when it is ' \downarrow ', the operations are executed from the address N down to 0, being N the highest memory address. Thus, e.g., the element ' \uparrow (r0, w1)', goes from the first address up to the last one, applying a read operation (where a solid '0' data background is expected) followed by a write operation (using the solid '1') in each address. A bracket pair '{ }' delimits a complete dynamic test algorithm.

$\uparrow (w0);$
 $\{\uparrow (r0, w1); \uparrow (r1, w0); \downarrow (r0, w1); \downarrow (r1, w0); \uparrow (r0); \}$
 (1)

$\uparrow (w1);$
 $\{\uparrow (r1, w0, r0, r0, r0, r0);$
 $\uparrow (r0, w1, r1, r1, r1, r1);$
 $\uparrow (r1, w0, r0, r0, r0, r0);$
 $\downarrow (r0, w1, r1, r1, r1, r1);$
 $\downarrow (r1, w0, r0, r0, r0, r0);$
 $\uparrow (r0, w1, r1, r1, r1, r1); \}$
 (2)

In Figure 4, the test flow is presented, which details all the steps to perform the static and dynamic tests. This procedure was repeated for all the specimens of memories throughout the experiment when feasible. Some calibration runs were performed for every beam configuration change due to the high device sensitivity to the radiation sources. This was more important for heavy ions since the error rates were very high for certain Linear Energy Transfer (LET) values. As shown in the figure, the test flow forecasts functional checks to identify the device state before and after starting irradiation, and at the end, after the power cycle. The main test conditions for defining the duration of a run are the accumulated fluence and the number of detected SELs. In particular, the runs were performed with a fluence of up to 10^7 ions/cm^2 unless a large number of SEL occurred beforehand (hundreds).

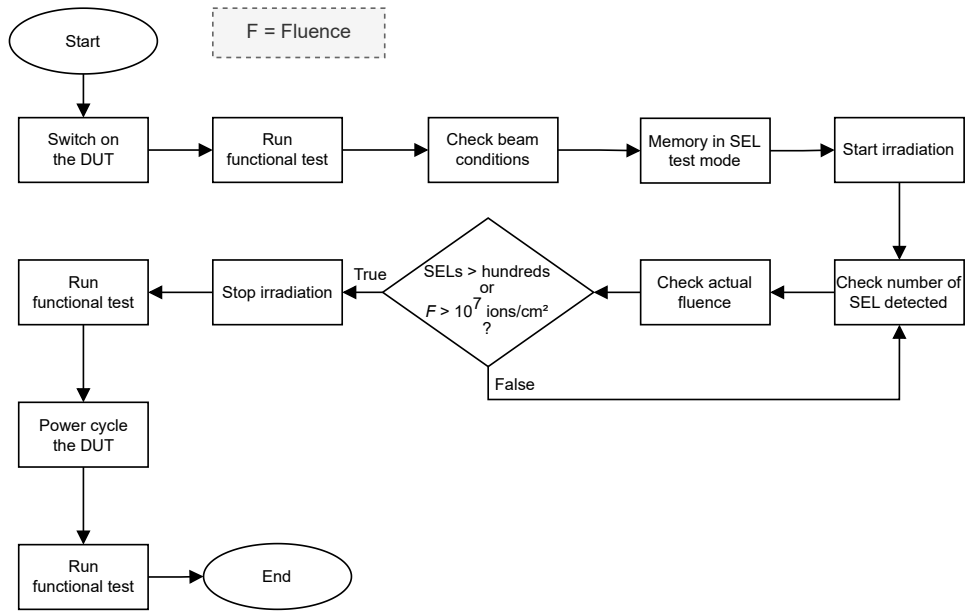


Fig. 4. Test execution flow for all test modes.

C. Measurements and reporting

The waveforms in Figure 5 show the enhanced capabilities of timing coherence achieved with the proposed instrumentation. With this type of information, we can correlate memory operations to a current level not only on the main power input but also in the IO lines. The Figure refers to a full dynamic test execution, in which each part of the algorithm is highlighted by the vertical separators and detailed with the captions at the top. The current is measured and logged in short intervals with a resolution of $25 \mu A$. Using this resolution, it is possible not only to observe the current plateaus but also minor variations during each phase of the device operation (e.g., decoding, precharge).

This system takes from $220 \mu s$ to $370 \mu s$ to acquire a current sample and switch off the power line, depending on the moment that the new sample is received in the controller from the digital sensor. Every error reported by the test engine records the cycle counter at the error detection, the test identification, and the error data and address. The current logging is concurrently performed and reports the cycle counter and current values. The cycle counter operates with a clock period of $80 ns$.

In general, for memory testing, the SEL current threshold is defined before a test run and is not modified during the execution. However, dynamic threshold changing could be a required feature to support elaborated testing schemes in complex systems. For example, for a system-on-chip with multiple power domains and a long power-up sequence, the feature described in III-B enables real-time changing of the SEL current threshold with predefined values appropriate for each stage. Furthermore, as shown in Figure 5, distinct steps of an algorithm execution may have characteristic current profiles, allowing for the adjustment of the SEL monitoring scheme according to the executed algorithm.

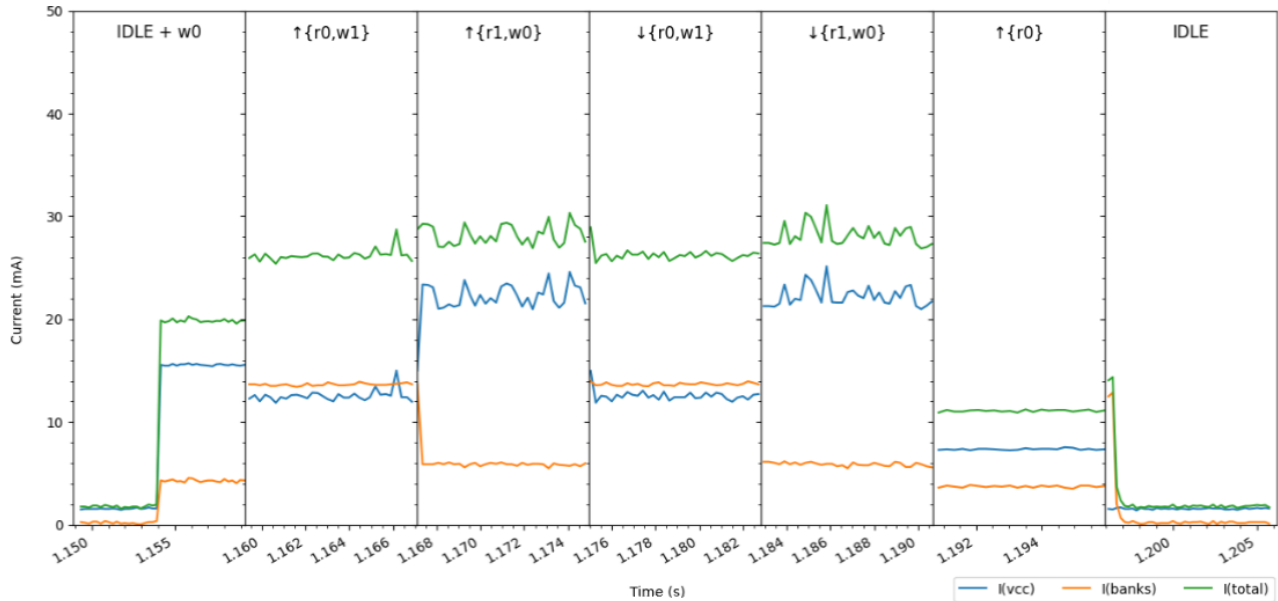


Fig. 5. Instrumentation capabilities: correlation between memory operations and current measurements.

IV. DATA ANALYSIS

We performed experiments in two facilities with different particles: heavy ions, in the Radiation Effects Facility (RADEF) at the University of Jyväskylä, Finland, and protons, in the Proton Irradiation Facility (PIF) at the Paul Scherrer Institute (PSI), Switzerland. For RADEF, the beam has a 10% homogeneity for the selected irradiation area and heavy-ion cocktail of $16.3 MeV/n$, capable of generating a flux up to approximately $3 \times 10^5 ions/cm^2/s$. The ions selection included the following species and LET (at silicon surface and vacuum mode in $MeV.cm^2/mg$): $^{17}O^{6+}$, 1.52; $^{40}Ar^{14+}$, 7.2; $^{57}Fe^{20+}$, 13.3; $^{83}Kr^{29+}$, 24.5; and $^{126}Xe^{44+}$, 48.5. In PSI, we selected the following proton energies (in MeV): 16, 29, 51, 70, 101, 151, and 200. Copper plates were used in the beam path to generate different energies and two primary proton energies were used to allow proper testing at the lower energy range (in MeV): 100 and 200. Proton fluxes of about 3×10^7 to $8 \times 10^7 p/cm^2/s$ were used, and all tests were performed at ambient room temperature and air pressure. The beam had a 10% homogeneity for the selected irradiation area and beam energies throughout the full experiment.

The experimental setup was reused for the facilities with minor adaptations. For the heavy-ion experiment, eight SRAM devices were evaluated, covering two manufacturing lots, and they required delidding for proper particle penetration. Using microscopy in the delidded chips allowed for verifying the die markings

and some internal structures. Various irradiation angles and test modes were explored in the heavy-ion campaign. For the proton experiment, four SRAM devices were used, of which two were reused from the previous experiment for checking experimental data consistency and the remaining two (from the same manufacturing lot) were pristine to increase sample size but spot potential cumulative biases, if significant. Only the most relevant test modes were applied in this campaign, based on the outcomes from the heavy-ion experiments.

As previously stated, the main objective of this work is not to present the characterization results or to extensively report cross sections, which is out of the scope of this article and subject to publication in [14]. Conversely, we present those outcomes that support the evaluation of the capabilities of the proposed instrumentation and their benefits in comparison to more traditional and simpler strategies. From the experimental results, we could observe many interesting behaviors that were decisive to corroborate or exclude formulated hypotheses and initial assumptions.

A. SEE cross sections

To present the baseline capabilities of the experimental instrumentation, we include a summary of cross sections acquired during the heavy-ion campaign, shown in Table I. The proposed instrumentation allowed the acquisition of SEL [14], SEU, and SEFI cross sections for the DUTs in a reliable manner throughout the experiment without the necessity for manual intervention inside the irradiation room. Moreover, alongside the facility's capabilities, it was possible to explore different angles, allowing measurements for additional LETs, and test four DUTs without opening the chamber, optimizing the beam utilization. As previously described in Figure 4, we targeted an accumulated fluence of $1 \times 10^7 \text{ ions/cm}^2$ or at least a hundred events for each test run. This condition was necessary to optimize the beam utilization due to the high DUT sensibility for higher LETs since hundreds of events were achieved earlier than the defined fluence. The outcomes suggest no impact on the cross section with the different test modes. Also, it is important to highlight that the SEU cross section values were artificially reduced for higher LETs due to the high number of SEL occurring. If the SEL rate is exceedingly high, the capability to retrieve the radiation-induced SEUs is reduced since the test is restarted frequently, inhibiting the possibility of retrieving all induced errors.

TABLE I
SUMMARY OF CROSS SECTIONS FOR THE HEAVY-ION EXPERIMENT.

Cross section ^{1,2}	LET [MeV.cm ² /mg]					Weibull Fitting			
	1.5	7.2	13.3	24.5	48.5	W	S	XS _{sat}	LET _{th}
XS _{SEU} [cm ² /bit]	4.62×10^{-12}	4.15×10^{-9}	1.09×10^{-8}	2.24×10^{-8}	1.20×10^{-8}	14.6	1.7	2.06×10^{-8}	1.5
XS _{SEL} [cm ² /device]	9.97×10^{-8}	3.65×10^{-7}	1.61×10^{-6}	3.46×10^{-3}	7.64×10^{-2}	25.5	7.4	1.03×10^{-1}	7.2
XS _{SEFI} [cm ² /device]	9.07×10^{-8}	-	-	3.59×10^{-3}	6.87×10^{-2}	-	-	-	-

¹ Only cross sections for perpendicular incidence in one DUT (same as flight lot) are shown; ² All tested modes included for SEL cross section and only static/dynamic for SEU and SEFI cross sections.

B. SEL current and LET correlation

For Figure 6, we performed an analysis with the intent to correlate current levels and the heavy ion LET. For that, we used the reported maximum current during an SEL event and associated it with the LET of this particular run. This analysis was done to further investigate the various SEL current levels that were recorded during irradiation. Finally, we could not observe a clear correlation between these parameters, which supported discarding the impact of LET on inducing distinct SEL types. However, this opened other possibilities that could be better investigated through a laser test campaign, in which region-specific targeting and isolation are possible. These current clusters might indicate the presence of multiple power domains or sensitive regions in the device that, when triggered by an SEL, generate distinct faulty current levels. Furthermore, in complex systems (e.g., mixed-signal integrated circuits), the SEL behavior may differ depending on affected structures in the device architecture due to their heterogeneous elements. For

instance, affecting embedded memory can lead to distinct behavior in comparison to the arithmetic logic of a processing core or even an analog circuit structure within the device.

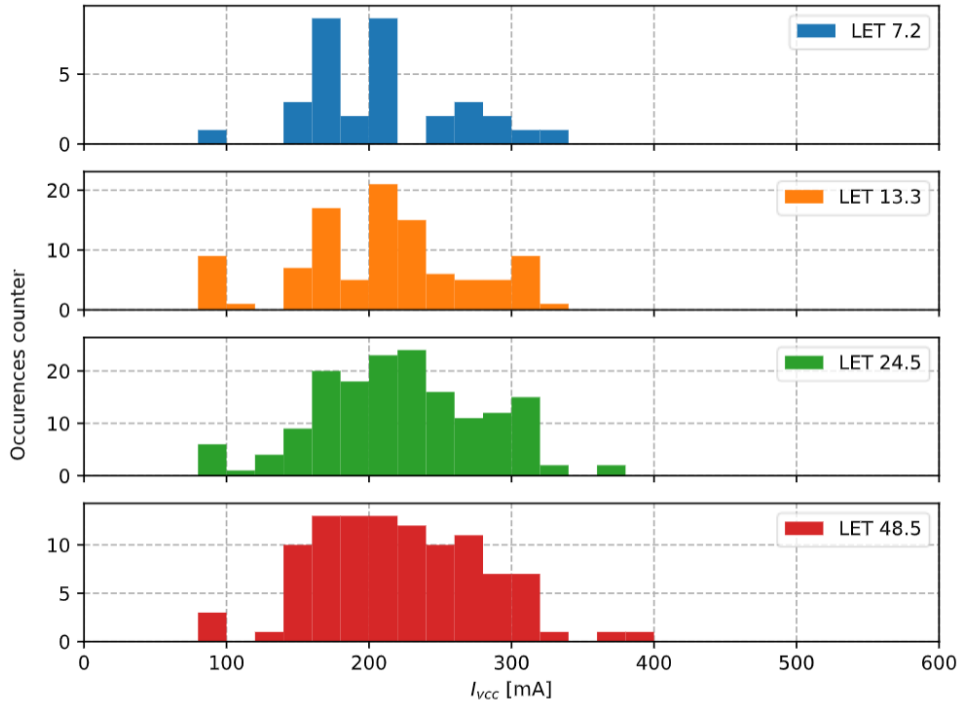


Fig. 6. Histogram of SEL current levels per LET during heavy-ion irradiation. Current levels are the average measured during the SEL period for the runs in standby mode.

C. SEL and SEFI correlation

In Figure 7, the current measurements (blue line) and error information (green dots) are superposed, allowing a time-coherent analysis of the memory behavior under irradiation. In order to support the visualization, a histogram is also presented, providing the average number of errors for a period of 25 *ms*. Using this information, it is possible to identify a peak of errors (bit upsets) more than 10 times higher than the average during a SEL. This correlation was observed in most SEL events, leading to the conclusion that SEL and error accumulation are associated events. Figure 7 is an example run that was selected from the heavy-ions campaign, but this correlation was also observed in the proton irradiation.

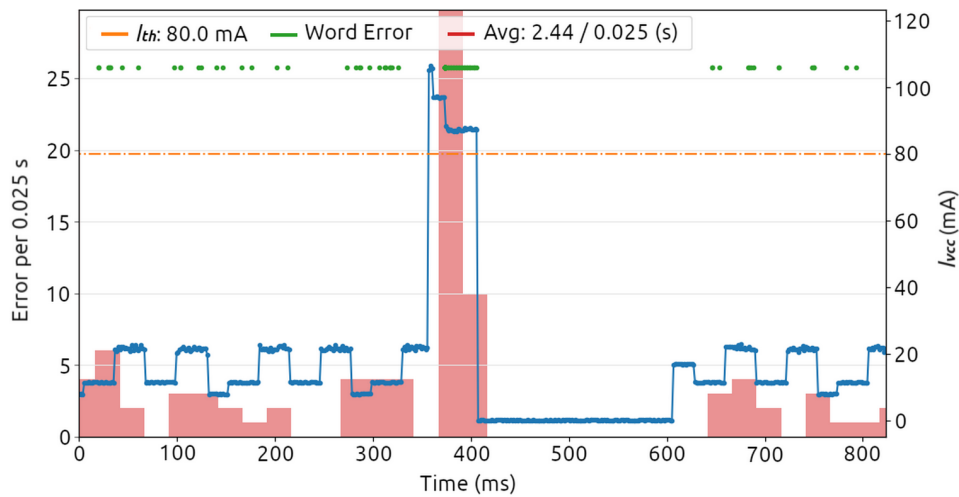


Fig. 7. Test run for March C- during heavy ion irradiation showing the bit upset histogram and the DUT current consumption superposed with synchronized timestamps.

To further investigate this behavior, we performed an additional analysis, in which errors during and outside SEL events were highlighted to allow further classification. Figure 8 presents an example for this analysis using a heavy-ion test run in dynamic mode. It uses the timestamped bit error results to plot them in a logical bitmap representation. The logical bitmap is a two-dimensional plot of the memory indexing contiguous data addresses following rows, columns, and arrays logical mapping. It is possible to observe that, during SEL events, not only error accumulation is observed, but also larger patterns (column block errors) are formed. This behavior is important to take into consideration since block errors are capable of surpassing mitigation schemes, such as common Error Correcting Codes (ECC). In this context, based on their characteristics and occurrence (95% of test runs), we classified the accumulated column block errors during SELs as SEFI events and the isolated upsets (mainly outside the SELs) as SEU events. Therefore, the SEL not only changes the memory's current behavior but also triggers SEFIs with more potential impact on the execution than most SEUs.

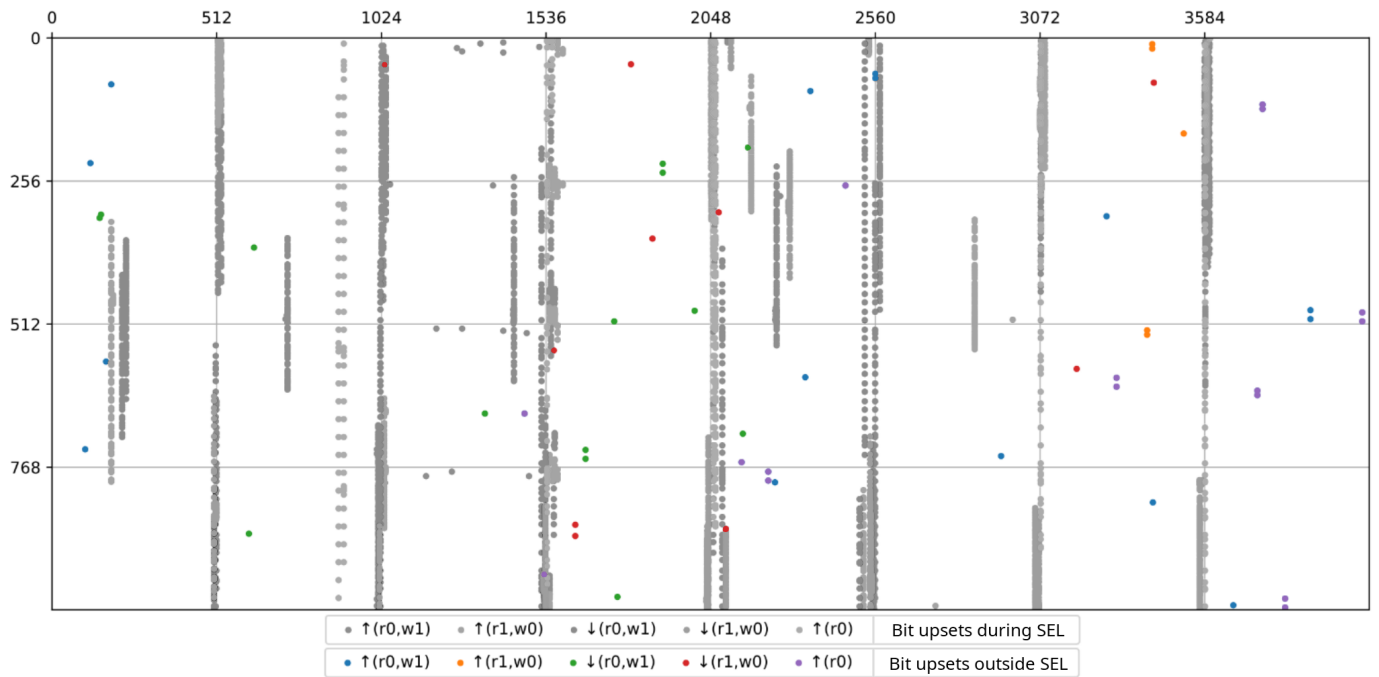


Fig. 8. Logical bitmap of the memory address space with the identified bit upsets during a March C- run with a LET of $48.5 \text{ MeV.cm}^2/\text{mg}$. The x and y axis represent addresses in an arrangement based on the logical memory organization with arrays, rows, and columns, as specified on the datasheet [12]. For this bitmap, bit upsets during and outside SEL events were highlighted.

D. SEFI classification

The logical bitmap that is shown in Figure 9 enables another type of analysis that was possible with the proposed instrumentation. It uses the timestamped bit error results to plot them in a logical bitmap representation. This information is displayed in real time on the host computer, allowing the operators to easily be aware of the DUT behavior and follow the experiment progression. In this figure, we show an example of the reported errors during distinct SEL events. We selected this run because the three main observed SEFI show the following behavior: 1. lines in the edges of the bitmap; 2. lines errors in central regions; and 3. sparse error clusters, forming lines, in four distinct regions. This result supports the analysis of the ECC capabilities to correct the SEFIs since, despite being a robust hardening strategy, it has limitations with error accumulation. With access to the memory's physical bitmap, it would be possible to further investigate, classify, and correlate error types with the observed error location and current behavior. It is worth noting that for this memory device, the observed SEFIs are intuitively observed as block errors and correlated with SELs, but for other systems, the observed SEFIs can be difficult to classify or distinguish their source. Thus, as proposed, with precise and synchronized current monitoring, it is possible to identify current signatures for each SEFI type, supporting their classification.

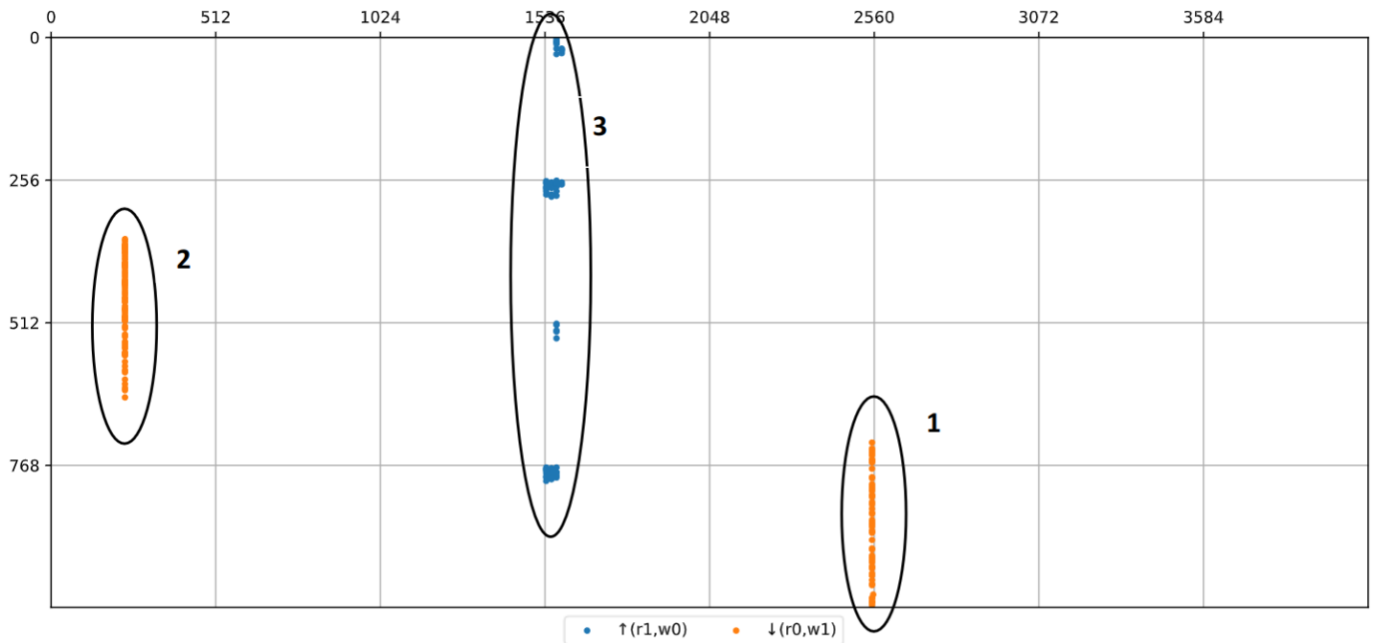


Fig. 9. Logical bitmap of the memory address space with the identified SEFIs during distinct SELs. The x and y axis represent addresses in an arrangement based on the logical memory organization with arrays, rows, and columns, as specified on the datasheet [12]. For this bitmap, isolated SEUs were hidden to allow better visualization of the clusters.

V. DISCUSSION

We introduced an experimental instrumentation based on widely available COTS components for in-depth monitoring of SEEs in electronic systems. Through the exploration of a case study (SRAM memory), we presented the main characteristics of the proposed approach, discussed the obtained results, and provided examples exploiting the instrumentation capabilities. As discussed, traditional SEL monitoring solutions for memories often just count overcurrent events and rarely report the correlation with other types of events. In particular, coherent timestamping is another missing capability, reducing the opportunities for in-depth analysis. Even if different test modes are employed, many setups perform the current monitoring with external circuitry, lacking the correlation between events and current spikes. The proposed instrumentation provided a solution for these limitations, enabling enhanced analysis of the observed effects. Notably, when compared to traditional or simplified approaches, some important conclusions for this study would not be possible, such as the correlation between SELs and SEFIs (error accumulation), which required precise time synchronization. This information was necessary to support the understanding of the flight behavior of the studied SRAM memories, as reported in prior work [14].

Besides that, the proposed instrumentation has an adequate resolution on the individual SEL events with more precise current logging with high-frequency sampling and clustering capabilities. The usage of fine-grain measurements highly improves the investigation of the observed events, providing details of the induced errors using information about their current signatures and faulty behavior. The instrumentation also allowed characterizing other SEE cross sections, which improves the overall knowledge about the memory's response to radiation effects. Table II summarizes the performance and functional parameters of the developed instrumentation.

It is worth mentioning that this instrumentation is not limited to SRAM memories since it can be used for other memory types. Only a few adaptations are required, such as addressing size, pin assignments, and specific protocols. In some cases, even the same test board could be used since the memories are often built with similar chip packages and pinouts. Since the proposed instrumentation is based on an FPGA, it has a very flexible pin assignment that supports easy integration with other memory types. Furthermore, as discussed in Section IV with a few examples, the strategy presented in this work can be extended to

TABLE II
SUMMARY OF FUNCTIONAL PARAMETERS OF THE INSTRUMENTATION.

Parameters	Value	Observations
Current resolution	25 μA	-
Threshold current	up to 725mA	Configurable in real-time
Timing resolution	80ns	Current and memory errors synchronization
Current conversion	140 μs	Analog to digital conversion
Current sampling	220 μs	-
Response time ¹	1.1ms to 1.25ms	From high current to SEL detection
Test modes	-	Standby, chip-enabled, static, and dynamic ²
Power monitoring	-	Main supply and IO banks monitored

¹ Considering five current samples for filtering, ² March C- and Dynamic Stress.

other device types and more complex systems, such as microprocessors, FPGAs, and systems-on-chip. To achieve that, the test engine and error reporting should accommodate other types of tests (e.g., benchmark output checking). With this type of SEE monitoring with enhanced synchronization, it is possible to identify the current signatures of the tested device for a broad range of workloads and operational modes. Using this information, researchers can compile a dictionary with current signatures correlating operational states and SEL response that could provide more capabilities for predicting systems behavior under the target radiation environments.

VI. CONCLUSIONS

We proposed experimental instrumentation for SEE monitoring aiming to achieve in-depth analysis by enhancing the observability and synchronization of distinct types of measurements. For that, we discussed the adopted methodology and practical aspects beyond the available radiation testing strategies in the literature. The limitations and opportunities of our approach were discussed. We also presented further perspectives on the improvement and extension of the instrumentation for complex devices and systems. After carrying out two experimental campaigns in irradiation facilities, we validated our proposal and presented the main positive outcomes of using this approach in comparison with more traditional strategies. Notably, the solution provides enhanced synchronization, high sampling rate, fast response time, detailed resolution, and flexibility. Therefore, as part of this study, we were not only able to further investigate the SRAM memories used on-board the PROBA-V satellite and provide insights about their flight behavior and SEL sensitivity, but also propose robust instrumentation for SEE monitoring of general electronic systems.

In future work, integrating temperature control capabilities into the system will allow the exploration of other temperature ranges that can significantly affect the SEL response of the devices. Besides that, a feature that might support the experiment execution is a flexible interface ready for integration with the facility's beam shutter control, enabling fine timing adjustments, such as SEL events isolation. Finally, we also observed some behaviors that can be worthy of further investigation by using the proposed instrumentation (e.g., through a laser test campaign).

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