Comparison of Modular Multilevel Converter and Neutral Point Clamped Converter Topologies for MVDC applications

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Keywords

«AC-DC converter», «Medium voltage converter», «Modular Multilevel Converter (MMC)», «Power transmission», «3-Level NPC ».

Abstract

The utility grid is experiencing a shift from a top-down architecture to a decentralized system with a hybrid AC and DC network. This includes MVDC networks. The AC-DC power converter is a key technology for this transition. This article presents a comparison between the 3-Level NPC and MMC topologies in terms of size, power losses and DC fault response for MVDC networks. It was found that the 3L-NPC has lower costs related to semiconductor devices. In terms of efficiency, the MMC converter has a better performance, namely thanks to its reduced switching losses. Regarding passive elements, both topologies seem to be comparable. Finally, the MMC offers more flexibility in DC fault handling, namely thanks to the use of bypass thyristor.

Introduction

In order to achieve the net zero CO_2 emissions goal by 2050, the massive deployment of renewable energy sources (RES) is required [1]. The current utility grid will change from a top-down architecture to a decentralized system with small-scale distributed power generators. A possible pathway for the future distribution networks is to have a hybrid AC and DC network, where the DC network comes to support the AC network and helps maximizing its capacity [2]. Medium voltage DC (MVDC) point-to-point links [3] and networks [4] may play an important role in the future grids and represent a feasible solution that could allow the integration of large shares of RES and electric vehicles. A key technology for the deployment of MVDC systems is the AC-DC power converter that interfaces the AC and DC networks. The choice of the appropriate AC-DC converter must be done for different voltages found in the MVDC range, from 1.5 kV to ±100 kV [5].

The high controllability of voltage source converters (VSC) and their ability to operate on weak AC systems suggest that VSCs are the most likely to be used in MVDC systems. The two-level inverter (2LI) and the neutral point clamped (NPC) are good candidates [6]. The modular multilevel converter (MMC) has revolutionised the HVDC market since its invention in 2003 [7] and it remains valid for MVDC. The cascaded H-bridge (CHB) [8] and other cascaded converters [3], [9] or flying capacitor (FC) [10] can be considered too.

Given all the possible topologies to be used in MVDC, there is a need to determine which topologies are best suited for specific applications and what advantages they present over other topologies. This need has been previously identified and addressed in different works. In [11] a rapid assessment method for modular converter topologies for HVDC was presented. The methodology includes the definition of the operating point, the degrees of freedom and proposes a series of key performance indicators (KPIs) to be used when comparing or evaluating converter topologies.

At medium voltage range there is an interest in researching and comparing different types of multilevel converters for high-power motor

drives. A comparison between the MMC and CHB was presented in [12] for three voltage levels (4.16, 6.9 and 13.8 kV) and three power levels (1, 3 and 5 MVA). A similar comparison was done in [13] between the MMC, the CHB and the 5-level active NPC (5L-ANPC) converter. For this latter study three different semiconductor ratings were used and the assessment was done for three voltage levels (4.16, 6.9 and 13.8 kV) and two power levels (3 and 5 MVA). The comparisons were made in terms of efficiency, number of components, capacitance requirements and total volume.

Similarly, there is an increasing interest in comparing converter topologies for grid connected applications. In [14] the authors compared the MMC and the NPC topologies for a battery energy storage system (BESS) of 5 MVA connected to the 10 kV distribution network. The 3L-NPC and four MMC variants with different semiconductor devices were compared in terms of operation performance, component losses, harmonic content and cost.

A further study comparing the MMC, 3L-NPC and cascaded 3L-NPC (C3L-NPC) was done in [15] considering not only the efficiency, but also the reliability and long term investment indicators such as the return on investment (ROI) based on redundancy and maintenance considerations for a voltage range from ±10 kV to ±50 kV. Another comparison between MMC and 3L-NPC was presented in [16] in a range of voltages between ±6 kV and ±100 kV using as KPIs the semiconductor utilisation, efficiency, harmonic content and size of the converter.

Another topic of great importance in MVDC multi-terminal networks is the AC-DC converter response to a DC short circuit. This is because in such networks, the design of a DC protection device (circuit breaker, fuse or other) must be coordinated with the design of the converter. The protection strategy of a radial MVDC network was discussed in [17]. A review of technologies for MVDC circuit breakers (CBs) was presented in [2], [18]. In [2] a classification was proposed including: mechanical CB, solid state CB and hybrid CB. The mechanical CB is the most cost effective but it typically operates in tens of milliseconds or more [19]. The AC-DC converter must withstand the short-circuit current until the CB clears the fault. To the best knowledge of the authors, the current state of the art does not deal with DC faults when comparing AC-DC converter topologies.

This article presents the comparison of the most prominent AC-DC converter topologies for MVDC networks, namely 3L-NPC and MMC. The proposed methodology evaluates several KPIs and it takes into account AC and DC network requirements. The novelty resides in a comparison done for grid applications for several voltage and power ratings and the assessment of the DC fault response of both topologies.

This article is organised as follows. First, the methodology of AC-DC converter assessment is introduced. Second, the key converter design equations are recalled and a case study is defined. Third, the NPC and MMC DC fault response is presented and discussed. Finally, the KPIs of both topologies are summarised.

Methodology of converter topology assessment

A general methodology used for the assessment and comparison of AC-DC converters was proposed in [16]. It allows to do a fast evaluation of a converter topology for a specific application. It can be used to assess innovative topologies or to compare different solutions.

The methodology is detailed in Fig. 1. The first step is to define the applicable requirements that the design must comply with. Then, considering the state of the art, different converter topologies are selected for the assessment. Afterwards, the operating points of the converter are identified depending on the application. The design is done for the nominal point or for other operating points considered to

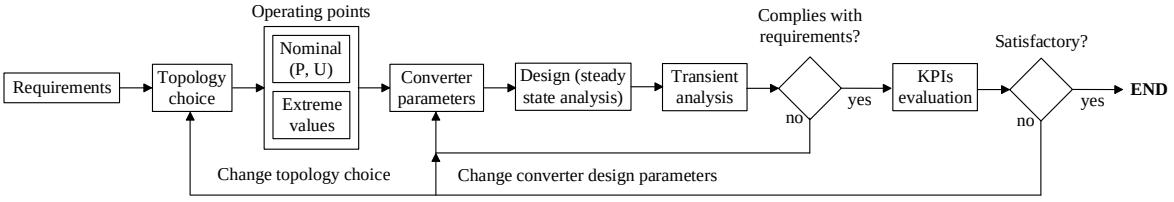

Fig. 1. Methodology for the design and evaluation of AC-DC converters. Adapted from [16]

be the worst-case or critical ones. There are some degrees of freedom for the design, like the semiconductors rating for example.

With all the inputs needed to do the design, a steady state analysis of the converter is performed. This allows to calculate the values of currents and voltages, as well as the different design parameters such as the total number of semiconductor devices and the values of the passive elements. Several designs are obtained as a result of considering different values of the degrees of freedom (converter parameters) or different operating points. The most convenient design is selected.

The transient analysis step ensures the compliance with some of the grid requirements, like the THD or response to faults. If the design does not comply with the requirements, an iterative process is done, changing the design or varying the converter parameters.

The calculation of the KPIs is done for different topologies and design variations. The process is over once the obtained KPIs are satisfactory. The choice of the KPIs depends on the application and the interest of the designer. The relevant KPIs considered in this article are:

- Number of semiconductor devices,
- Total blocking voltage,
- Semiconductor oversizing factor,
- Electric energy factor (capacitors),
- Magnetic energy factor (inductors),
- Conduction losses factor,
- Switching losses factor,
- Diode i^2t at 10 ms.

For all the listed KPIs, it is considered that the lowest value is the best one.

Number of semiconductor devices

The number of semiconductor devices is a good indicator of the cost of the converter without making a detailed cost breakdown. For an MMC, the number of submodules (SMs) per arm is given by (1). For this topology, each arm must be able to withstand the entire DC voltage V_{dc}. Knowing that only half-bridge submodules (HBSMs) are considered here, it is easy to compute the total number of devices needed per arm $N_{SM,arm}$ with the SM average voltage V_{SM}. For the NPC converter, each valve (series connection of semiconductor devices) must be able to withstand half of the DC voltage V_{dc}, as shown in equation (2), where $N_{sw,series}$ is the number of devices in series per valve and V_{sw} is the device derated voltage (typically around 50% of the semiconductor voltage rating).

$$N_{SM,arm} = ceil\left\{\frac{V_{dc}}{V_{SM}}\right\} \quad (1)$$

$$N_{sw,series} = ceil\left\{\frac{V_{dc}}{2V_{sw}}\right\} \quad (2)$$

Total blocking voltage

The total blocking voltage TBV is defined as the sum of the maximum blocking voltage of each individual semiconductor device. For IGBT modules it can be found in the datasheet as collector-emitter voltage V_{CES}. This KPI gives a similar information to the number of semiconductor devices, but expressed in Volts.

$$TBV = \sum_{i=1}^{N_{switches}} V_{CES,i} \quad (3)$$

Semiconductor oversizing factor

The semiconductor oversizing factor O_{sw} is useful to know how much the installed semiconductor devices are actually being used. It is represented by VA_{RMS}, the RMS current multiplied by the semiconductor's blocking voltage. With this, it is possible to know how oversized the converter is, computing the ratio between the total used semiconductor power VA, and the nominal converter power P_{DC}.

$$O_{sw} = \frac{\sum_{i=1}^{N_{switches}} VA_{RMS,i}}{P_{DC}} \quad (4)$$

Electric energy factor

This factor is an indicator of the size of the capacitors in the converter. Indeed, their size is related to the energy that they can store. The energy factor E is the ratio between the total energy that can be stored in all the converter capacitors W_{cap} and the nominal converter power P_{DC}.

$$E = \frac{\sum_{i=1}^{N_{cap}} W_{cap,i}}{P_{DC}} \quad (5)$$

Magnetic energy factor

Equivalent to the electric energy factor for capacitors, the magnetic energy factor indicates the size of the inductors. For inductors with an air core, the size is directly related to the apparent power. The magnetic factor k_{ind} is the

ratio between the apparent power S_{ind} and the nominal converter power P_{DC}.

$$k_{ind} = \frac{\sum S_{ind}}{P_{DC}} \quad (6)$$

Power losses factor

The power losses factor represents the percentage of losses in a converter with respect to the transmitted power P_{DC}. In this work only the semiconductor losses are considered since they are predominant. They are divided into conduction P_{cond} and switching losses P_{sw}. The losses calculation is detailed in [16], [20] and the respective losses factors P_c and P_s [21] are presented in equations (7) and (8).

$$P_c = \frac{\sum P_{cond}}{P_{DC}} \quad (7)$$

$$P_s = \frac{\sum P_{sw}}{P_{DC}} \quad (8)$$

i^2t at 10 ms

The fault current integral or i^2t of a semiconductor device is an important parameter related to its thermal limitation. If the maximum i^2t is exceeded, the semiconductor device could be damaged. This KPI is related to the behaviour of a converter in case of a short circuit. Since a DC pole-to-pole fault results in the highest fault current for the converter, it is important to determine the i^2t for this type of fault to make sure the limit is not reached. Here, it is proposed to consider the i^2t value 10 ms after a pole-to-pole fault. 10 ms is chosen for being the current neutralization time [22] including the action of the protection relay and the DCCB [23], [24]. The i^2t is found for all the devices of the converters and the worst (highest) value is chosen.

Converter design and case study

The MVDC system studied in this article is composed of an AC grid, a transformer, an AC-DC converter and a DC network, as shown in Fig. 2. The AC-DC converter is either an MMC as shown in Fig. 3, or an NPC converter including AC and DC filters, as shown in Fig. 4. The system parameters are shown in Table I.

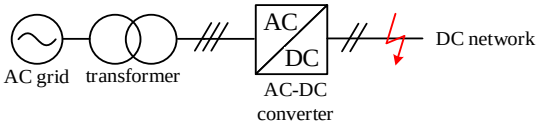

Fig. 2. MVDC system analysed for the case study

Table I: System parameters

AC grid voltage [kV]	225
Short circuit power [MVA]	3126
Xtr [%]	15

There are several possible voltage levels to build MVDC systems [25]. The nominal currents are defined according to MVAC switchgear (630 A) and HVDC converter (1500 A) typical values. The selected voltage and current levels for this case study are shown in Table II. Two voltage levels, representative of the higher and lower voltage range, are highlighted.

Table II: Voltage and current levels of the case study

DC voltage [kV]	DC current [A]
±6	630 1500
±10	
±20	
±35	
±50	
±100	

For each voltage and current combination presented in Table II, a design is done for both converter topologies, resulting in 12 different designs for each one. IGBT modules and clamping diodes of 3.3 kV and 1800 A were considered for all the cases [26].

The considered MMC is a three-phase converter, with HBSMs, as shown in Fig. 3.

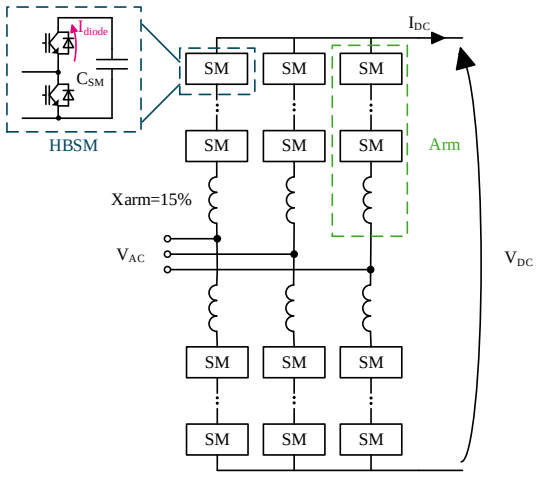

Fig. 3. Modular multilevel converter topology

The arm reactance for the MMC X_{arm} was taken as 15% of the base converter impedance, this being a common practice in HVDC [27].

$$X_{arm} = 0.15\, Z_{base} = 0.15 \frac{V_{ac}^2}{S_{nom}} \quad (9)$$

The submodule capacitance C_{SM} was calculated considering the energy variation in the capacitor ΔW [28], as shown in (10), where V_{SM} is the average submodule voltage (taken as the semidonductor derated voltage), $N_{SM,arm}$ the number of submodules per arm and ε the voltage ripple, assumed to be 10%.

$$C_{SM} = \frac{\Delta W}{2\varepsilon N_{SM,arm} V_{SM}^2} \quad (10)$$

The energy swing is calculated as shown in (11) [28], where V_{dc} and I_{dc} are the DC voltage and current, respectively, f is the operating frequency of the converter (50 Hz), $cos\varphi$ is the power factor and k is the ratio between the AC and DC voltages V_{ac} and V_{dc}.

$$\Delta W = \frac{V_{dc} I_{dc}}{2\pi f} \left(1 - \frac{1}{\left(\frac{2}{k\, cos\varphi} \right)^2} \right)^{\frac{3}{2}} \frac{4}{cos\varphi} \quad (11)$$

The modulation considered for the MMC is a PWM with a switching frequency of 175 Hz.

The NPC converter is a three-level converter as shown in Fig. 4. A PWM modulation is used with a switching frequency of 650 Hz. The AC filter L_{AC} was chosen to be 0.15 p.u. verifying that the harmonic content was not over the established limit of 8% for THD [29] and the DC filter was added to limit the current increase during a fault in the DC network. L_{DC} was changed in linear proportion to the power. For the case ±10 kV and 630 A the chosen value was 1 mH.

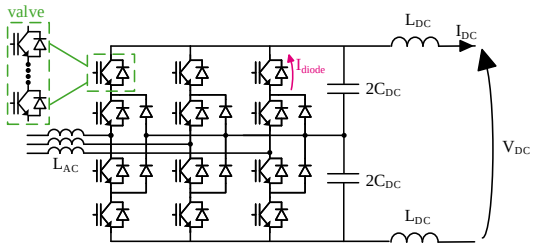

Fig. 4. Three-level neutral point clamped converter with AC and DC filters

The DC capacitors were sized using (12) and (13), where S_{VSC} is the nominal power of the converter in MVA, ω is the electrical frequency V_{DC} is the DC voltage, ΔV_{DC} is the voltage ripple [27], in this study assumed to be 10% maximum and τ is the time constant of DC capacitor charging, selected as 10 ms. These two equations allow to comply with the ripple specification and the control bandwidth requirements.

$$C_{DC} > \frac{S_{VSC}}{2\omega V_{dc} \Delta V_{dc}} \quad (12)$$

$$C_{DC} < \frac{2\tau S_{VSC}}{V_{dc}^2} \quad (13)$$

DC fault response

The fault is assumed at the converter DC terminals (see Fig. 2) with a fault resistance of 14 mΩ. This is the worst-case scenario considering the converter fault current withstand. The results shown in here correspond to the case ±10 kV, 630 A, but the general trends were found to remain the same for all the cases. Shortly after a DC fault, the converters are blocked, behaving like uncontrolled rectifiers. Fig. 5 shows the voltage between the DC terminals. As it can be seen, before the fault the DC voltage for both converters is the nominal voltage 1 p.u. or 20 kV (±10 kV). After the fault, the DC voltage oscillates before it stabilizes. For the MMC, the oscillations are more prominent and the steady state DC voltage after the fault is around zero. The NPC reaches the steady state much faster.

Fig. 6 shows the DC current. Before the fault, the DC current for both topologies is 630 A, the nominal current. After the fault, there is a peak before the current stabilizes in its steady state value. For the NPC topology, the high peak is caused by the discharge of the DC link capacitors into the fault, reaching around 12 kA. From there the current slowly decays before reaching steady state. The MMC current on the other hand has a much lower peak because the converter blocking avoids the discharge of the SM capacitors into the fault. It is observed however, that the MMC has a higher steady state current than the NPC. This was found to be the case for all the considered voltage and power levels above ±6 kV. This is because the equivalent AC inductance of the NPC is twice as big as that of the MMC (15% vs. 7.5%) which results in a lower steady state current for the NPC. Had the equivalent AC inductance been the same for both topologies, the same steady state current value would be observed.

Fig. 7 shows a zoom of the DC current 50 ms after the fault as well as the maximum diode current of the converter. It can be seen that the DC current has a much steeper slope for the

NPC than for the MMC, due to the DC capacitor discharge into the fault. The diode current for the NPC rises with a steep slope, but not immediately after the fault, since the current does not flow through the diodes until after the capacitor is totally discharged into the fault. This is not the case for the MMC, for which the diode current increases immediately after the fault.

Fig. 8 shows the maximum diode currents and their respective i^2t values for both topologies. The i^2t value 10 ms after the fault is slightly higher for the NPC (0.24 vs 0.19 MA^2s). The typical maximum value of i^2t for the semiconductors of the selected rating is around 0.5 MA^2s.

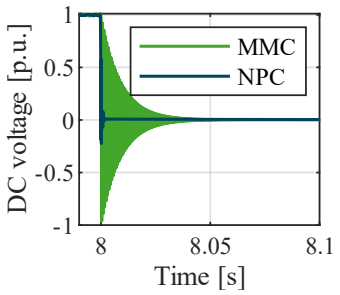

Fig. 5. DC voltage after a pole-to-pole fault for the case ±10 kV, 630 A

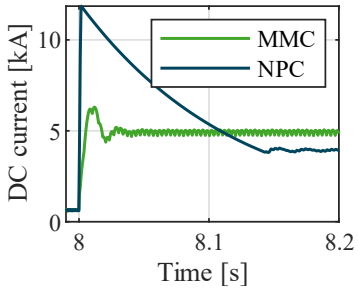

Fig. 6. DC current after a pole-to-pole fault for the case ±10 kV, 630 A

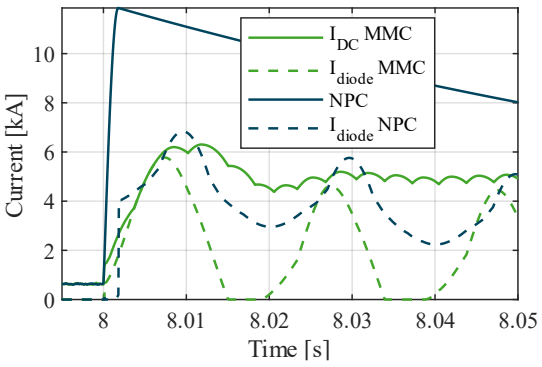

Fig. 7. DC and max diode currents after a pole-to-pole fault for the case ±10 kV, 630 A

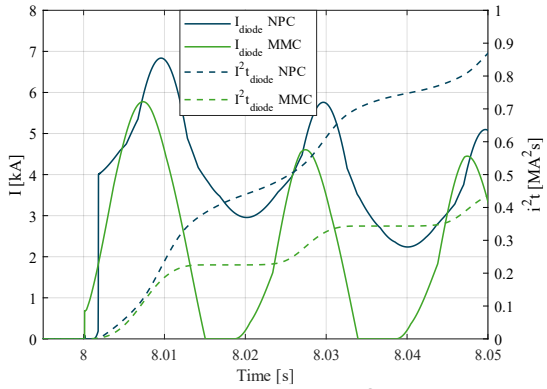

Fig. 8. Max diode current and i^2t values for the case ±10 kV, 630 A

The i^2t value 10 ms after the fault was found to increase with the voltage and with the power for the MMC converter as shown in Fig. 9. For the NPC converter, the i^2t value seems to decrease with the different voltage levels, but it is always higher for the higher nominal current. For the case with nominal current of 630 A, both topologies have very similar values, while for the case with nominal current 1500 A, the MMC has an i^2t well above that of the NPC.

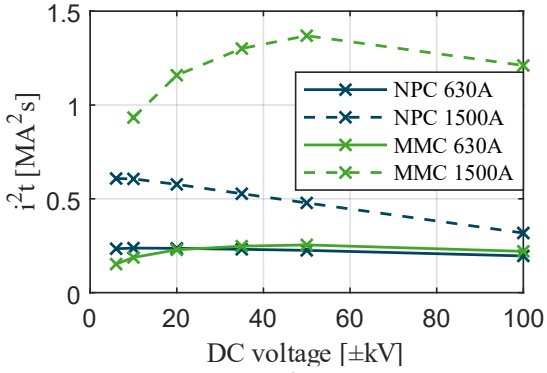

Fig. 9. Evolution of the i^2t 10 ms after the fault as a function of the DC voltage and current

It is important to mention that the value of the i^2t and the DC fault current greatly depend on the values of the AC and DC filters of the NPC. Given that the DC filter limits the peak fault current, it would be possible to reduce the peak for all the cases by increasing L_{DC}. Nevertheless, it is important to consider that as a general practice, a protection thyristor is added in the HBSM of the MMC. These devices have a much higher i^2t than the diodes of the converter, making the protection of the converter relatively straightforward in the case of a pole-to-pole fault. The addition of these devices is not an easy solution for the NPC.

Assessment of converter topologies

In this section, the KPI values are presented for the voltage levels ±10 kV and ±100 kV and for both nominal currents. The results are presented in Fig. 10, Fig. 11, Fig. 12 and Fig. 13. The preferred values are towards the inside of the chart.

As a first KPI, the number of semiconductor devices is shown, it is divided into switches (IGBT and its antiparallel diode) and clamping diodes, which will only be present in the NPC topology. The total number of semiconductor devices (as well as the total blocking voltage) is always greater for the MMC than for the NPC, suggesting that the latter topology is preferrable. It can also be observed that the semiconductor oversizing factor is smaller for the NPC, meaning that for this topology less installed semiconductor power is required than for the MMC, for the same nominal DC power. Moving on to the electric and magnetic energy factors, it can be seen that the electric energy factor is smaller for the NPC. The magnetic factor seems to be always better for the MMC converter.

Regarding the converter efficiency there does not seem to be a noticeable difference between both topologies in the conduction losses. On the other hand, there is an important difference in the switching losses factor of both topologies. Indeed, the losses for the NPC are much higher than for the MMC. This is due in part to the higher switching frequency (650 Hz vs 175 Hz). Additionally, the losses were computed with the converters working in rectifier mode. In this mode, the NPC converter exhibits higher losses than in inverter mode, as the current paths are different and the current flows more through the diodes. Considering the total losses, the MMC would be the most advantageous topology.

Finally, concerning the behaviour of the system in case of a DC short circuit, it was previously discussed that for 630 A both topologies have very close i^2t values while for 1500 A, the MMC presents higher values than the NPC. Although the NPC values could be improved by increasing L_{DC}, protective thyristors can be used for the MMC topology. Therefore, there is no clear conclusion on which topology would be better for this KPI.

Fig. 10 to Fig. 13 show that the KPI trends remained the same for all voltage and power ratings. A possible reason for this, is that the sizing strategy was kept the same for all the voltage and power levels.

The synthesis is presented in Table III.

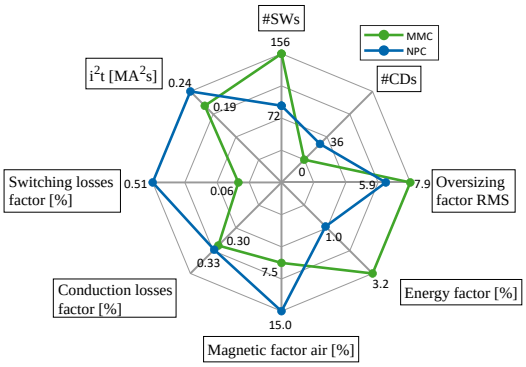

Fig. 10. KPIs for ±10 kV, 630 A

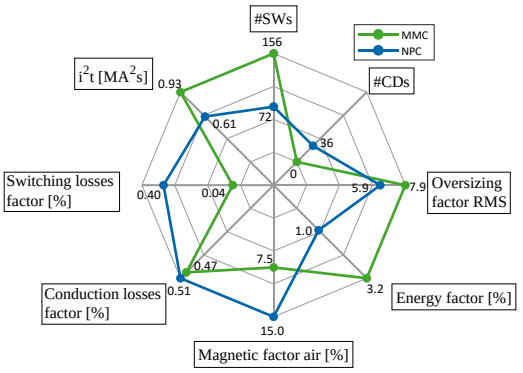

Fig. 11. KPIs for ±10 kV, 1500 A

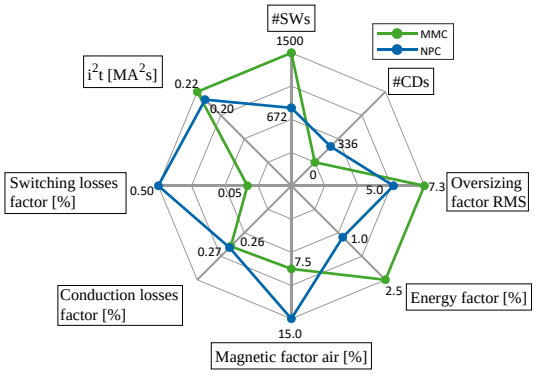

Fig. 12. KPIs for ±100 kV, 630 A

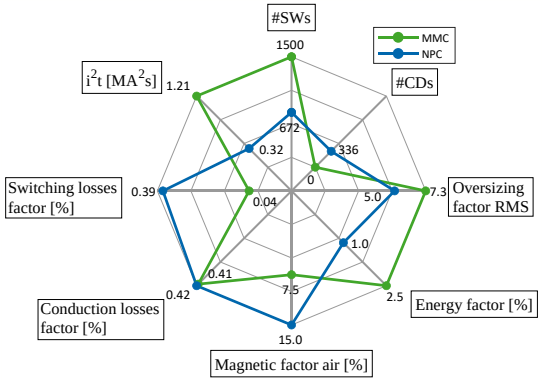

Fig. 13. KPIs for ±100 kV, 1500 A

Table III: Synthesis of assessment: + for better, - for worse and = for similar (*MMC including bypass thyristor)

	NPC	MMC
Cost of semiconductors	++	−−
Size of capacitors	+	−
Size of inductors	−	+
Efficiency	−	+
DC fault withstand	=	= ++*

Conclusion

A methodology for the design and assessment of AC-DC converters was followed to perform the design and comparison of the 3L-NPC and MMC converter topologies for MVDC applications. Twelve different cases were studied to consider the entire MVDC voltage range, including six voltage and two current levels. It was found that the NPC has less semiconductor devices and a better semiconductor utilization than the MMC. Regarding the size of the converter related to the use of passive components, it is unclear which topology is better, as the NPC has a smaller electric energy factor for the capacitors, but the MMC has a smaller magnetic energy factor for the inductors.

In terms of losses the MMC has a much better performance with switching losses significantly lower than those of the NPC. Finally, for the i^2t, there is no noticeable difference between both topologies with a nominal current of 630 A, while for 1500 A the NPC presents smaller values, appearing to be better. This should however not be taken as a final conclusion, considering this KPI could be further improved for both topologies through L_{DC} and L_{arm} sizing and protective thyristors.

Further analysis could be done to make an even more complete comparison, for instance assessing the reliability of these topologies, checking how the KPIs would change with a varying load profile and considering the technological limitation of the series connection of switches.

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