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Defect Engineering for Enhanced Silicon Radiofrequency Substrates

Martin Perrosé,* Yoann Baron, Baptiste Lefaucher, Pablo Acosta Alba,*
and Jean-Pierre Raskin

Herein, high-resistivity silicon substrates with specific He⁺ ion implantations to mitigate the parasitic surface conduction effect are studied. Several postimplantation thermal annealing conditions are investigated. Substrate performance is assessed at radiofrequencies (RFs) using the small-signal characterization of coplanar waveguides (CPW) structures. The best effective resistivity (ρ_{eff}) of 4 k Ω cm is achieved with the wafer annealed at 600 °C for 2 h. This ρ_{eff} value is also stable as a function of DC bias applied to the CPWs. Those high RF performances originate from the nature of the defects created by ion implantation. Defects are deeply analyzed using spectroscopy measurement and scanning transmission electron microscopy. Combining these measurements, it is shown that {311} defects are probably responsible for the achieved high RF performances. Finally, the link between charge carriers trapping in the RF domain and defects nature is discussed to develop a defects engineering strategy for low-loss RF substrates. The proposed fabrication method enables the fabrication of RF passivation layer locally over the wafer, and thus the cointegration of RF devices with fully depleted silicon-on-insulator technology.

their high performance, the preservation of RF signals integrity is essential. Nevertheless, modern telecommunication technologies involve wide very-high frequency bands, which face several challenges in terms of signal quality and integrity. Actually, RF devices must show extremely low losses and very-high linearity.^[2] Choosing the right substrate is of capital importance to fabricate high-performance circuits. In the last decade, silicon-on-insulator (SOI) substrates were introduced to increase the electrical performance of advanced complementary metal oxide semiconductor (CMOS) devices.^[3] To make SOI substrates compatible with RF technologies requirements, high-resistivity (HR) silicon-based wafers were introduced.^[4] However, HR-SOI substrates suffer from positive fixed charges at the SiO₂/Si interface, creating a so-called parasitic surface conduction (PSC) layer.^[5] This

1. Introduction


Nowadays, modern wireless telecommunication standards enable impressive data transfer rates.^[1] These technologies are based on the use of radiofrequency (RF) signals. To conserve

PSC layer makes SOI substrates not suitable for RF applications. In this context, the introduction of a trap-rich (TR) layer beneath the buried oxide (BOX) is proposed to avoid the formation of the PSC and thus conserve the high resistivity properties of the SOI substrate that guarantee low losses and high linearity to the RF-integrated functionalities.^[5] To go further, the cointegration of RF devices with CMOS devices using a fully depleted-SOI (FD-SOI) technology on a single wafer is explored. Nevertheless, the current TR layer standard fabrication consists of a thick undoped polycrystalline silicon (Poly-Si) deposition, making it not compatible with FD-SOI CMOS integration.^[3] One of the main current paths toward cointegration is to locally fabricate TR layers beneath RF devices. Therefore, several solutions to achieve TR layers compatible with FD-SOI features were recently proposed such as PN junctions,^[6] local Poly-Si fabrication,^[7] or local deep-level impurities passivation.^[8] All these solutions can be locally done as they are all based on ion implantation. Indeed, ion implantation combined with photolithography can be performed on a selected region of a substrate. PN junction passivation is based on the fabrication of P- and N-doped regions beneath the oxide. The formed PN junctions locally increase the resistivity, thus improving RF performance.^[6] The local Poly-Si fabrication is based on the use of an amorphizing ion implantation followed by a nanosecond laser annealing, two processes that can be done locally, this approach also leads to better RF performance.^[7] The deep-level impurities passivation is

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mainly achieved using ion implantation of metallic impurities, followed by a thermal treatment to place them in substitutional sites, leading to the formation of deep charge carriers traps. It should be noted that as local TR layer mainly benefits to RF passive devices, the lateral variability of the ion implantation can be neglected compared to the average size of RF passive components (e.g., several microns to several millimeters for antennas). Thus, the precise control of the lateral dispersion of local ion implantation is not a major issue. Nevertheless, these solutions suffered from several limitations in terms of costs (double implantation and photolithography for PN junctions, use of nanosecond laser annealing for local Poly-Si fabrication, use of Au ions for local deep level passivation) or performance (frequency roll-off for PN junctions, bias dependency for local deep level impurities passivation). In this work, we show that a combination of ions implantation (He) and low-temperature annealing (at 600 °C for 2 h) constitutes a promising approach to locally fabricate TR layers.

Indeed, this process creates crystalline defects that are efficient for charge carriers trapping, leading to high-quality integrated RF functionalities. Therefore, we propose to assess the crystalline defects enabling the efficient charge carriers trapping in the RF domain in such a substrate. To that end, defects responsible for the radiative recombination of charge carriers are identified using photoluminescence (PL), and their morphology is investigated by scanning transmission electron microscopy (STEM).

2. Experimental Results

2.1. Samples Fabrication

Samples are fabricated from 200 mm-diameter p-type HR Si substrates with nominal resistivities between 3 and 8 kΩ cm. A 200 nm-thick oxide (SiO₂) layer is formed by thermal oxidation at 900 °C in a dry atmosphere. Two He⁺ implantations are sequentially performed, the first one at an energy of 45 keV and a dose of 3×10^{16} at cm⁻², the second one at an energy of 17 keV and a dose of 9×10^{16} at cm⁻². Then, samples are annealed in a TEMPRESS vertical furnace (convection heating) for 2 h at various temperatures (400, 600, 800, 900, and 1100 °C) in a N₂ atmosphere. The used annealing temperature ramp is 10 °C per minute and the samples have been put into the furnace

at 200 °C. As a reference, a wafer is similarly implanted but not subsequently annealed. To perform RF characterization, coplanar waveguides (CPW) are fabricated on top of all samples. To do that, a plasma-enhanced chemical vapor deposition of a 200 nm-thick TEOS layer is performed at 260 °C. Then, 100 nm-thick Ti (as an adhesion layer) and 1 μm-thick Au layers are deposited and patterned to define CPW lines which have a central signal line width of 70 μm, a gap between signal line and planar grounds of 42 μm, and a ground width of 316 μm and lengths of 1.5 or 0.5 mm. The fabricated CPW structures are shown in **Figure 1**.

2.2. RF Performance

First, the RF performances of He-implanted silicon substrates are analyzed using standard RF figures of merit. The effective resistivity (ρ_{eff}) is an RF figure of merit commonly used to assess signal losses related to the substrate.^[9] To extract ρ_{eff} , a small-signal RF characterization is performed using a PNA-X Vector Network Analyzer together with ground signal ground probes. The detailed way to experimentally extract ρ_{eff} is mentioned in ref. [10]. To benchmark the RF performances of our samples, their ρ_{eff} are extracted as a function of the DC bias applied to the central line of CPW lines (**Figure 2**).

The nonannealed reference wafer and the one annealed at 400 °C present ρ_{eff} values of 1.7 and 1 kΩ cm, respectively. Usually, a ρ_{eff} versus DC bias flat profile is associated with some Fermi level pinning in the bandgap, and a high ρ_{eff} value is associated with a deep Fermi level pinning in the bandgap. The obtained values for those samples are very stable versus DC bias showing that the Fermi level is pinned in the bandgap. The 600 °C annealed sample reaches a flat ρ_{eff} value of 4 kΩ cm over the whole DC bias range. This indicates a deeper Fermi level pinning in the 600 °C sample than in the 400 °C and nonannealed samples. The 800 °C annealed sample shows a different behavior. ρ_{eff} is stable between -15 and +8 V at 4 kΩ cm. Then, ρ_{eff} drops from 4 kΩ cm at +8 V down to 2.6 kΩ cm at +15 V. This asymmetry testifies to an efficient hole trapping (high ρ_{eff} in negative bias) and an inefficient electron trapping (low ρ_{eff} in positive bias). The 900 °C annealed sample also presents this asymmetry in the ρ_{eff} profile as ρ_{eff} drops from

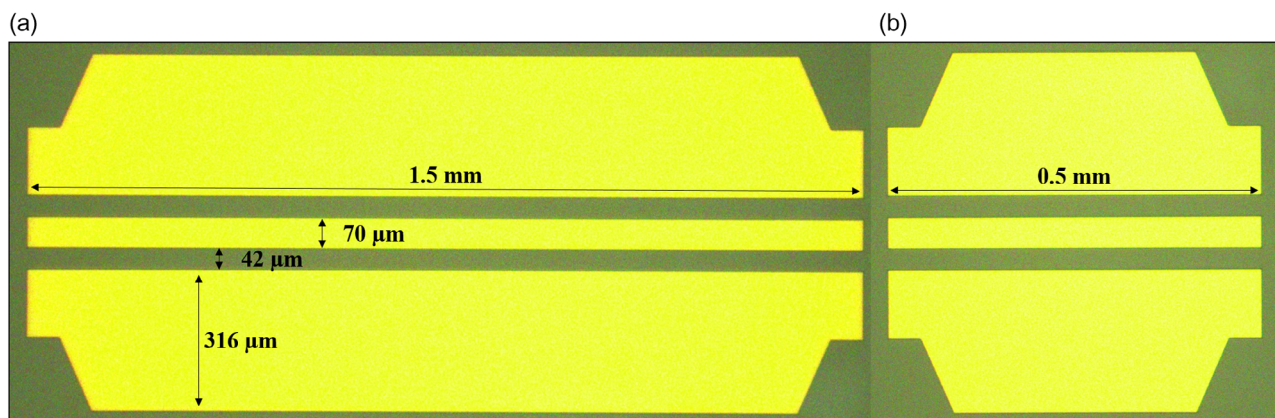


Figure 1. Photography of the two CPW used for RF characterization with lengths of a) 1.5 mm and b) 0.5 mm.

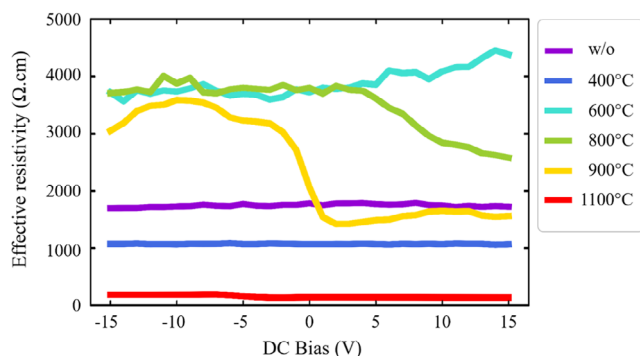


Figure 2. Effective resistivity (mean value between 5.5 and 6.5 GHz) at room temperature for all He⁺ implanted dielectric-on-silicon samples versus DC bias.

4 kΩ cm for negative biases down to 1.4 kΩ cm for positive biases. The ρ_{eff} value of the 1100 °C annealed sample drops to the low value of 100 Ω cm.

To conclude, very-high RF performance is obtained using a 600 °C postimplantation annealing. In addition, as the proposed process is compatible with a local formation of traps over a wafer, it appears promising for the cointegration of TR layer with FD-SOI technology.

2.3. Defect Identification by PL

We try to identify the crystalline defects present in our samples as a function of the annealing temperature. Actually, the He⁺-implantation-based process gives high RF performance for a thermal budget until 600 °C. Nevertheless, it could be interesting to clearly identify the crystalline defects leading to the charge carrier trapping which is effective for RF applications.

To get information about the crystalline defects nature in our samples, PL spectroscopy measurements are performed. The sample is held at 10 K inside a cryostat, and measurements are performed using a confocal microscopy setup. Continuous optical excitation is provided using a 485 nm laser diode. The

light is focused onto the sample surface using a microscope objective with a numerical aperture (NA) = 0.26 (Mitutoyo M Plan Apo NIR 10×). The PL is collected using the same objective and sent to a grating spectrometer with a photodiode array camera for spectral analysis. The PL spectra for all samples are shown in **Figure 3**. The nonannealed sample (**Figure 3a**) presents a sharp peak at 1218 nm corresponding to the zero-phonon line (ZPL) of the W-center, which is a 3-interstitials cluster.^[11] This sample also presents a low-intensity broad D3-line around 1330 nm which is probably associated with small interstitial clusters (ICs).^[12] The 400 °C annealed sample (**Figure 3b**) presents a sharp peak at 1120 nm associated with intrinsic band recombination in silicon,^[13] indicating the crystalline recovery of the silicon lattice. A peak at 1190 nm is observed and associated with the ZPL of the X center (4-interstitials cluster).^[11] The D3 line is still present whereas the W center disappears as expected at this temperature.^[14] For the 600 °C annealed sample (**Figure 3c**), we can still observe the Si line and the D3-line. Nevertheless, an additional peak corresponding to the R-line appears near the D3-line at around 1376 nm. This R-line is associated with the presence of {311} defects in the sample.^[12,15] The 800 °C annealed sample (**Figure 3d**) still shows the Si-line and two non-previously observed broad D2 and D1 lines around 1440 and 1522 nm, respectively. These lines are associated with dislocation loops (DLs).^[12] For the 900 and 1100 °C annealed samples (**Figure 3e,f**, respectively) spectra, we can only see the Si-line.

2.4. Defect Morphology by STEM

We qualitatively analyze the STEM images and their consistency with PL spectra. Based on PL spectra obtained with our samples, we expect to see at least {311} defects, DLs, and cavities in STEM images. STEM observations using bright-field (BF) contrast performed on nonannealed, 600 °C, and 800 °C annealed samples are shown in **Figure 4**.

The nonannealed sample presents a highly damaged Si matrix with numerous small ICs (in black contrast). This probably explains why the corresponding PL spectra (**Figure 3a**) do not show the Si-line. This sample also presents some small {311}

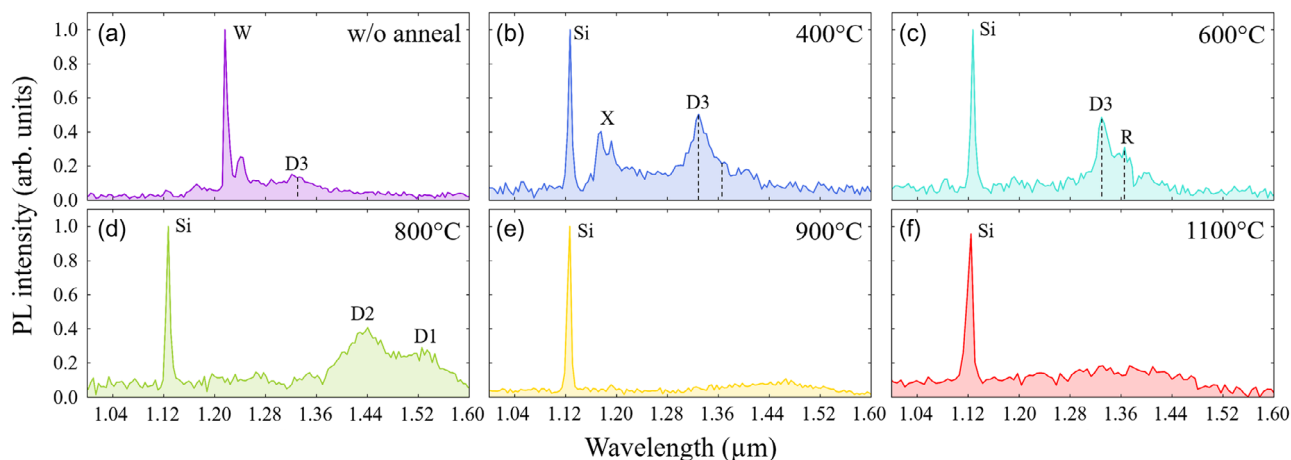


Figure 3. a) PL spectra measured at 10 K with a 488 nm laser of He⁺-implanted dielectric-on-silicon samples with no anneal, or 2 h anneals at b) 400 °C, c) 600 °C, d) 800 °C, e) 900 °C, and f) 1100 °C.

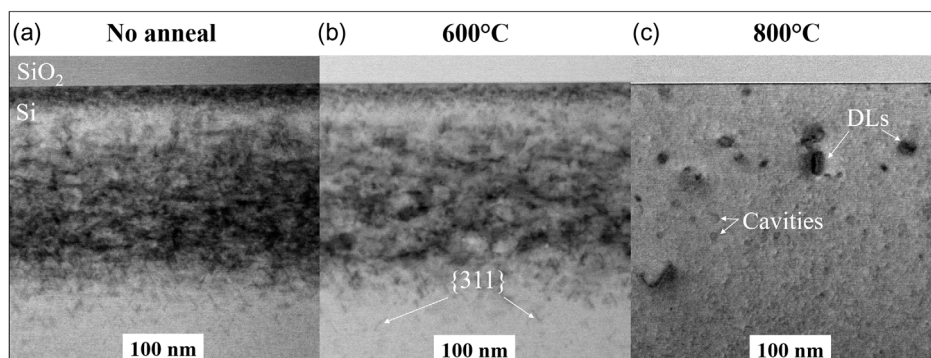


Figure 4. a) STEM-BF imaging of He⁺ implanted Silicon samples with no anneal, or 2 h anneals at b) 600 °C and c) 800 °C.

like defects in the end-of-range (EOR) region of the He⁺ implantation. These defects cannot be seen on the associated PL spectra probably due to their small density. For the 600 °C annealed sample, the presence of large {311} defects in the EOR region is highlighted in Figure 4. This is consistent with the observation of the R-line in the associated PL spectra (Figure 3c), confirming the presence of {311} defects. Moreover, those defects are known to be formed in silicon after ion implantation and annealing in the 600–750 °C range.^[16] Otherwise, in the 800 °C annealed sample, no {311} defects are present due to their dissolution. Nevertheless, DLs are observed, once again confirming the PL spectra observations (Figure 3d). The presence of empty cavities is also highlighted in the 800 °C annealed sample. Indeed, cavities are formed after high-dose He-implantation (typically > 1 × 10¹⁶ at cm⁻²) in Si.^[17] Cavities are also present in the non-annealed and 600 °C annealed samples, but cannot be easily seen with the used STEM-BF contrast due to their small diameters at that temperature.

3. Discussions

In the previous sections, we showed that the RF performance of substrates implanted with He⁺ ions evolves as a function of annealing temperature. An optimum RF performance is obtained for the 600 °C annealed sample. We also studied defects morphology using PL and STEM and showed that {311} defects were preferentially present in the 600 °C annealed sample. In this section, we discuss the link between defects morphology, their associated trapping levels obtained by C–V measurements, and the RF performance at the substrate level. The electrical activity of ion implantation-induced defects has been widely studied using a combination of PL and deep-level trap spectroscopy measurements.^[18,19]

3.1. Asymmetric ρ_{eff} Versus DC Bias Profile

First, we can discuss the presence of an asymmetry in the ρ_{eff} versus DC bias profile of the 800 °C and 900 °C annealed samples. Indeed, the fact that ρ_{eff} is higher in the negative DC bias range is due to more efficient trapping of holes than electrons trapping in these substrates. We showed that cavities and DLs (only for the 800 °C annealed sample, see Figure 4c) are the single extended defects present in these samples. Actually, DLs are

known to create deep acceptor trapping levels,^[19] whereas cavities generate deep donor levels.^[20] This can probably explain why the ρ_{eff} versus DC bias profile of the 800 °C sample is slightly asymmetric: the DLs density is still high enough to provide good electron trapping. Thus, the ρ_{eff} versus DC bias profile of the 900 °C sample is highly asymmetric because of the deep holes trapping provided by the cavities and the weak electrons trapping provided by DLs which are present in extremely low density.

3.2. Defects Suitable for High RF Performance

Second, it could be interesting to identify the crystalline defects that are responsible for very-high RF performance obtained after a 600 °C anneal. As the PSC layer fixed charges generate an accumulation of electrons beneath a SiO₂ layer, we focus on electrons traps. Indeed, we previously showed that cavities are responsible for holes trapping, proving that they are not responsible for the high performance obtained at 600 °C. **Table 1** lists the different crystalline defects identified by PL or STEM as a function of the annealing temperature. In this table, defects that are known to generate a deep acceptor trapping level are highlighted. By making a comparison with ρ_{eff} values obtained at 0 V (i.e., only the PSC contribution), we can argue that {311} defects are effective for electron trapping in the RF domain.

Although the impact of the annealing time has not been widely studied in this article, it is an important parameter that can highly affect defects morphology. Nevertheless, defects generated by He implantation in Si (such as He bubbles) mainly

Table 1. Crystalline defects identified with respect to annealing temperature. Defects that are known to generate a deep acceptor trap are highlighted with a star.

Temperature	post-implantation	400 °C	600 °C	800 °C	900 °C
Defects					
Point defects	x	x	–	–	–
ICs*	x	x	x	–	–
He-bubbles	x	x	x	–	–
{311}*	–	–	x	–	–
Cavities	–	–	–	x	x
DLs*	–	–	–	x	x

evolved in the first instants of annealing.^[17] Thus, if the annealing time is longer than a few tens of minutes, the impact of the annealing time should be minor compared to the impact of the annealing temperature.

3.3. Influence of Defects Layer Depth

As the electric field generated by fixed oxide charges at the SiO₂/Si interface evolves as $\frac{1}{r^2}$, it is generally admitted that it is more favorable to generate traps as close as possible to this interface. Thus, the formation depth of electrically active defects should have a strong impact on RF performance. However, it is known that amorphizing ion implantation generates {311} defects in the EOR implantation zone, whereas nonamorphizing ion implantation generates them around the projected range (R_p) depth (corresponding to the maximum ion concentration).^[16] In our case, He-implantation generates a number of vacancies above the amorphization threshold of Si, leading to an EOR defects layer depth of about 300 nm beneath the oxide layer for the deepest He⁺ implantation. Thus, there is probably a way to optimize our process by reducing this depth.

4. Conclusion

In this article, we measured the RF performance of He⁺-implanted high-resistivity silicon wafers. We showed that the postimplantation annealing temperature had a strong impact on RF performance. Thermal annealing at 600 °C for 2 h led to a high RF performance with an effective resistivity of 4 kΩ cm over the whole measured DC bias range. We also investigated the defects that are responsible for high RF performance at this temperature combining PL and STEM measurements. Due to the presence of the R-band in the PL spectrum for the 600 °C annealed sample, we can argue that {311} defects, which were also observed in STEM micrographs, were probably at the origin of such RF performance. This result enables the development of defects engineering strategies for enhanced RF semiconductor substrates, opening the way for another local RF passivation technique using ion implantation. Such a local RF passivation technique using ion implantation seems promising for the co-integration of high-performance FD-SOI and RF devices.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

ion implantation, photoluminescence, radiofrequency, silicon-on-insulator, trap-rich layers

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