



HAL
open science

On-Line Digital Fine Monitoring of SiC MOSFET Gate-Oxide Health: A Dual-Channel Gate Driving Approach

Mathis Picot-Digoix, T-L Le, S. Azzopardi, Sébastien Vinnac, Frédéric Richardeau, Jean-marc Blaquiere

► **To cite this version:**

Mathis Picot-Digoix, T-L Le, S. Azzopardi, Sébastien Vinnac, Frédéric Richardeau, et al.. On-Line Digital Fine Monitoring of SiC MOSFET Gate-Oxide Health: A Dual-Channel Gate Driving Approach. 2024 36th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Jun 2024, Bremen, Germany. pp.84-87, 10.1109/ISPSD59661.2024.10579698 . hal-04647322v1

HAL Id: hal-04647322

<https://hal.science/hal-04647322v1>

Submitted on 14 Jul 2024 (v1), last revised 15 Jul 2024 (v2)

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

On-Line Digital Fine Monitoring of SiC MOSFET Gate-Oxide Health: A Dual-Channel Gate Driving Approach

M. Picot-Digoix, T-L Le, S. Azzopardi
Safran Tech, Safran
Paris, France
mathis.picot-digoix@safrangroup.com

S. Vinnac, F. Richardeau, J-M. Blaqui re
LAPLACE, Universit  de Toulouse
CNRS, INPT, UPS
Toulouse, France

Abstract— SiC power MOSFETs, compared to their Si counterparts, still lack maturity, hindering their adoption in aeronautical applications. Consequently, there is a growing need for the development of smart gate drivers with built-in functions like health monitoring. Reducing failures and downtime in power converters relies on an early detection of component ageing. However, assessing reliably the health condition of power transistors in PWM operation remains a challenge. In this perspective, a non-invasive strategy is proposed. This approach aims to determine precisely and accurately the health state of the gate oxide of a SiC power MOSFET. It uses a dual-channel gate driver to trigger a slow turn-on event and clean switching measurement within a PWM frame. This method involves an on-line tracking of oxide ageing, or charge-trapping indicators present in the gate signal waveform.

Keywords— SiC MOSFET; health monitoring; gate driver; gate oxide

I. INTRODUCTION

In silicon (Si) MOSFETs, a uniform and low-defect gate oxide layer is facilitated by the natural chemical affinity between Si and silicon dioxide (SiO₂). Conversely, silicon carbide (SiC) exhibits a crystalline structure distinct from Si, rendering the SiC/SiO₂ interface more prone to defect formation and consequent reduction in channel mobility [1]. To mitigate the decreased electron mobility in SiC MOSFETs, gate oxide thickness is minimised to optimise channel resistance and attain an acceptable threshold voltage [2].

The reduction in gate oxide thickness enhances the applied electric field and electrical stress on the gate oxide. SiC MOSFETs typically operate at high temperatures, exacerbating charge trapping tunnelling in near-oxide interface defects. Consequently, intrinsic MOSFET parameters drift over time, leading to performance degradation and reliability issues. In current practice, the assessment of MOSFET health primarily revolves around monitoring the plateau voltage (V_P) [3, 4, 5]. However, this parameter is heavily influenced by the operating point, which significantly impacts measurement reliability. Some approaches opt for a threshold voltage (V_{TH}) monitoring strategy. Although effective in reflecting the transistor's ageing, extracting its value on-line presents challenges [6]. One proposed solution involves detecting the MOSFET's channel formation and extracting the gate-source voltage (V_{GS}) at this

moment (approximately equal to V_{TH}). However, its validation in PWM operation is pending [7].

The proposed method entails a rapid on-line and accurate digitisation of a segment of V_{GS} to extract several health indicators, including V_P, the duration of the plateau (Δt_P), and a knee voltage (V_{KN}) approaching V_{TH} in no-load operation (refer to Fig. 1b) characterised by a decrease in the V_{GS} slope.

II. PROPOSED APPROACH

As illustrated in Fig. 1a (blue and red curves), the load current (I_{LOAD}) significantly influences the V_{GS} turn-on waveform, leading to reverse recovery overshoot, oscillations, and a general decline in signal quality. Moreover, extracting the targeted health indicators from a V_{GS} turn-on waveform necessitates a slowdown of the switching process, as depicted in Fig. 1a (yellow curve).

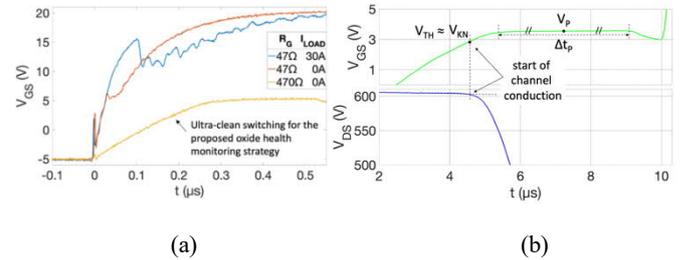


Fig. 1. Influence of gate resistance and load current on the turn-on waveform of V_{GS} (V_{DS}=600V) for a 1.2kV 80mΩ SiC MOSFET in half-bridge operation (a), definition and illustration of the various health indicators considered on V_{GS} during a no-load turn-on (b)

Employing a high-value gate resistance enables the desired health indicators, particularly the plateau voltage, to remain uncontaminated by non-health-related contributions:

$$V_P(t) \approx V_{TH} + \frac{I_{LOAD}}{G_{FS}} + \frac{2C_{OSS}}{G_{FS}} \frac{dV_{DS}}{dt} + f\left(\frac{\lambda}{G_{FS}} \cdot V_{DS}(t)\right) \quad (1)$$

where I_{LOAD} represents the load current directed into the midpoint of the inverter leg, V_{BUS} is the DC bus voltage, G_{FS} is the transconductance of the MOSFET, C_{OSS} is its output capacitance, and λ its short channel parameter representing the oblique evolution of the plateau in SiC MOSFETs. Although this short channel is inherent to the SiC transistor's structure and cannot be mitigated, the impact of both the load current

I_{LOAD} and turn-on dynamics can be lessened to reduce their influence on V_P . This ensures that variations in V_{TH} are not overshadowed and are accurately reflected by V_P , rendering it a more relevant health indicator. Therefore, the strategy adopted to extract health indicators from the V_{GS} waveform involves slowing down the turn-on process using a high-value gate resistance to achieve a measurement-oriented clean switching. This is achieved through a dual-channel gate driver, as introduced in [8] and depicted in Fig. 2.



Fig. 2. Test schematic, proposed gate driving architecture, and SiC MOSFET health monitoring scheme ($V_{DD}=20V$, $V_{SS}=-5V$, $V_{BUS}=600V$, $L=7.6mH$, $R=82\Omega$)

During normal switching operation, a conventional low-value gate resistance, “Fast” buffer is used (Enable=1) to ensure high switching dynamics for the MOSFET. However, when the FPGA initiates a slow turn-on health measurement, this buffer is transitioned into a high-impedance state (Enable=0), allowing the always active high-value gate resistance *Slow* buffer to take over and govern the slow turn-on dynamics.

The digitisation of V_{GS} is done at 5Mps with 12 bits and is controlled by an FPGA. It can accurately and consistently replicate the operating point by initiating the slow turn-on at a specific moment in the sinusoidal modulating period (T_{MOD}) when the current is negligible, ensuring comparable measurements over time. Therefore, it is crucial to ensure that the frequency of the modulating signal (f_{MOD}) is a submultiple of the carrier frequency (f_{SW}). It ensures a consistent replication of the operating point; otherwise, an active measurement of the load current is required to anticipate the next zero-crossing of the current. To increase the temporal resolution of V_{GS} , a multi-cycle time-interleaved acquisition technique is used, triggered at the same point ($n.T_{MOD}$). Such a method allows reaching a sampling rate of 175Mps and an extreme accuracy of the extracted indicators (see Fig. 5 and Tab. 1).

For each acquisitions cycle, a V_{GS} derivative calculation is performed. When the derivative decreases slightly, it is considered that the beginning of the knee is reached. This phenomenon occurs due to the start of the V_{DS} commutation; thus, it is a first marker of V_{TH} . After that, a sharp decrease in the derivative is sought to detect the beginning of the plateau, and the end of the plateau is detected by the appearance of a strong negative value on the derivative. These values are memorized for each cycle, and the average of all cycles is

calculated, discarding any values that are very far away if they exist.

III. EXPERIMENTAL SETUP

The Device Under Test (DUT) is a discrete TO-247-3L package 1200V-36A-80m Ω planar gate SiC MOSFET. The proposed strategy uses a dual-channel gate driver plugged into a 600V inverter leg test power bench. Heatsinks are attached to the Devices Under Test (DUT) to decrease the thermal resistance between their case and the ambient air to stabilise their case temperature as much as possible.

M. Picot-Digoix, T. -L. Le, S. Azzopardi, S. Vinnac, F. Richardeau and J. -M. -M. Blaquière,
 "On-Line Digital Fine Monitoring of SiC MOSFET Gate-Oxide Health: A D A Dual-Channel Gate Driving Approach,"
 2024 36th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Bremen, Germany, 2024, pp. 84-87,
 Accepted Author Version (Extended Abstract) Manuscript : <https://hal.science/hal.science/> (Open Access)
 Editor Version : doi: 10.1109/ISPSD59661.2024.10579698.

Fig. 3. 600V test bench comprising high-side and low-side SiC MOSFETs and zoom on the proposed health monitoring gate driver PCB as detailed in Fig. 2 (5.3x3.1cm)

IV. RESULTS AND SIGNIFICANCE

Measurements are first conducted at a 600V no-load 20kHz PWM condition. A slow turn-on through a high-value gate resistance (see Fig. 2) is inserted within the PWM frame (see Fig. 4). When the Miller plateau's end is identified, the low-value *Fast* buffer is reactivated, to quickly complete the gate charge.

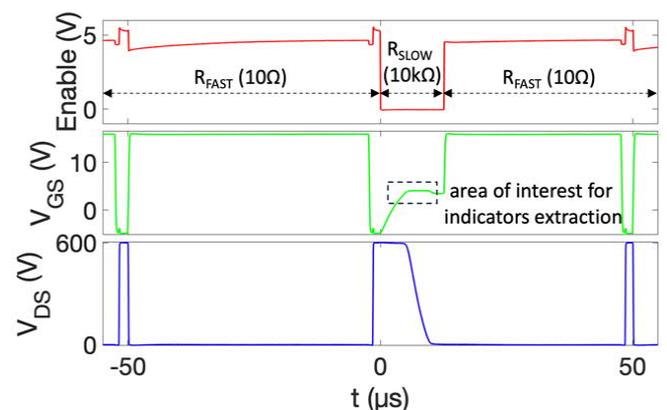


Fig. 4. Inclusion of a slow turn-on measurement within a PWM frame at no-load condition ($f_{SW}=20kHz$, $f_{MOD}=100Hz$, $V_{BUS}=600V$)

This non-invasive slow turn-on is completed in only $8\mu\text{s}$ or 16% of the switching period. As depicted in Fig. 5, a comparison is conducted at no-load condition between the V_{GS} waveform obtained by an oscilloscope and the one obtained by the proposed acquisition system. On the plateau area of interest, the relative error between the two signals is less than 0.5% which validates the extreme accuracy of the proposed V_{GS} extraction method.

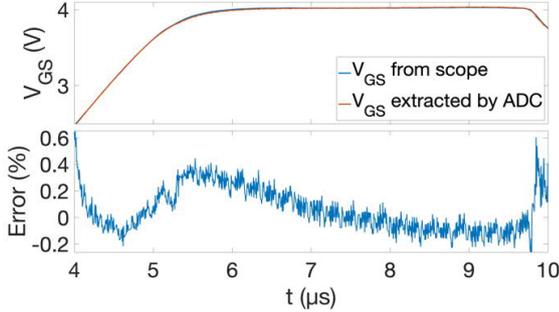


Fig. 5. Relative error between the V_{GS} waveforms obtained by the oscilloscope (Tektronix DPO4104B, averaged over 32 cycles) and by the proposed acquisition system (no-load condition)

Then, to evaluate the proposed health monitoring method under no-load condition, DUTs are subjected to accelerated ageing through High-Temperature Gate Bias (HTGB) stress for 24 hours under a gate bias of 35V. This facilitates and accelerates the gate-oxide charge trapping process that would happen slowly over time under normal operation.

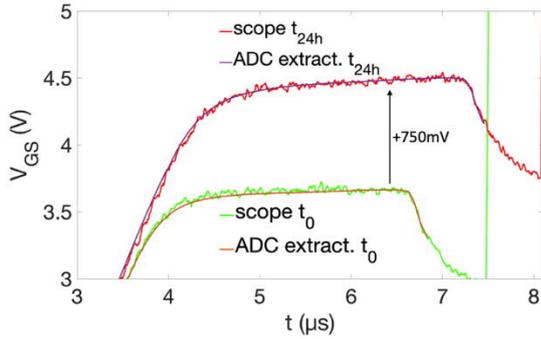


Fig. 6. Comparison of the V_{GS} waveforms between a healthy transistor and an aged one (stress conditions: $V_{GS}=35\text{V}$, $T_{CASE}=150^\circ\text{C}$ for 24h) within a PWM frame (no-load, $T_{CASE}=20.5^\circ\text{C}$, $V_{BUS}=600\text{V}$)

After the stress, the SiC MOSFET case is cooled down to a stable ambient temperature of 20.5°C to eliminate the V_{TH} temperature-related-drift ($\approx 10\text{mV}/^\circ\text{C}$). The comparison of the before/after stress V_{GS} turn-on waveforms is given in Fig. 6. Following the accelerated ageing stress, a significant drift of $+750\text{mV}$ ($+20\%$) is observed on the plateau area. Simultaneously, the extracted V_{GS} waveform is directly displayed by the FPGA control board on a touchscreen user interface as depicted in Fig. 7. Coming from dedicated derivative criteria, the three targeted health indicators (see Fig. 1b) are then added to the displayed waveform. The same protocol is then applied with an RL load (see Fig. 2), with measurements synchronized around a zero-current point at a certain duty cycle (see Fig. 8).



Fig. 7. Controller interface, visualisation of the health indicators on the extracted V_{GS} waveform (each indicator arises from dedicated derivative criteria). Here, $V_{KN}=3315\text{mV}$, $V_P=4453\text{mV}$, and $\Delta t_p=2868\text{ns}$.

The extreme accuracy and repeatability of the health indicators are confirmed (see Tab. 1) and a parameter's drift of 620mV ($+14\%$) is detected after stress (see Fig. 9 and Tab. 2), which validates the concept both in no-load and loaded conditions.

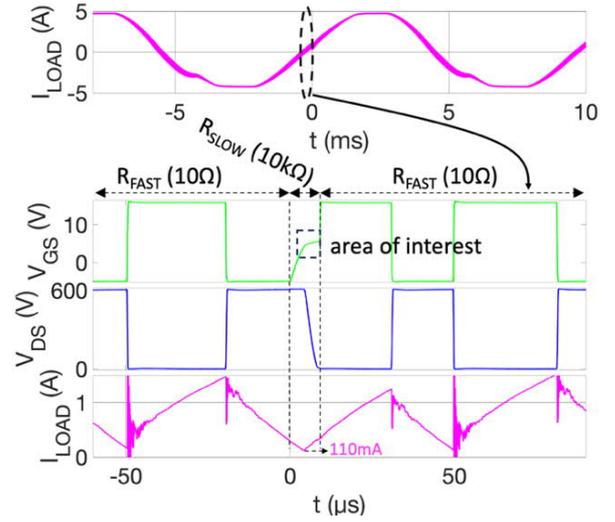


Fig. 8. Inclusion of a slow turn-on measurement within a PWM frame manually synchronised around a zero-current point ($f_{sw}=20\text{kHz}$, $f_{MOD}=100\text{Hz}$, $V_{BUS}=600\text{V}$)

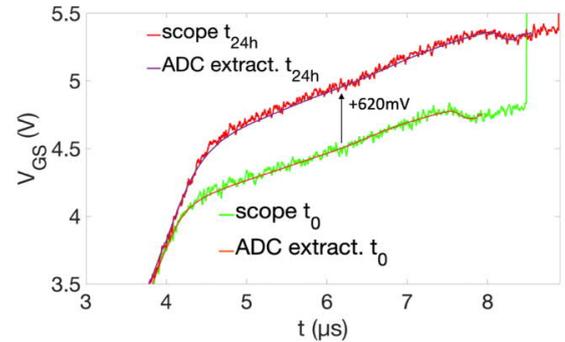


Fig. 9. Comparison of the V_{GS} waveforms around the plateau region between a healthy transistor and a stressed one (stress conditions: $V_{GS}=35\text{V}$, $T_{CASE}=150^\circ\text{C}$ for 24h) within a PWM frame (RL load, $T_{CASE}=20.5^\circ\text{C}$, $V_{BUS}=600\text{V}$)

To evaluate the repeatability of the proposed system and the stability of indicator measurements, a set of 20 slow turn-ons is executed. The values of the extracted indicators are displayed on the user interface (refer to Fig. 7). Each value is recorded, and the Relative Standard Deviation (RSD) is reported in Tab. 1.

TABLE I. REPEATABILITY STUDY ON EXTRACTED HEALTH INDICATORS OVER 20 SUCCESSIVE MEASUREMENT CAMPAIGNS (DUT n°1)

	Health Indicator	Mean Value	Standard Deviation	Relative Standard Deviation
No-Load	V_{KN}	3.31V	5.2mV	0.16%
	V_P	4.42V	12.9mV	0.29%
	Δt_P	2.87 μ s	6ns	0.21%
RL Load	V_{KN}	3.30V	8.9mV	0.27%
	V_P	4.99V	24.5mV	1.63%
	Δt_P	5.35 μ s	19ns	0.36%

It is shown that the proposed health monitoring system provides extremely stable results whether under no-load or loaded conditions. This consistency enables reliable comparisons over time to detect possible ageing-related-drifts (refer to Tab. 2), confirming the effectiveness of the approach.

TABLE II. COMPARISON OF EXTRACTED HEALTH INDICATORS IN A PWM FRAME BEFORE AND AFTER STRESS

	Health Indicator	Fresh MOSFETs	Stressed MOSFETs
No-Load (DUT n°2)	V_{KN}	2.93V	3.32V (+13%)
	V_P	3.70V	4.45V (+20%)
	Δt_P	2.67 μ s	2.87 μ s (+7.5%)
RL Load (DUT n°3)	V_{KN}	3.26V	3.60V (+10%)
	V_P	4.50V	5.12V (+14%)
	Δt_P	3.31 μ s	3.46 μ s (+5%)

The sensitivity of the considered health indicators to an HTGB stress is detailed in Tab. 2. Among them, V_P emerges as the most responsive indicator: under a given stress and a fixed quantity of trapped charges in the gate oxide layer, V_P displays the most pronounced drift (up to +20%). This increased sensitivity arises from the combined impacts of decreased channel electron mobility (hence, decreased G_{FS}) and elevated V_{TH} . Consequently, V_P stands out as a preferred indicator for monitoring the health condition of SiC MOSFETs.

V. CONCLUSION

An original on-line strategy for monitoring the health of SiC MOSFET gate oxide is introduced. This method relies on a dual-channel gate driver capable of selectively switching between a traditional low-value and an original high-value gate resistor to intentionally slow down specific turn-on events. This allows sufficient time for digitising a segment of the V_{GS} waveform around the plateau region, enabling the digital extraction of three health indicators. The effectiveness of this approach is evaluated under both no-load and on-line loaded conditions, using SiC MOSFETs subjected to accelerated ageing. The evaluation reveals indicators drifts of up to +750mV (+20%) and +620mV (+14%), respectively, as detected by the controller. Additionally, the relative relevance of the considered health indicators is discussed, with the plateau amplitude emerging as an indicator of choice.

REFERENCES

- [1] S. T. Pantelides et S. Wang, "Si/SiO₂ and SiC/SiO₂ Interfaces for MOSFETs – Challenges and Advances," *Silicon Carbide and Related Materials*, vol. 527, pp. 935-948, 2005.
- [2] U. Karki, N. S. Gonzalez-Santini et F. Z. Peng, "Effect of Gate-Oxide Degradation on Electrical Parameters of Silicon Carbide MOSFETs," *IEEE Transactions on Electron Devices*, vol. 67, pp. 2544-2552, 2020. I.S. Jacobs and C.P. Bean, "Fine particles, thin films and exchange anisotropy," in *Magnetism*, vol. III, G.T. Rado and H. Suhl, Eds. New York: Academic, 1963, pp. 271-350.
- [3] B. Akin, S. Pu, F. Yang, E. Ugur and C. Xu, "SiC MOSFET Aging Detection Based on Miller Plateau Voltage Sensing," *IEEE Transportation Electrification Conference and Expo (ITEC)*, pp. 1-6, 2019.
- [4] M. Wang, W. J. Zhang, J. Y. Liang, W. Tung Ng, H. Nishio, H. Sumida et H. Nakajima, "A Smart Gate Driver for SiC Power MOSFETs with Aging Compensation and Ringing Suppression," *International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pp. 67-70, 2021.
- [5] M. Wang, J. Zhang, W. T. Ng, H. Nishio, M. Iwamoto et H. Sumida, "Application of a Smart Gate Driver to Detect Aging in SiC Power MOSFETs," *International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pp. 187-190, 2023.
- [6] X. Jiang, J. Wang, H. Yu, J. Chen, Z. Zeng, X. Yang et Z. J. Shen, "Online Junction Temperature Measurement for SiC MOSFET Based on Dynamic Threshold Voltage Extraction," *IEEE Transactions on Power Electronics*, vol. 36, pp. 3757-3768, 2021.
- [7] M. Farhadi, B. T. Vankayalapati, R. Sajadi and B. Akin, "AC Power Cycling Test Setup and Condition Monitoring Tools for SiC-Based Traction Inverters," *IEEE Transactions on Vehicular Technology*, vol. 72, pp. 12728-12743, 2023.
- [8] M. Picot-Digoix, F. Richardeau, J.-M. Blaqui re, S. Vinnac, S. Azzopardi et T.-L. Le, "Quasi-Flying Gate Concept Used for Short-Circuit Detection on SiC Power MOSFETs Based on a Dual-Port Gate Driver," *IEEE Transactions on Power Electronics*, vol. 38, pp. 6934-6938, 2023.