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CMOS Gate Driver with Integrated Gate Current Monitoring Method for Fault Under Load Short Circuit Detection of SiC Power Modules

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Abstract— Existing literature has primarily focused on using gate signals for short-circuits type I detection (Hard Switch Fault, HSF) replacing the traditional desaturation method and eliminating external components (high-voltage Diode). However, an unaddressed aspect remains in detecting short-circuit type II (Fault Under Load, FUL). This article introduces a Gate-Driver (GD) IC with a fully integrated approach for the FUL detection. This solution strategically uses the gate current copy (I_{gcopy}), enabling ultra-fast FUL detection. Experimental results demonstrate reliable fast short-circuit detections for power modules, in less than 100ns. This IC is fabricated using NXP Semiconductors' high-voltage SMARTMOS10 130nm CMOS SOI technology. The integration of these complementary detection methods (HSF & FUL) in the High-Side and Low-Side SiC MOSFET (for power modules) GDs effectively addresses the challenge of ensuring a full Half-Bridge protection system.

Keywords— SiC MOSFET; CMOS; Gate Driver; Current sensing; Short-Circuit; Detection; Fault Under Load; Power module

I. INTRODUCTION

Silicon Carbide (SiC) is one of the prime examples of Wide Bandgap (WBG) semiconductor materials gaining traction in the market due to their superior properties. They offer higher efficiency and faster switching speeds compared to traditional Silicon Insulated Gate Bipolar Transistors (IGBTs), making them ideal for applications where power density, size, and efficiency are critical. However, these advantages give rise to certain technical challenges which must be addressed such as short-circuit (SC) ruggedness demanding a fast SC detection and protection in less than 1 μ s. Common SC detection techniques employed in industrial applications and presented in the literature often center around monitoring power signals, notably using methods such as the Desaturation method (for Drain-Source voltage monitoring, V_{DS}). However, this method necessitates an external high-voltage diode, leading to potential cross-talk issues between the power circuit and the GD. Alternatively, some systems monitor the Drain Current (I_{drain}), yet this approach can be expensive, space-consuming, or highly dependent on parameters like the parasitic power source inductance¹ (L_s).

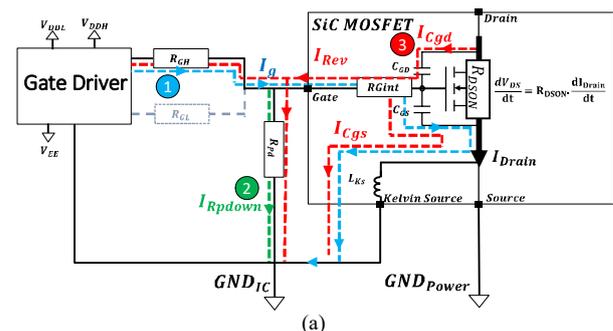
Regarding the gate signals (such as the gate-source voltage, V_{GS} , or the gate current, I_g , or the gate charge, Q_g) monitoring systems of power devices, the focus is mainly on using them solely for HSF detection. To overcome these issues, we have extended and upgraded our previously demonstrated technique from ISPSD2023. Our approach uses an accurate integrated I_{gcopy} monitoring system that detects any modifications in gate current resulting from FUL SC.

II. BENEFITS AND CHALLENGES OF THE GATE CURRENT MONITORING APPROACH FOR FUL SHORT-CIRCUIT

In a Half-Bridge circuit, the FUL SC case occurs on a power device under test (DUT) after fully charging it. The FUL SC is caused by either a command error or a failure in the complementary power device. Before the fault, the DUT operates in its ohmic region, characterized by the maximal gate-drain capacitance value (C_{gdmx}). When the FUL fault starts, a high fault drain current variation (dI/dt_{Fault}) flows through the DUT. This dI/dt_{Fault} , combined with the DUT's on-resistance ($R_{DS(ON)}$), results in a high and positive dV_{DS}/dt . Consequently, this high dV_{DS}/dt induces reverse gate current (I_{Rev}) and gate over-voltage (ΔV_G) in the gate signals (V_{GS} and I_g) due to the coupling between power and gate signals through C_{gdmx} .

The proposed concept involves using I_{gcopy} to monitor the current through the Pull-Down resistor (I_{RpD} , ranging from 0.5mA to 1.5mA, for instance) supplied by the GD after fully charging the power device to establish a positive current offset (depicted in green in Fig. 1). A decrease in I_g indicates to the GD that additional current is being generated by the power device (illustrated in red in Fig. 1). This method allows us to detect any modification in the I_g generated by the GD. By implementing a current threshold (I_{Ref}) with I_{gcopy} , our system can identify the absence of positive I_g , indicating FUL SC.

The limitation of the demonstrated technique from ISPSD2023³ lies in its inability to copy negative I_g a constraint inherent in the proposed architecture, which can only copy positive variations of the I_g . Beyond the inability to copy a negative current, there is also another constraint regarding the current level scale. For HSF monitoring, we typically deal with copying an initial current that can reach 15A. However, in FUL monitoring, the current is typically around 1A in FUL cases and around a couple of mA in normal switching cases. So despite the simplicity of this SC detection approach, the key challenge lies in maintaining highly accurate I_{gcopy} to ensure fast and reliable detection system.



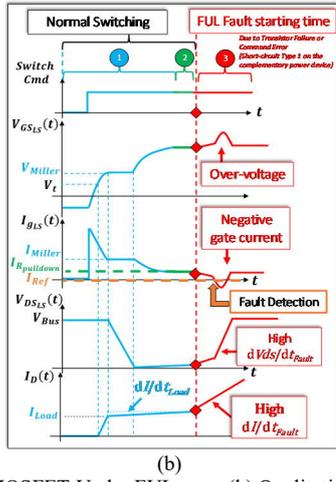


Fig. 1. (a) SiC MOSFET Under FUL case, (b) Qualitative SiC MOSFET signals in FUL case.

A. Robustness Assessments

To assess the robustness of this approach, we will consider the dispersion of the Half-Bridge circuit parameters that affect the I_{Rev} in normal switching cases (NTO) and FUL cases. Our analysis focuses on drain current variation set by the load (dI/dt_{Load}) as the primary cause of I_{Rev} in normal switching scenarios. Fig. 2 demonstrates this relationship through Cadence™ simulation, varying dI/dt_{Load} at different SiC MOSFET junction temperatures T_{jSiC} . Higher dI/dt_{Load} values lead to increased dV_{DS}/dt , resulting in elevated I_{Rev} . Additionally, I_{Rev} rises with T_{jSiC} due to the increase of the DUT's $R_{DS(on)}$ with temperature. Considering the impact of drain current (I_{drain}) value itself, higher drain currents raise SiC MOSFET on-resistance, further increasing I_{Rev} (as illustrated in Fig. 3).

The same study has been done in FUL cases, simulations shows a minimal I_{Rev} value of 0.14A, 3 times higher than the I_{Rev} in Normal switching cases at $dI/dt_{Load}=0.08\text{kA}/\mu\text{s}$ and $T_{jSiC}=25^\circ\text{C}$. This study highlights that adjusting the I_{Rpd} to the application's specification is crucial for ensuring robust SC detection.

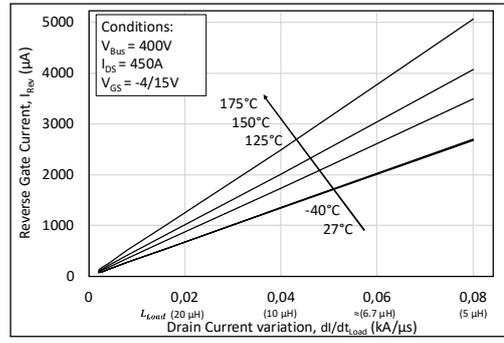


Fig. 2. dI/dt_{Load} versus I_{Rev} in NTO case in Cadence™ simulation for different T_{jSiC} : CAB450XM3 model, $R_{GH}=R_{GL}=1\Omega$, $V_{DDH}=15\text{V}$, $V_{EE}=-4\text{V}$, $L_{Bus} = 11\text{ nH}$, $L_{CS}=0.3\text{nH}$

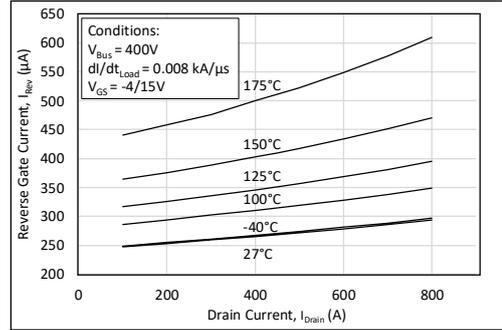


Fig. 3. I_{Drain} versus I_{Rev} in NTO case in Cadence™ simulation for different T_{jSiC} : CAB450XM3 model, $R_{GH}=R_{GL}=1\Omega$, $V_{DDH}=15\text{V}$, $V_{EE}=-4\text{V}$, $L_{Bus} = 11\text{ nH}$, $L_{CS}=0.3\text{nH}$

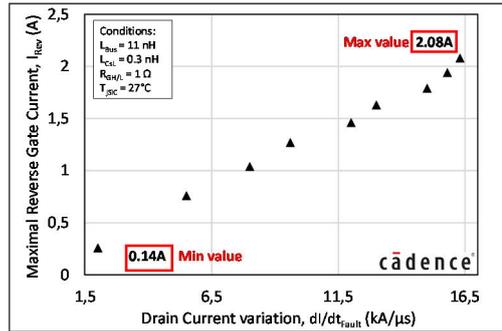


Fig. 4. dI/dt_{Load} versus I_{Rev} in FUL case in Cadence™ simulation: CAB450XM3 model, $V_{DDH}=15\text{V}$, $V_{EE}=-4\text{V}$

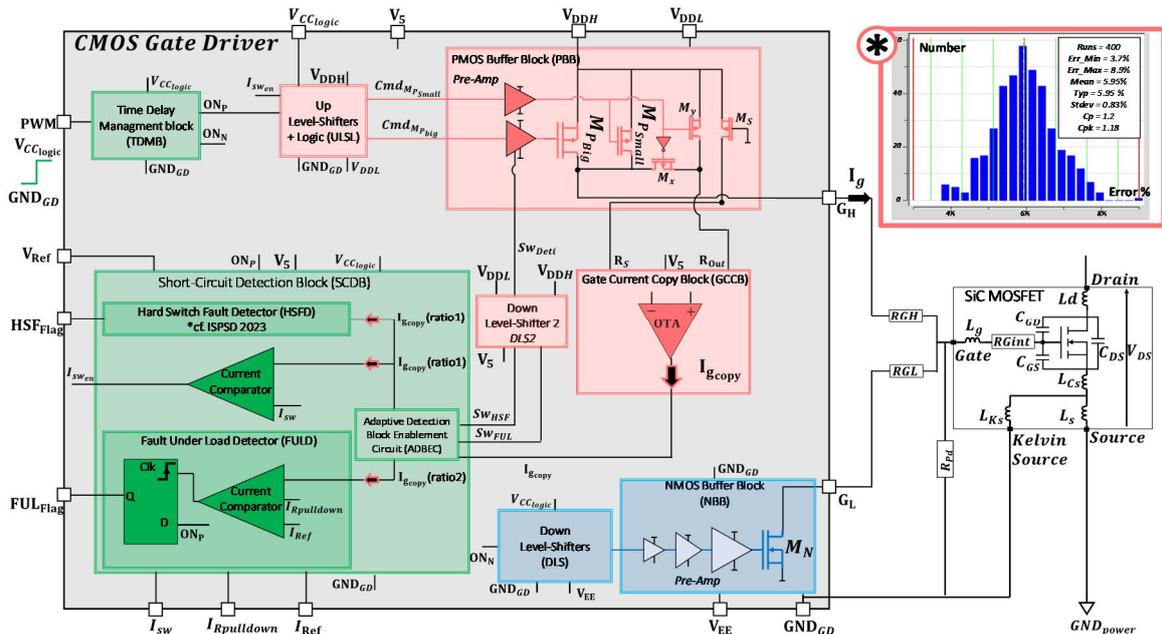


Fig. 5. Gate Driver architecture, * Histogram analysis: effect of process variation on the positive OTA performances for FUL monitoring

III. NOVEL GATE DRIVER ARCHITECTURE WITH AN ACCURATE, FAST AND INTEGRATED GATE CURRENT COPY

A. Gate driver architecture

The proposed design aims to improve the GD specifications presented in ISPSD2023, which involves having a fast and accurate I_{gcopy} during and after the power device charging phase. To achieve this, we propose to use two segmented PMOS Power Switches, M_{PBig} & M_{PSmall} (Fig. 5) in order to adapt the I_{gcopy} ratio to ensure high accuracy in monitoring the I_{Rpd} after fully charging the power device, allowing us to detect any modifications in I_g resulting from FUL SC. This integrated approach is more robust than monitoring (ΔV_G). To explain the concept behind this accurate I_{gcopy} , let's delve into the block diagram of the proposed GD architecture presented in Fig 6. During the SiC gate charging phase (PWM is high), M_{PBig} and M_{PSmall} are activated to rapidly charge the power device, while M_s generates internally the I_{gcopy} with a ratio approximately equal to 1600 (ratio #1). The end of the SiC MOSFET charging phase is detected by using a current comparator with the I_{gcopy} and a low current reference (I_{Sv}) as inputs. Once the end of SiC MOSFET charging is detected, M_{PBig} is deactivated, leaving only M_{PSmall} active. This leads to an increase in drop across M_{PSmall} enhancing the OTA's accuracy in copying this small I_g . Additionally, this reduces the I_{gcopy} ratio to 3 (ratio #2), determined by the ratio $(n_{gPsmall} \times n_{pPsmall}) / (n_{gS} \times n_{pS})$, with n_{gx} the number of gate segment of an elementary transistor and n_{px} the number of transistors connected in parallel. Subsequently, the FUL detection system is enabled with the new I_{gcopy} ratio. To replicate the external behavior of the I_g and obtain an integrated copy of the reverse gate current (I_{Rcopy}), the GD is given the pull-down resistor current divided by the same ratio #2. By having a I_{gcopy} and an integrated pull-down resistor current (I_{Rpdint}), the GD is capable of generating I_{Rcopy} . This copy is then used with a reference current (I_{Ref}) to detect FUL SC cases.

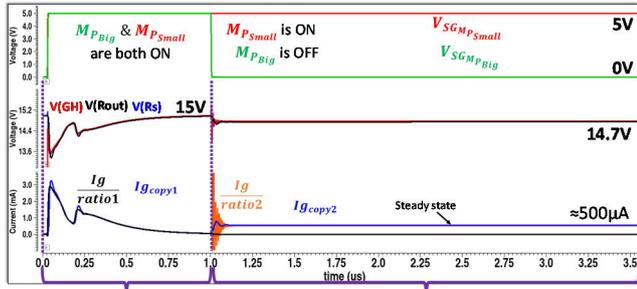


Fig. 6. Chronogram highlighting the selective activation mode between M_{PSmall} and M_{PBig} to modify the I_{gcopy} in NTO Cadence simulation: $R_{GHLowSide} = R_{GLLowSide} = 1\Omega$, $V_{DDH} = 15V$, $V_{EE} = -4V$, $L_{Bus} = 11$ nH, $L_{Cs} = 0.3$ nH, $R_{PullDown} = 10$ k Ω , $V_{Bus} = 400V$, $I_{Load} = 100A$, $L_g = 17$ nH, $T_{SiC} = 25^\circ C$

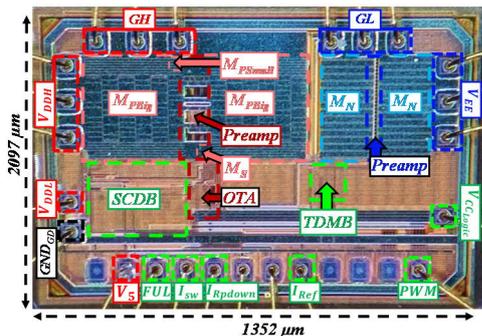


Fig. 7. Gate Driver bare die microscopic photo (2097 $\mu m \times 1352 \mu m$)

IV. SHORT-CIRCUIT DETECTION FUNCTIONALITY VALIDATION USING A SiC HALF-BRIDGE MODULE

To validate the concept and the robustness of the Short-Circuit Detection Block (SCDB) the GD is measured on the designed Evaluation Board connected (EVB_{designed}) to a SiC Half-Bridge power module (CAB450XM3: 1200V, 450A) driven on a homemade designed safe test-bench dedicated for SCs as shown in Fig. 8. Fig. 9 shows a normal switching event (Double Pulse Test), without any SC detection on the Low-Side SiC MOSFET (flag stays low). The High-Side SiC MOSFET is driven at -4V for VGS, representing a typical hard switching test for the transistor and its body diode. The FUL SC event is performed on the Low-Side SiC MOSFET, the High-Side SiC MOSFET is driven with a commercial GD with $V_{GS} = -4V/15V$. For both experiments, the Low-Side SiC MOSFET is also driven by the designed CMOS GD. Under FUL, Fig. 10. shows a detection time of 360ns (flag is high), corresponding to a SC SiC I_{drain} of 570A at the detection time which is 27% greater than the nominal current of the DUT. The detection flag is not looped back and the PWM signal is intended to be cleared after the rising of the flag. The soft shut down is realized by the High-Side GD driven by the FPGA which generates the PWM signal. These results demonstrate the speed of the SC detection method without the need of an external DSAT high voltage diode.

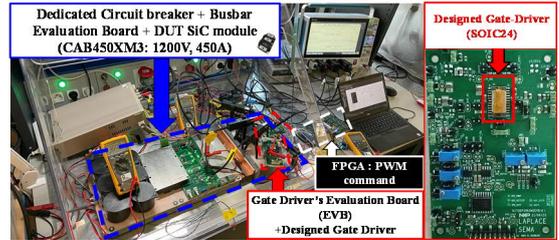


Fig. 8. (Left) Double-Pulse Test and Short-Circuit Test bench, (Right) Gate driver's EVB_{designed} with the Designed GD

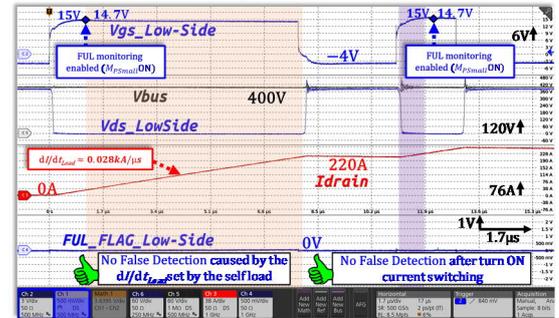


Fig. 9. Double-pulse test with CREE SiC module (CAB450XM3: 1.2kV, 450A): $V_{Bus} = 400V$, $R_{GHLowSide} = R_{GLLowSide} = 1\Omega$, $R_{PullDown} = 5$ k Ω , $V_{gsHighSide} = -5V$, $dI/dt_{Load} = 0.028$ kA. μs^{-1}

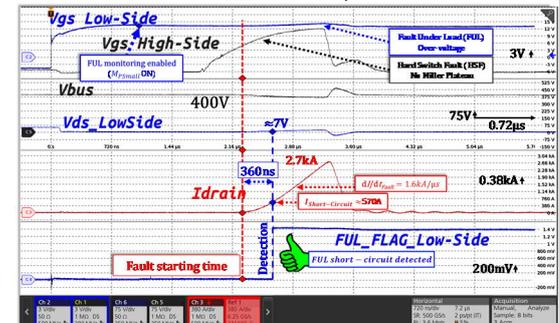


Fig. 10. Internal FUL with CREE SiC module (CAB450XM3: 1.2kV, 450A): $V_{Bus} = 400V$, $R_{GHLowSide} = R_{GLLowSide} = 1\Omega$, $R_{GHighSide} = R_{GLHighSide} = 12\Omega$, $R_{PullDown} = 5$ k Ω , $dI/dt_{Fault} = 1.6$ kA. μs^{-1}

V. ANALYTICAL MODELING, SIMULATION AND EXPERIMENTAL SYNTHESIS

Fig. 11 illustrates experimental SC detections by the designed GD under varied di/dt_{Fault} [0.8kA/μs; 2.7kA/μs], achieved by adjusting the bus voltage. The experiment is repeated for two different current reference values (I_{Ref} {1;0.6}mA) generated externally (Fig. 5). In these experiments, we targeted Internal Hard FUL SC cases (di/dt_{Faults} = [2 ; 3] kA/μs), External Hard FUL SC cases ([1; 2] kA/μs) and External Soft FUL SC cases ([0.5; 1] kA/μs). Fig. 10 also illustrates experimental results closely aligning with simulation and analytical model results. Observations highlight that higher di/dt_{Faults} result in faster SC detections at approximately the same I_{drain} values. The second observation is decreasing the current reference leads to faster SC detection, as expected.

To understand the proposed analytical model, we will first examine the GD circuitry, gradually simplifying it to create an easily understandable circuit representing the impact of the FUL SC. Fig. 12.a illustrates the GD alongside its external parameters and the SiC MOSFET with its internal parameters. Within the GD after fully charging the power device, only M_{Psmall} is activated, possessing an on resistance significantly greater than both the external gate resistance and the internal gate resistance of the SiC MOSFET module by at least two orders of magnitude ($R_{DsonMPsmall} \gg R_{gint}$ and R_{GH}). Additionally, it's crucial to note that the pull-down resistor surpasses $R_{DsonMPsmall}$, R_{gint} and R_{GH} by at least one order of magnitude. Given these considerations, the equivalent circuit is depicted in Fig. 12.b. Further simplification (Fig. 12.c) is achieved by recognizing that our analysis window is much smaller than the time constant ($R_{DsonMPsmall} \times C_{gs} \gg 500ns$). Consequently, we arrive at an equivalent circuit representing a variable current source, which emulates the current generated by C_{gd} charging C_{gs} . In the steady state, prior to the occurrence of the FUL SC, the potential $V(Gext)$ equals the voltage supply of the GD (V_{DDH}) minus the voltage drop induced by $R_{DsonMPsmall}$ ($V_{Gext}(0)$). As previously discussed, the FUL SC leads to a ΔV_G , resulting from the current generated by C_{gd} (I_{Cgd}). The FUL detection system will detect the SC occurrence when the potential $V(Gext)$ reaches V_{DDH} , as outlined in Eq. 1. This condition signifies that M_{Psmall} is no longer sourcing any current. At this time, the FUL detection system will detect the absence of I_{gcopy} and activates the FUL flag. The detection time (t_{dec}) can be determined by extracting it from Eq. 3 and by using Eq. 4 & 5

$$V_{DDH} = V_{Gext}(t_{dec}) = V_{Gext}(0) + \Delta V_G(t = t_{dec}) \quad (1)$$

$$\frac{dV_{Gext}(t)}{dt} = \frac{C_{gdmax}}{C_{gdmax} + C_{gs}} \cdot \frac{dV_{DS}(t)}{dt} \quad (2)$$

$$\Delta V_G(t_{dec}) = \frac{C_{gdmax}}{C_{gdmax} + C_{gs}} \cdot V_{DS}(t_{dec}) \quad (3)$$

$$V_{DS}(t) = R_{DSON}(I_{drain}(t)) \cdot I_{drain}(t) \quad (4)$$

$$R_{DSON}(I_{drain}(t)) = 1 + K \cdot \frac{dI_{drain}}{dt} \cdot t \quad (5)$$

$$\text{with } I_{drain}(t) = \frac{dI_{drain}}{dt} \cdot t \text{ \& } \frac{dI_{drain}}{dt} = \text{Constant}_1 \text{ \& } K = \text{Constant}_2$$

$$t_{dec} = \sqrt{\frac{\Delta V_G}{\frac{C_{gdmax}}{C_{gdmax} + C_{gs}} \cdot R_{DSON} \cdot K \cdot \frac{dI_{drain}}{dt}} + \frac{1}{4 \cdot K^2 \cdot \frac{dI_{drain}}{dt}} - \frac{1}{2 \cdot K \cdot \frac{dI_{drain}}{dt}}} \quad (6)$$

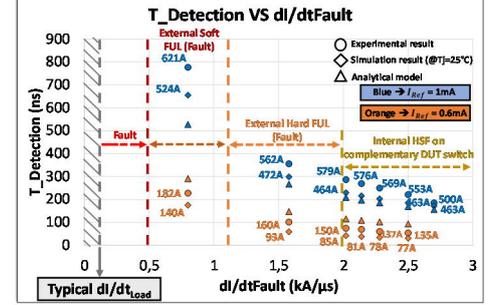


Fig. 11. Simulation, Experimental and Analytical results superimposition for SC detection for various di/dt_{Faults} set by the V_{Bus} (using CREE SiC module, CAB450XM3: 1.2kV, 450A): $R_{GHLowSide} = R_{GLLowSide} = 1\Omega$, $R_{GHHighSide} = R_{GLHighSide} = 12\Omega$, $R_{PullDown} = 5k\Omega$

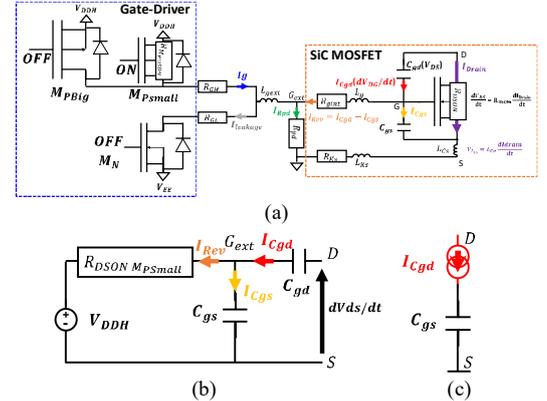


Fig. 12. Progression of Equivalent Circuit Simplification of the GD and the power device in a FUL case

VI. CONCLUSION

An integrated gate current copy, which is the ideal candidate for a fully integrated solution for a FUL detection is presented. This ultra-fast and robust technique senses indirectly the drain current variation indirectly via the gate drain capacitance. Through a novel GD architecture featuring segmented output transistors, we demonstrate improved gate current copy accuracy. Validation experiments conducted on automotive 1200V 450A SiC power module showcase the capability to detect FUL SC in less than 100 ns at drain currents around 500A which is just 11% higher than the nominal current of the power device and demonstrating no false detection in normal switching cases avoiding the use of a dedicated and costly sense-FET-current SiC die.

REFERENCES

- [1] J. Wang and X. Jiang, "Review and analysis of sic mosfets' ruggedness and reliability," IET Power Electronics, vol. 13, no. 3, pp. 445-455, 2020.
- [2] J. Xue, Z. Xin, H. Wang, P. C. Loh and F. Blaabjerg, "An Improved di/dt-RCD Detection for Short-Circuit Protection of SiC mosfet," in IEEE Transactions on Power Electronics, vol. 36, no. 1, pp. 12-17, Jan. 2021.
- [3] X. Liu, X. Li and T. Basler, "Short Circuit Type II and III Behavior of 1.2 kV Power SiC-MOSFETs," 2022 24th European Conference on Power Electronics and Applications (EPE'22), Germany, 2022, pp. 1-9.
- [4] A. El Boubkari et al., "CMOS Gate Driver with Integrated Ultra-Accurate and Fast Gate Charge Sensor for Robust and Ultra-Fast Short Circuit Detection of SiC power modules," 2023 35th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Hong Kong, 2023, pp. 68-71.
- [5] M. Picot-Digoix et al., "Quasi-Flying Gate Concept Used for Short-Circuit Detection on SiC Power MOSFETs Based on a Dual-Port Gate Driver," in IEEE Transactions on Power Electronics, vol. 38, no. 6, pp. 6934-6938, June 2023, patent: WO20240234.