Dynamic Analysis of RF CMOS Inverter-Based Ring Oscillators using an All-Region MOSFET Charge-Based Model in 28nm FD-SOI CMOS

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***Abstract*—Due to their continuous nature across all the inversion regions of MOS transistors, charge-based models are a promising analytical tool for preliminary design sizing that brings the advantages of simplicity and accuracy. These models allows for the efficient exploration of a design space while reducing the computational burden associated to complete compact models. In this paper, a method to analyze the dynamic and frequency performances of a single-ended inverter-based ring oscillators is presented. The proposed analysis is based on the time-domain evaluation of the loading currents, as well as of the input and output voltages of the ring oscillator's constituent inverters, using the Euler method. The novelty of this approach is the use of a 5-parameter charge-based model that considers short-channel effects. The proposed analysis is tested on a practical implementation in 28nm FD-SOI CMOS technology and the results, including the maximum achievable frequency and dynamic efficiency are compared to those obtained using the UTSOI2 model.**

***Index Terms*—Charge-based model, Euler method, inverter, ring oscillator, short-channel effects, 28nm FD-SOI CMOS**

I. Introduction

Charge-based models have been increasingly used in recent years. Their reduced number of parameters and their continuous nature across all inversion regions of MOSFET transistor operation make them well-suited for defining analytical design strategies. However, the use of such models, like ACM [1] or EKV [2], still appears to be limited to small-signal circuits [3] [4]. Recently, different flavors of these models accounting for short channel effects have been proposed [5] [6], opening the door to analysis of advanced technologies. The objective of this paper is to explore the feasibility of the direct application of these models to a large-signal transient analysis of inverter-based ring oscillators.

Numerous formulations exist regarding the frequency analysis of ring oscillators such as [7] or [8]. However, to our knowledge, none of them encompass the complete dynamic analysis of these circuits. Indeed, those analysis used characteristic working points of the composing inverters of the ring oscillator to determine its features. These features are directly linked with the shape of the loading currents and transient voltages across the different inverters composing the RO. Therefore, a more precise study of the dynamic behavior of the RO and the balance between PMOS and NMOS transistors composing the inverters is necessary.

This article aims to present a computational method based on a charge-based model with a reduced number of parameters, which enables an easy exploration of the design space, particularly at lower supply voltages. The goal of this analysis is not to replace the use of the complete compact models implemented by the foundries in the Design Kits (DK) of a given technology, but to offer designers a simpler and intuitive approach for preliminary sizing to avoid intensive blind simulation campaigns. Indeed, due to the simplicity of design-oriented charge-based models, this is achieved by establishing links between model's physical parameters with circuits' metrics.

The rest of the paper is structured as follows. Section II presents a 5-parameter version of the ACM model. Section III describes the proposed methodology for the dynamic analysis of both the CMOS inverter and the single-ended ring oscillator. Section IV validates the proposed methodology on a practical case study implemented in STMicroelectronics 28 nm FD-SOI CMOS technology. Obtained results are compared to simulations using the foundry's UTSOI2 models included in the DK of the technology. Finally, section V summarizes the overall paper contribution.

II. 5-Parameter Charge-Based Model

The aim of this section is to present the transistor-level charge-based model used for the computational analysis presented in section III. Firstly, the different physical parameters of the model are presented, followed by the model equations.

A. Parameters Overview

As previously mentioned, different charge-based models have been proposed such as the ACM or the EKV model. This work utilizes a 5-parameter version of the ACM model presented in [5]. The 5-parameter ACM (in the following, 5PM ACM) employed here includes the three classical long-channel parameters: the sub-threshold slope factor n, the equilibrium threshold voltage V_{T0} and the specific current I_{S0}. Additionally, two short-channel parameters are included: the dimensionless drain-induced barrier lowering (DIBL) effect factor σ, which leads to a reduction of the carrier's barrier potential occurring at the source side as the drain voltage

increases; and the carrier velocity saturation effect parameter ζ which is also a dimensionless parameter defined as

$$\zeta = \frac{\mu U_T}{L} \cdot \frac{1}{\nu_{sat}}, \tag{1}$$

where μ is the effective mobility of the carriers, $U_T = k_B T/q$ is the thermal voltage, L is the transistor length, v_{sat} is the saturation velocity of the carriers, k_B the Boltzmann constant, T the temperature, and q the elementary charge.

It is important to note that all these parameters can be extracted physically from measurements or simulations. The extraction procedure is summarized in [9] and [6]. For this study, MOSFETs with a length of $L = 60\,\text{nm}$, $90\,\text{nm}$, and respectively $120\,\text{nm}$ are used. The sets of parameters presented in Table I have been extracted following the guidelines in [6] for both NMOS and PMOS transistors in the 28 nm FD-SOI CMOS technology. It should be noted that we have defined a normalized specific current $I_{S0_{norm}} = \frac{I_{S0}}{W}$, presented in Table I. The specific current is the only parameter that has a dependence with the width of the transistor. Furthermore, as it will be shown, this normalization simplifies the exploration of the design space, particularly for delay analysis of the CMOS inverter and the associated study of the width balance between the PMOS and NMOS transistors.

TABLE I
ACM 5PM MODEL PARAMETERS OBTAINED THROUGH EXTRACTION FOR LVTNFET AND LVTPFET WITH LENGTHS OF L = 60 nm, 90 nm, AND 120 nm, IN 28nm FD-SOI TECHNOLOGY (MEASUREMENT UNIT: $I_{S0_{norm}}$ $(\mu A/\mu m)$ AND V_{T0} (mV)).

L		n	$I_{S0_{norm}}$	V_{T0}	σ	ζ
60	NMOS	1.18	2.78	390.4	0.0233	0.044
	PMOS	1.207	0.703	420.9	0.0328	0.022
90	NMOS	1.13	2.02	401.6	0.0134	0.035
	PMOS	1.15	0.586	440.5	0.0171	0.0205
120	NMOS	1.12	1.58	408.8	0.01	0.03
	PMOS	1.135	0.5	449.5	0.0117	0.0197

B. Model Formulation

The model is based on the normalized inversion charge ratios at the source q_S and drain q_D sides of the transistor, defined as

$$q_{S(D)} = \frac{Q_{S(D)}}{Q_P}, \tag{2}$$

where, $Q_{S(D)}$ represents the inversion charge density at the source (respectively drain) side and Q_P the pinch-off charge per unit area defined as

$$Q_P = \pm n C'_{ox} U_T, \tag{3}$$

where, C'_{ox} is the oxide capacitance per unit area. The plus sign refers to a n-channel transistor whereas the minus one indicates a p-channel transistor.

As presented in [5], a modulated normalized source (respectively drain) inversion charge ratios to consider the carrier's velocity saturation, these charges are defined as

$$q'_{S(D)} = q_{S(D)} - q_{sat}, \tag{4}$$

where, q_{sat} represents the normalized saturation drain charge ratio and is related to the normalized saturated drain current by

$$i_{Dsat} = \frac{2}{\zeta} q_{sat}. \tag{5}$$

The unified charge-control model (UCCM) is then applied to the previously defined modulated charges, leading to:

$$\frac{V_P - V_{S(D)B}}{U_T} = q'_{S(D)} - 1 + \ln\left(q'_{S(D)}\right), \tag{6}$$

where, V_P is the normalized pinch-off voltage approximated as

$$V_P \approx \frac{V_{GB} - V_{T0} + \sigma\left(V_{DB} + V_{SB}\right)}{n}. \tag{7}$$

Equations (5) and (6) leads to the following formulation of the normalized saturation drain charge ratio:

$$q_{sat} = \frac{\zeta}{2}\left[\left(q'_S + 1\right)^2 - 1\right]. \tag{8}$$

The modulated normalized source (respectively drain) inversion charge ratios are then computed to evaluate the drain current defined as

$$I_D = I_{S0} \cdot \frac{\left(q_S - q_D\right)\left(q_S + q_D + 2\right)}{1 + \zeta\left(q_S - q_D\right)}, \tag{9}$$

where the specific current I_{S0} is defined as

$$I_{S0} = \mu n C'_{ox} \frac{U_T^2}{2} \frac{W}{L_{eff}}, \tag{10}$$

where, W represents the width of the transistor and L_{eff} its effective or electrical length.

III. Inverter and Single-Ended RO Analysis

This section presents the proposed methodology for the dynamic analysis of a CMOS inverter, which is then extended to a single-ended inverter-based ring oscillator. This methodology is based on the Euler method, which is applied to calculate the loading current and transient voltages of inverters.

A. Inverter Study

Using the continuous nature of charge-based model across all operating regions of the transistor, the exploration of design space such as at very low supply voltage is easily feasible.

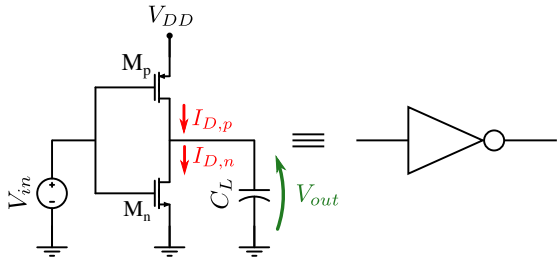

Fig. 1. CMOS Inverter.

The propagation time τ between two output voltage levels V_A and V_B during a single transition is defined as

$$\tau = \int_{V_A}^{V_B} \frac{C_L}{I_L} dV_{out}, \tag{11}$$

where,

$$I_L = I_{D,p} - I_{D,n}, \tag{12}$$

and where, as shown in Fig. 1, C_L is the load capacitance at the output of the inverter, I_L is the current passing through the load capacitance, $I_{D,p}$ (respectively $I_{D,n}$) is the drain current of the PMOS (respectively NMOS) transistor composing the inverter, and V_{out} the voltage across C_L.

Because of the transcendental nature of (6), the Euler method is used to numerically solve the integral in (11). Thus, the transient evolution of the drain current is approximated by dividing the evaluation time into a number of sufficiently small time steps and approximating the evolution of the current flowing through the load capacitance within each time step by a first order Taylor expansion. By repeating this procedure, the temporal behavior of the inverter during one transition is obtained, enabling the computation of the propagation time.

B. Single-Ended Ring Oscillator Study

The dynamic analysis presented in the previous subsection can be utilized to compute the transient behavior of inverter-based circuits. In this paper, the transient behavior of a single-ended inverter-based ring oscillator (presented in Fig. 2) which is composed of N inverters, where N is an odd number, is analyzed.

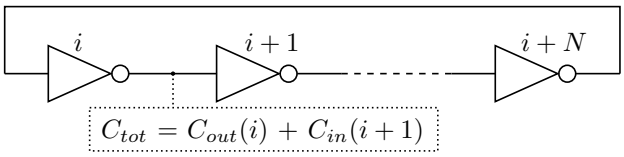

Fig. 2. Single-Ended Ring Oscillator.

To determine the ring oscillator frequency, the parasitic capacitances of each transistor should be considered. Using Miller's theorem and the analysis from [10], the value of each equivalent capacitance between every inverter is defined as

$$C_{tot} = 4 \cdot (C_{GD,p} + C_{GD,n}) + C_{DB,p} + C_{DB,n} + C_{ext}. \tag{13}$$

$C_{GD,p}$ (respectively $C_{GD,n}$) represents the intrinsic part of the gate-to-drain capacitance of the PMOS (respectively the NMOS) transistor, and $C_{DB,p}$ (respectively $C_{DB,n}$) represents the intrinsic part of the drain-to-bulk capacitance of the PMOS (respectively the NMOS) transistor. These intrinsic parts are functions of the terminal voltages as well as the geometry of the transistors and are computed using the equations proposed in [11]. On the other hand, C_{ext} represents the extrinsic parts, and their dependence on the voltages is negligible. However, they are dependent on the geometry of the transistors. Thus, a numerical $W \cdot L$-based scaling law has been extracted from the UTSOI2 model. From [12], the intrinsic parts are defined as

$$C_{GD,p(n)} = \left(1 - \frac{\sigma_{p(n)}}{n_{p,(n)}}\right) C_{GD0,p(n)} - \frac{\sigma_{p(n)}}{n_{p,(n)}} C_{GS0,p(n)}, \tag{14}$$

and,

$$C_{DB,p(n)} = \left(n_{p,(n)} - 1\right) C_{GD,p(n)}, \tag{15}$$

where,

$$C_{GD0,p(n)} = \frac{2}{3} C_{ox,p(n)} \frac{\alpha_{p(n)}^2 + 2\alpha_{p(n)}}{\left(1 + \alpha_{p(n)}\right)^2} \frac{q_{D,p(n)}}{1 + q_{D,p(n)}}, \tag{16}$$

and,

$$C_{GS0,p(n)} = \frac{2}{3} C_{ox,p(n)} \frac{1 + 2\alpha_{p(n)}}{\left(1 + \alpha_{p(n)}\right)^2} \frac{q_{S,p(n)}}{1 + q_{S,p(n)}}, \tag{17}$$

where,

$$\alpha_{p(n)} = \frac{1 + q_{D,p(n)}}{1 + q_{S,p(n)}}, \tag{18}$$

and, $C_{ox,p(n)} = C'_{ox,p(n)} \cdot W_{p(n)} \cdot L$ represents the oxide capacitance of the PMOS (respectively NMOS) transistor.

IV. Results and Discussions

The proposed methodology can be used to explore the design space of inverter-based circuits easily and accurately. In this regard, firstly, we will show how the ACM model enables the exploration the design space to efficiently balance both the rising and falling times of a CMOS inverter. Secondly, the proposed methodology will be used to explore the frequency and dynamic efficiency of a single-ended ring oscillator in a wide range of power supply voltages. To verify the feasibility of the approach, results are compared to UTSOI2 simulation.

A. Time Delay Analysis

Numerical L-based scaling laws using a polynomial regression were extracted for the parameters presented in section II by performing several simulation-based extractions of LVT NMOS and LVT PMOS with different transistor lengths ranging from 30 nm to 150 nm using 28 nm FD-SOI CMOS technology. Using these scaling laws, the rising t_r and falling t_f times of a single CMOS inverter are computed as a function of L and $k = W_p/W_n$. The rising and falling times are defined as the time throughout a transition from 10% to 90% of V_{DD}. To achieve minimum and equal falling and rising times, the studies conducted on 28 nm FD-SOI CMOS from [13] have been used, fixing the NMOS width to $W_n = 0.35\,\mu$m. For a power supply voltage of $V_{DD} = 0.75$ V, the ratio t_r/t_f is presented in Fig. 3. It shows that depending on L, the equilibrium point between t_r and t_f is reached for different k.

Fig. 3 demonstrates that the ACM charge-based model applied to the previously presented analysis provides the capability to explore a wide design space while considering just a reduced number of parameters. Moreover this study can be conducted for different power supply and the width of the NMOS transistor can be fixed to different values. It offers designers the possibility to find balanced rising and falling times in inverter-based circuits and simplify the pre-sizing approach during design. The same analysis will now be applied to study various characteristics of a single-ended ring oscillator.

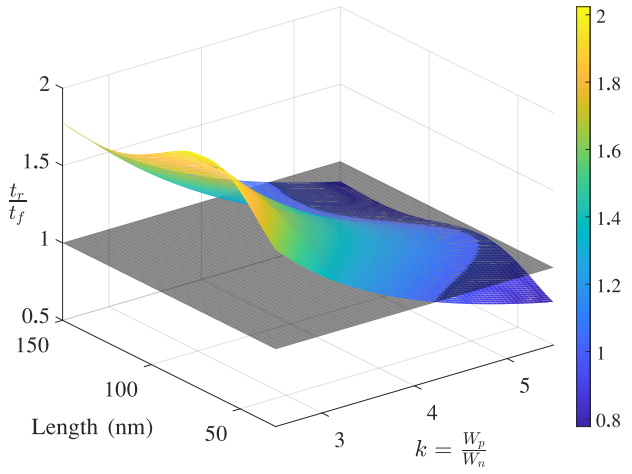

Fig. 3. Evolution of the ratio of the rising over falling times for $L \in [30\ nm, 150\ nm]$ and $k = \frac{W_p}{W_n} \in [2.5, 5.5]$ in 28nm FD-SOI CMOS technology for $W_n = 0.35\ \mu m$ and $V_{DD} = 0.75\ V$.

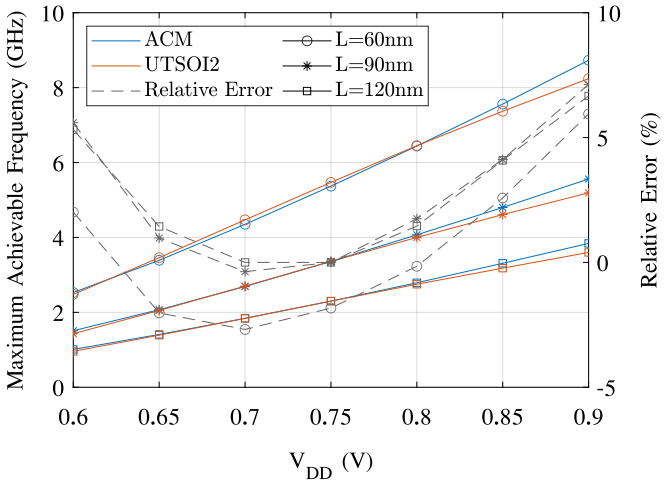

Fig. 4. Model comparison (ACM and UTSOI2) of the maximum achievable frequency for a SERO of $N = 5$ stages with $L_p = L_n = 60\ nm$, $90\ nm$, and $120\ nm$, $W_n = 0.35\ \mu m$, and $W_p = 1.18\ \mu m$, $1.31\ \mu m$, and $1.38\ \mu m$ in 28nm FD-SOI CMOS technology.

B. Supply Voltage Consideration

To evaluate the accuracy of the presented analysis, a single-ended ring oscillator consisting of $N = 5$ CMOS inverters was simulated using the ACM charge-based model and the UTSOI2 model. A set of three different lengths (60, 90, and 120 nm) was simulated using the parameters presented in Table I obtained from the numerical L-based scaling laws. The model's precision regarding the oscillator frequency (Fig. 4) and its dynamic efficiency defined as $\eta_{dyn} = f_{osc}/P_{dyn}$ (Fig. 5) over a range of supply voltages ranging from $V_{DD} = 0.6\,\text{V}$ to $V_{DD} = 0.9\,\text{V}$ is evaluated. It is noteworthy that no physical capacitors were used between the different stages of the ring oscillator, and only the MOSFET's parasitic capacitances were considered. The intrinsic part of these capacitances were dynamically computed using the equations presented in Section III-B. A numerical $W \cdot L$-based scaling law has been extracted from the UTSOI2 model to complete the study.

Fig. 4 and 5 demonstrate that the proposed dynamic analysis conducted with the 5-parameter ACM model exhibits high accuracy compared to the simulation of the circuit using the UTSOI2 model. We can hypothesize that the precision loss observed at high V_{DD} regarding the maximum achievable frequency is mainly due to the non-inclusion of the mobility reduction factor parameter presented in [6] in the study. This hypothesis is reinforced by the results of Fig. 5 at higher V_{DD} as well. On the other hand, we explained the lack of dynamic power consumption at lower V_{DD} because of the non-inclusion of short-circuit power consumption in our model. Nonetheless, these results suggest that the proposed analysis can be used for a first approach to the design of large-signal circuits, such as frequency synthesizers.

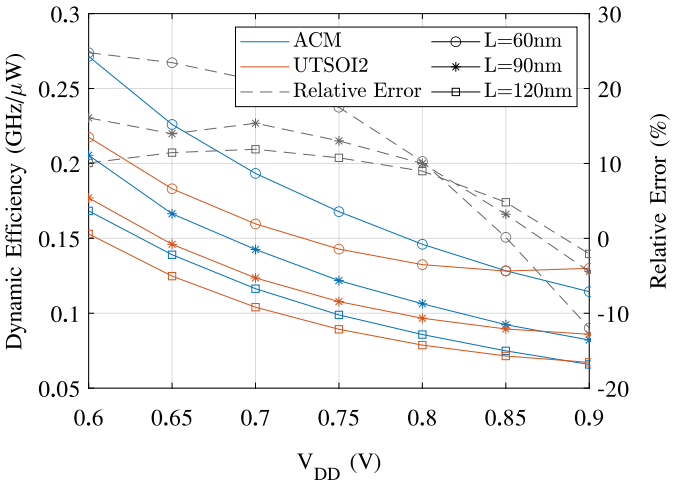

Fig. 5. Model comparison (ACM and UTSOI2) of the dynamic efficiency for a SERO of $N = 5$ stages with $L_p = L_n = 60\ nm$, $90\ nm$, and $120\ nm$, $W_n = 0.35\ \mu m$, and $W_p = 1.18\ \mu m$, $1.31\ \mu m$, and $1.38\ \mu m$ in 28nm FD-SOI CMOS technology.

V. Conclusion

This paper presents a dynamic analysis of a single-ended ring oscillator based on a 5-parameter design-oriented charge-based model and a numerical transient analysis. The proposed design-oriented analysis has been validated on practical implementations of CMOS inverters and ring oscillators in STMicroelectronics 28 nm FD-SOI CMOS technology. Obtained results show that the proposed strategy offers a good accuracy regarding the oscillation frequency and dynamic efficiency of the ring oscillator when compared to the industry-standard FD-SOI UTSOI2 model.

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