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Wideband Tunable N-Path Mixer With Calibrated Harmonic Rejection Including the 7th LO Harmonic

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Abstract—In this study, a harmonic-rejection N-path mixer is designed, implemented, calibrated, and measured. The proposed mixer features a wide bandwidth suitable for low-power multi-standard RF front-end receivers while keeping low complexity by opting for only 5 paths rather than 10 and only one stage to perform harmonic rejection up to the 7th local oscillator (LO) harmonic. This work employs a calibration strategy to prevent mismatches due to the fabrication process from affecting the system performance. The 0.17-1.2-GHz RF front-end mixer is fabricated in a 28-nm FDSOI technology. Measurements show a harmonic rejection higher than 45 dB for the 3rd, 5th, and 7th LO harmonics, 13 dB gain, 13.3 dB NF, -3.5 dBm in-band IIP3. The total power consumption is only 22 mW for a surface area of $0.62 \times 0.22 \text{ mm}^2$.

Index Terms—Harmonic rejection, harmonic rejection ratio, wideband RF front-end, harmonic rejection N-path mixer, software-defined radio, radio frequency amplifier, multi-standard receivers, passive mixer, low power, fully-depleted silicon on insulator.

I. INTRODUCTION

THE modern advances in computing technologies including digital signal processing, radio frequency hardware design, and modern communication systems opened the door towards a multitude of applications for the internet of things, wireless remote control, mobile data transfer, and high-speed communications. In order to address the wide variety of applications one may encounter in everyday life, a multitude of standards appeared addressing different distances, energy requirements, and frequency bands, leading step-by-step to a multi-standard IoT context. As a consequence, many researches investigated wideband architecture reconfigurability worldwide. Table I summarizes the allocated frequency bands for some usual standards showing some typical requirements for reconfigurability ranging between 0.38 GHz and 2.48 GHz.

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TABLE I: Frequency bands addressed by various standards

Standard	Owner	Frequency (MHz)
Zigbee	Zigbee Alliance	868-868.6 (Europe) 902-928 (US) 2400-2483.5 (Global)
T-GSM	GSM	380 / 410 / 810 / 900
Z-Wave	Sigma Designs	868.4 (Europe) 908.42 (US))
LTE-M	GSMA Carriers	450-2350 (uplink)
Lo-RaWan	LoRa Alliance	433.868 (Europe) 915 (US) 470 (China)
IEEE 802.11af	Open-IEEE Certified	470-710 (Digital Dividend)
IEEE 802.11ah	Open-IEEE Certified	850 (Europe) 900 (US) 700 (China)
IEEE 802.15.4	Open-IEEE Certified	868.3 (Europe) 902 (US) 2400 (China)

In radio communication, the implementation of multi-standard receivers can be achieved through different approaches, involving both software and hardware intervention. From a software point of view, the Software-Defined Radio (SDR) is a commonly used solution since one of its most important features is tunability. Following this software approach, the receiver can be reconfigured or updated to support new communication standards through software updates. This significantly reduces the need for hardware changes and can extend the device lifespan in a rapidly evolving wireless communication landscape. Meanwhile, the software approach is reduced by the availability of hardware to support a wide range of frequency bands.

Solid-state approaches are three-fold. First, the use of narrowband multiple parallel sub-receivers, such that each RF path is dedicated to one specific standard, consumes much power and takes up a large area thus increasing the cost of fabrication [1], [2]. An alternative approach involves employing a distinct receiver equipped with a single data processor capable of encompassing a broad spectrum of frequencies, facilitating the reception of diverse frequency ranges. Hence, the employment of a wideband receiver emerges as an evident solution, as stated by [3]. Numerous instances of wideband receivers have been documented in the literature, including

those designed for wideband TV reception [4], [5], ultra-wideband reception [6], [7], and even SDR applications [8], [9]. Third, solutions with tunable frequency band capabilities are very promising and could lead to a simplified architecture with a lower number of parallel receivers in the RF front-end. In particular N-path receivers or filters/mixers [10] [11], inherently tunable, are excellent candidates. This paper aims to explore performing architectures through calibration in the field of N-path mixing (NPM).

Furthermore, widely tunable or wideband, mixers accomplish the frequency translation by mixing the RF signal through switches controlled by a square wave at the local oscillator (LO) frequency that contains strong harmonic components. Due to this conversion, the interferers located around these LO harmonics will be as well down-converted to the baseband, hence generating unwanted signals at the same desired intermediate frequency (IF) [12] [13], thus degrading the signal-to-noise ratio (SNR) of the receiver as shown in Fig. 1.

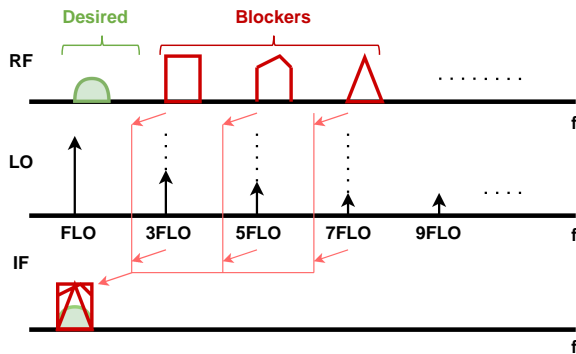


Fig. 1: LO harmonics folding in a wideband receiver.

To address this issue, the concept of harmonic rejection (HR) was introduced to reject LO harmonics [12] thus relaxing the frequency limitation for wideband applications. This objective can be achieved using either active mixers, usually based on Gilbert cells [5], or passive mixers, usually based on N-path [3], or both [14]. A key performance in a HR mixer is the harmonic rejection ratio referred to harmonic n (HRR_n). The HRR_n is defined as the power ratio between P_{IF} and $P_{IF,n}$, where P_{IF} is the IF power related to the down-conversion by LO of the RF signal and $P_{IF,n}$ is the IF power related to the down-conversion by LO n^{th} harmonic of the RF signal image close to $n\dot{L}O$ and presenting the same amplitude as its RF counterpart.

In [15], a harmonic rejection mixer was suggested for digital TV tuner applications, utilizing a conventional Gilbert cell with a switched load to reject the 3^{rd} and 5^{th} LO harmonics. It is worth mentioning that the achieved HRR falls below 40 dB, registering at 38 dB and 34.5 dB respectively. This level is relatively low when compared to the current state-of-the-art in harmonic rejection. Moreover, in [16], based on the Gilbert cell as well but with a modified differential multiple-gated transistor, a direct coupled HR mixer was proposed allowing to reject the 3^{rd} and 5^{th} LO harmonics with a HRR of 37.55 dB and 67.52 dB respectively. In parallel, passive mixers as HR-NPM appear to be excellent candidates to reject

the LO harmonics. They were introduced in several works for HR applications including [17] [18] and [19]. In [10], an LNTA-first harmonic rejection N-path mixer (HR-NPM) was proposed, where gm cells were scaled accurately to drive the mixer. However, for this architecture, one block was not enough to reject the odd harmonics but required the design of a second block in the baseband end. This echoes a more recent work, in [20], where a harmonic rejection approach was employed for reducing the 3^{rd} and 5^{th} harmonics thus achieving a $HRR > 51$ dB through two blocks, a harmonic rejection N-path mixer followed by a harmonic recombination which increased the complexity of the system. Another two-block technique is offered in [21] and [22] which implemented HR at the output of the LNA (18-37 dB) as the first block and in baseband (46-53 dB) as the second block. This system exhibits a notable power draw (≈ 54 mW). One technique has been proposed in [23] by adding interleaved inductors at the RF side, hence, allowing the operation of an 8-phase N-path mixer with 25% (rather than 12.5%) duty cycle clocks. However, not only do these inductors take up space on the chip but also allow rejecting the 3^{rd} harmonic only and not the 5^{th} .

This paper aims to propose an innovative, widely tunable mixer rejecting the even, 3^{rd} , 5^{th} and 7^{th} LO harmonics. Similar to the conventional HR-10PM architecture (Table II), our proposed architecture can reject harmonics up to the 8^{th} order. However, this improved version (HR-10PMeq) requires only three LNA gains, leading to lower power consumption; it also features a reduced number of switches, leading to less complexity. Compared to previous works, our system is compact, only one-block is needed to reach the desired HRR . To compensate for the absence of the harmonic recombination block, a calibration methodology within the specified frequency band is presented for the first time, aiming to optimize harmonic rejection and improve system performance.

The rest of the paper is organized as follows. Section II develops the concept of HR-NPM. Section III describes the working principle of the proposed HR-10PMeq and its circuit implementation. The calibration methodology is presented in Section IV. Section V provides the measurement results and a comparison with the state of the art. Finally, Section VI concludes this work.

II. HARMONIC REJECTION N-PATH MIXERS

A. Topology and Working Principle

Because of the mixing function between the two RF and LO signals, the idea behind harmonic rejection consists of synthesizing an effective LO signal, $eflo(t)$, having a reduced number of harmonics when compared to the conventional square duty cycle LO signal used in NPM [24], [25]. For this achievement, it is necessary to connect several parallel branches to the output capacitor path as illustrated on the general topology of HR-NPM architectures shown in Fig. 2. The latter consists of N paths, H gain stages each amplifying the RF signal through a gain G_h , and H branches where $H = N$ is a common choice. Each path is represented by a capacitor and made up of H switches driven by control signals $S_h(t)$.

TABLE II: NORMALIZED COEFFICIENTS FOR A SINE PERIOD FOR VARIOUS SAMPLING OF THE SINE WAVE OF FREQUENCY F_{LO}

H	H_r	H_g	S_w	G_1	G_2	G_3	G_4	G_5	G_6	G_7	G_8	G_9	G_{10}	G_{11}	G_{12}	G_{13}	G_{14}
5	3	2	20	1.62	1	-1	-1.62	0									
6	4	2	24	1	1	0	-1	-1	0								
7	5	3	42	1.82	2.26	1	-1	-2.26	-1.82	0							
8	6	3	48	1	1.41	1	0	-1	-1.41	-1	0						
9	7	4	72	2.67	4.09	3.59	1	-1	-3.59	-4.09	-2.67	0					
10	8	4	80	1	1.62	1.62	1	0	-1	-1.62	-1.62	-1	0				
11	9	5	110	2.71	4.61	5	3.82	1	-1	-3.82	-5	-4.61	-2.71	0			
12	10	5	120	1	1.72	2	1.72	1	0	-1	-1.72	-2	-1.72	-1	0		
13	11	6	156	1.94	3.41	4.12	3.88	2.76	1	-1	-2.76	-3.88	-4.12	-3.41	-1.94	0	
14	12	6	168	1	1.82	2.26	2.26	1.82	1	0	-1	-1.82	-2.26	-2.26	-1.82	-1	0

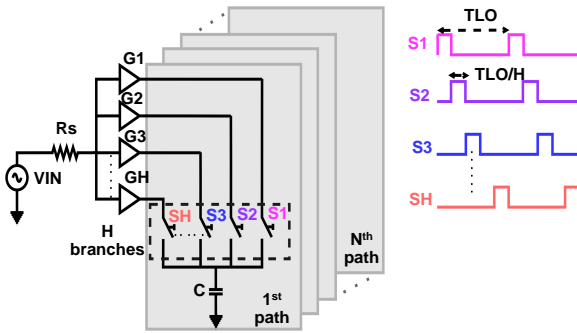


Fig. 2: Generic topology of HR-NPM.

The $eflo(t)$ applied to the mixer is based on a sine wave sampled at frequency $F_s = H \times F_{LO}$, which maximizes the number of zero coefficients, each coefficient corresponding to a dedicated gain during sampling. Sample h corresponds to gain G_h . Hence, the values of the gain coefficients have to be carefully controlled to reach the targeted harmonic rejection, noticing that coefficients set to zero do not need to be controlled. The computation is given by the following series defined for $1 \leq h \leq H$:

$$G_h = \frac{\sin \frac{2\pi h}{H}}{\sin \frac{2\pi}{H}} \quad (1)$$

For a given H ($H = N$), the normalized coefficients G_h are described in Table II, where H_r is the maximum rejected harmonic, H_g is the number of gain stages and S_w is the number of switches.

As $eflo(t)$ represents a sampled and held sine wave, it can be formulated using G_h as follows:

$$eflo(t) = \sum_{h=-\infty}^{\infty} G_h \delta(t - hT_s) \otimes g(t) \quad (2)$$

where $g(t)$ is the gate function of width $T_s = \frac{T_{LO}}{H}$ and amplitude 1.

The frequency domain equation of $eflo(t)$ is expressed by $EFLO(f)$ and is given below:

$$EFLO(f) = \frac{1}{2} \text{sinc}(\pi T_s f) \sum_{n=-\infty}^{\infty} \delta(f - nF_s \pm F_{LO}) \quad (3)$$

As presented in Fig. 3, the harmonics occur at $nF_s \pm F_{LO}$ and the first non-rejected harmonic is at $(H - 1)F_{LO}$.

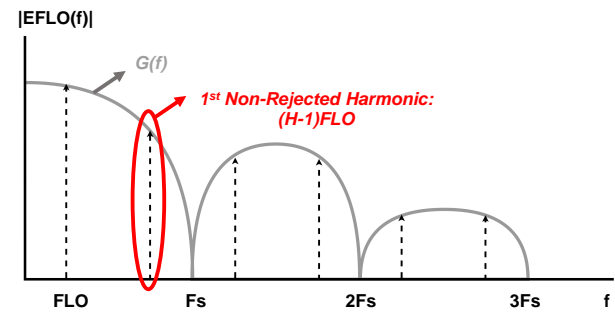


Fig. 3: Frequency response, $EFLO(f)$, of the effective LO, $eflo(t)$.

B. Complexity Analysis

The performance in terms of HR and selectivity are related to the number of samples, H , and the number of paths, N , respectively, whereas the complexity is related to the number of gain stages, H_g , and the number of switches, S_w . Conventional HR-NPMs are limited concerning the HR band. Usually, to reach higher HR, more gain stages are required, in other words, the system complexity increases with the targeted HR. According to Table II, the HR-8PM demonstrates HR band coverage up to the 6th harmonic while this achievement is accomplished with the utilization of 3 RF gains and 48 switches. However, the HR-10PM increases the HR band till the 8th harmonic, but it requires to increase the number of RF gains and switches to 4 and 80, respectively. The complexity increases with the HR band improvement, which leads to higher power consumption, more complex design, and more parasitic effects.

For this reason, the authors are proposing two figures of merit defined as:

$$\begin{aligned} \rho_1 &= \frac{H_r}{H_g}, \\ \rho_2 &= \frac{H_r}{S_w}, \end{aligned} \quad (4)$$

where H_r is the last rejected harmonic.

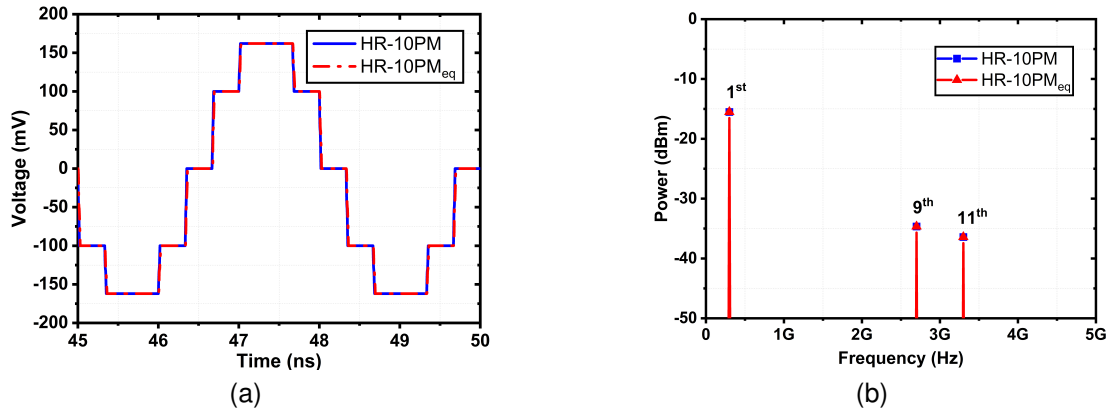


Fig. 4: The effective local oscillator signal for both conventional HR-10PM and the proposed HR-10PMeq in (a) time domain and (b) frequency domain.

A higher value of ρ_1 implies fewer gain stages required, leading to lower power consumption. Similarly, a higher value of ρ_2 implies fewer switches required, resulting in a smaller surface and lower complexity.

In this framework, it is noticeable to propose a system that allows the improvement of the HR band without increasing the system complexity and power consumption. In other words, a system that can reject up to the 8th just like the conventional HR-10PM with only 3 RF gains just like the conventional HR-8PM. To that end, authors propose to reduce the number of paths from 10 to 5, leading to an equivalent HR-10PM, the HR-10PMeq, at the expense of a slightly decreased frequency selectivity by a factor of 2 (10/5). See [26] for bandwidth formula depending on N . That way, there is no need for two differential gains of 1.62, but only one serving for all paths. The theoretical comparison between the conventional HR-10PM and the proposed HR-10PMeq is validated with cadence simulations. The time and the frequency domain representation of the $eflo(t)$ are given for these two structures in Fig. 4. As expected and aforementioned, both the HR-10PM and HR-10PMeq reject up till the 8th harmonic with the same power level of harmonics when similar conditions are applied for RF and LO.

III. PROPOSED HARMONIC REJECTION N-PATH MIXER

A. Architecture

As shown in the previous section, the HR-10PMeq is a simplified version of the conventional HR-10PM considering the complexity and the power consumption. Indeed, the main advantage of the architecture is the remarkable HR band without swelling the system complexity. Fig. 5 (a) shows the schematic illustration of this structure, it is composed of three differential RF amplifiers (RFAs) with voltage gain ratios [1:1.62:1]. Following the RFAs, there are 5 paths with a $2\pi/5$ phase shift between consecutive paths. Each path consists of 8 switches which are controlled by 10 clock phases denoted as S1 to S10, as shown in Fig. 5 (b).

The clock signals have a duty cycle of 1/10 and a consecutive delay of $T_{LO}/10$. This clock signals distribution associated

with gains is responsible for generating the $eflo(t)$ waveform presented in Fig. 4 (a) and its frequency response in Fig. 4 (b). The 3rd, 5th and 7th harmonics are totally rejected in these theoretical simulations with ideal elements, whereas the 1st harmonic occurs at the 9th order (2.7 GHz for $F_{LO} = 300$ MHz). As illustrated in Fig. 5, the symmetrical nature of the circuit, which is identified by the differential structure, limits the impact of mismatch and reduces the different parasitic effects coming from the wires, digital part, and so on. Hence, it ensures the rejection of the even-order harmonics.

B. Circuit Implementation

Fig. 6 shows a block diagram at the system level of the implemented HR-10PMeq. The designed functions include an active balun, three RFAs, a clock generator providing the 10 phases, and the 5-path mixer on a single chip. The active balun is responsible for transforming the single-ended signal into two balanced signals providing voltage gain in the meantime. The two main clock signals CLK and \overline{CLK} are derived from an external clock generator operating between 0.85 GHz and 6 GHz, and the RF input signal is derived from an external signal generator between 0.17 GHz and 1.2 GHz. The external trimmers are surface mounted on the testing PCB to control the biasing part of the amplification circuit. They have different specific functions that will be explained deeply later in this section.

1) *Balun and RF amplifier implementation:* The balun consists of the CG-CS topology shown in Fig. 7 (a). CG-CS amplifiers have the advantage of performing a single to differential conversion while, at the same time, synthesizing a low input real part which is useful for 50 Ω matching purposes for future measurements as is the case here.

In addition, the CG-CS amplifier achieves noise canceling that reduces the noise contribution of the CG stage to the overall noise which helps improve the performance of the mixer. Hence, the noise figure (NF) only depends on the CS transistor and the load resistances ($R_{L_{CG}}$ and $R_{L_{CS}}$). Whereas gm_{CS} is usually used to control NF, gm_{CG} is sized to achieve the targeted input resistance which can be

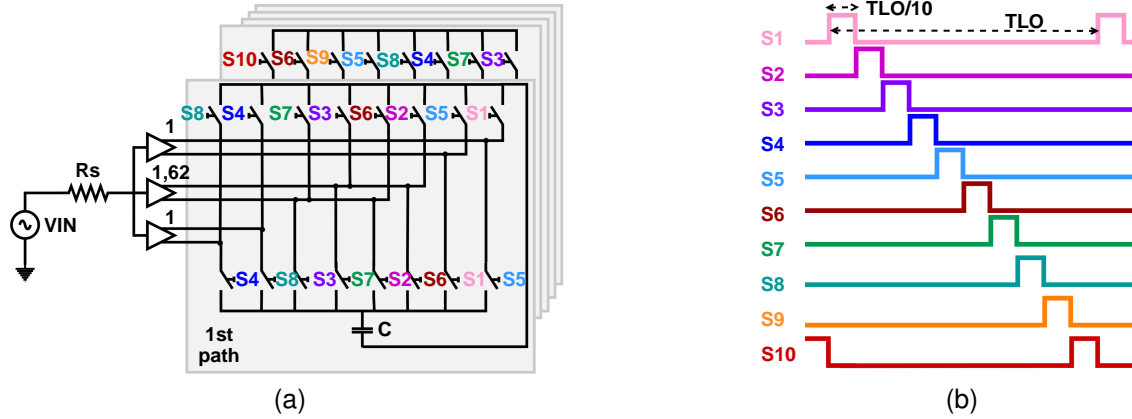


Fig. 5: Implemented HR-10PMeq architecture. (a) Schematic diagram of the RF amplifiers and the mixer per each path. (b) Chronograms of the clock signals driving the mixer.

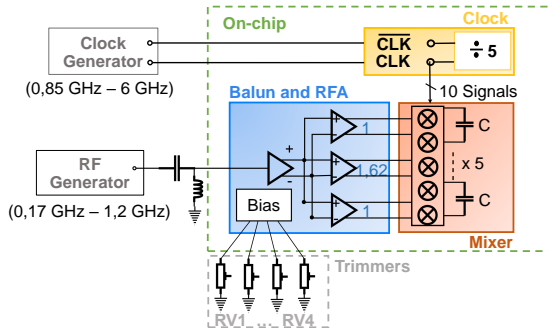


Fig. 6: Block diagram of the implemented HR-10PMeq.

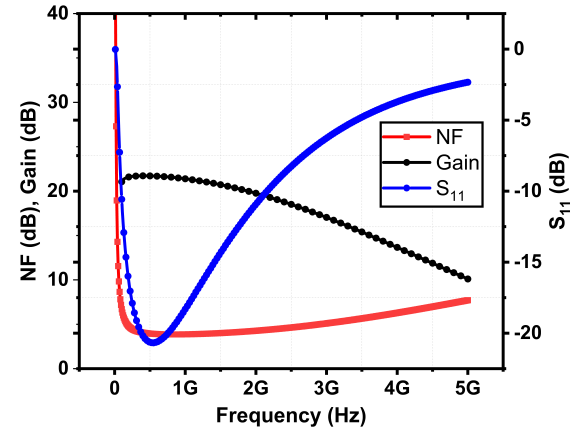


Fig. 8: The PLS results of the gain, NF, and matching of the amplifier block.

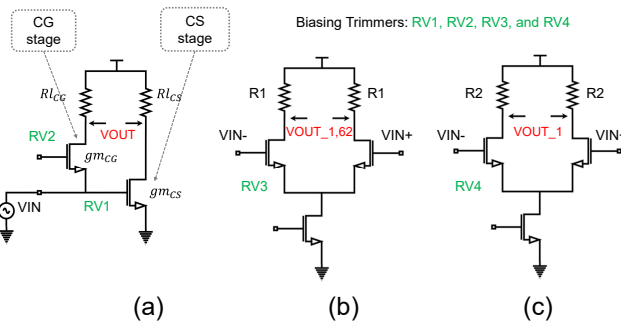


Fig. 7: (a) Balun. (b) RF amplifier stage with relative gain 1.62. (c) RF amplifier stage with relative gain 1 (this latter is replicated twice: two gains of 1).

approximated to $1/gm_{CG}$. Since the CG-CS behaves as an active balun, it is assumed that the two branches achieve the same gain ($G_{v_{CS}} = G_{v_{CG}}$) and that the gains are balanced with the loads Rl_{CG} and Rl_{CS} . The transconductances gm_{CS} and gm_{CG} being fixed, Rl_{CS} is used to set the gain and Rl_{CG} allows the differential gain to be balanced. Practically, to compensate for PVT variations, two tuning knobs $RV1$ and $RV2$ are used in our implementation to control the bias current of the CG and the CS stages, respectively. Hence, with $RV1$

it is possible to tune the S_{11} and, with $RV2$, to balance the differential output. The three RFA gains consist of differential pairs with resistive loads as in Fig. 7 (b) and Fig. 7 (c). They are used to implement the gain ratios of [1:1.62:1]. Since the HR performances are highly sensitive to gain values, the transconductances of the RFAs responsible for the 1 and 1.62 relative gain can be controlled with two tuning knobs $RV3$ and $RV4$ also implemented in the circuit.

Post-layout simulations of the whole amplifier block providing the ratio of 1.62, including the balun and the corresponding RFA, give a maximum gain of 22 dB for an input RF frequency around 300 MHz with a variation lower than 1 dB over the whole bandwidth as shown in Fig. 8. This block achieves a minimum NF of 4.8 dB around 1 GHz, with a maximum variation of 1.5 dB in the targeted bandwidth, 0.17-1.2 GHz, with matching better than 10 dB.

2) *Clock generation, LO phases:* In this framework, two 5-phase clock generators, based on Flip Flop Looped Shift Registers (FF-LSR), associated with logical combiners are used to generate the 10 phases with a 1/10 duty cycle. This method presents the advantage of needing an input master

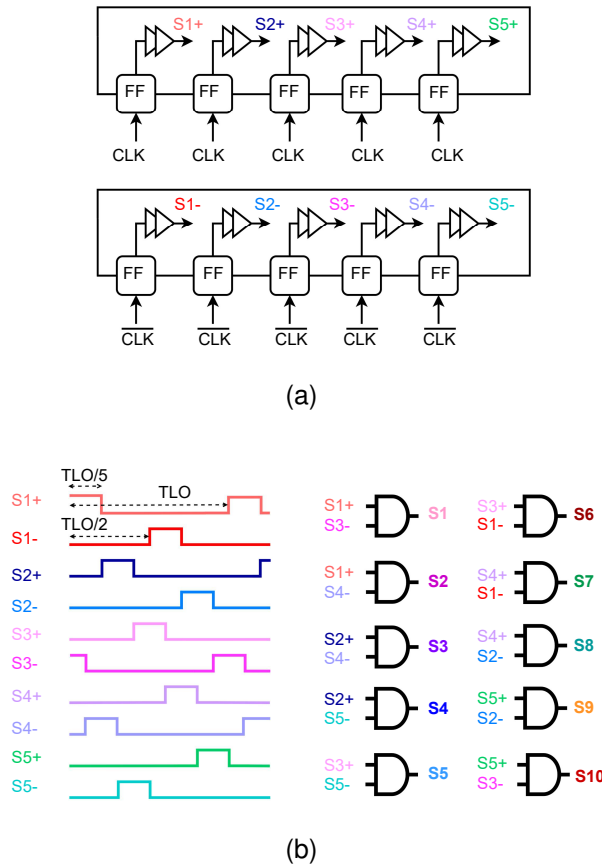


Fig. 9: Principle of clock signals generation. (a) Schematic diagram. (b) Chronograms.

clock frequency of only 5 times higher than the one required by the proposed system. The block diagram of the implemented generator of phases is illustrated in Fig. 9 (a). The FF-LSR are driven by 2 external clock signals: CLK and its complementary \overline{CLK} . The 10 output signals S_x^+ and S_x^- in Fig. 9 (b) are then combined using 10 AND logic gates to produce 10 clock signals from S1 to S10 at the LO frequency with a 1/10 duty cycle in Fig. 5 (b).

IV. CALIBRATION STRATEGY

A. Need for Calibration

The performance of the implemented HR-10PMeq architecture is evaluated in terms of the HRR . Indeed the main purpose of this work is to maximize the rejection of the harmonic components, including the 7th harmonic component. Unfortunately, the harmonic rejection principle relies on precise gain and phase ratios, while gain and phase mismatches can occur during the fabrication due to process variations, thus degrading the HRR . A gain mismatch can stem from the intricacies of the amplifiers; especially those tasked with synthesizing the gain ratio in complex HR systems. On the other hand, phase error, while also detrimental to overall system performance, can originate from multiple sources, including both the amplification and the clock generation systems. However, in practice, extensive research and empirical evidence have indicated that the clock generation system

tends to be the predominant source of phase errors. As such, meticulous attention must be devoted to the development and optimization of this crucial component to ensure precise timing and synchronization within the communication system.

The sensitivity of the HRR to both amplitude and phase errors has been partly considered in [9] and [27]. Meanwhile, the gain and phase mismatches impact the odd harmonics only, while the even harmonics are influenced by the differential mismatch exclusively. The relation between the HRR of the 3rd, 5th and 7th harmonics and these mismatches are given in the following equations as,

$$HRR_3 = \frac{\sin^2\left(\frac{3 \cdot 2\pi}{10}\right) \left(3\sigma_A^2 + 45\sigma_\phi^2\right)}{\left(3 \sin\left(\frac{2\pi}{10}\right)\right)^2 (4(G - 0.5)(G + 2))^2} \quad (5)$$

$$HRR_5 = \frac{\sin^2\left(\frac{5 \cdot 2\pi}{10}\right) (2\sigma_A^2)}{\left(5 \sin\left(\frac{2\pi}{10}\right)\right)^2 ((G - 0.5)(G + 2))^2} = 0 \quad (6)$$

$$HRR_7 = \frac{\sin^2\left(\frac{7 \cdot 2\pi}{10}\right) \left(3\sigma_A^2 + 45\sigma_\phi^2\right)}{\left(7 \sin\left(\frac{2\pi}{10}\right)\right)^2 (4(G - 0.5)(G + 2))^2} \quad (7)$$

where σ_A is the standard deviation of the gain in percentage and σ_ϕ is the standard deviation of phase error in radian. All these equations hold for:

$$G = \left(\frac{\sin\left(\frac{2\pi}{H}\right)}{\sin\left(\frac{2 \cdot 2\pi}{H}\right)}\right)^{-1} \approx 1.62 \quad \text{for } H = 10 \quad (8)$$

(6) shows that the 5th harmonic is consistently rejected with a very high rejection ratio (HRR_5 in dB would effectively tend to ∞), regardless of the gain and phase errors, demonstrating the robustness of this architecture to this harmonic. Regarding the 3rd and the 7th harmonics, the HRR degradation is plotted in Fig. 10 as a function of the gain and phase errors, respectively. It is observed that these two harmonics are highly sensitive to the gain and phase mismatches. A 1% gain error results in a notable 25 dB deterioration in both HRR_3 and HRR_7 , while a 1% phase error causes a 20 dB degradation.

The dramatic performance degradation in terms of HRR that is observed in Fig. 10 for a small variability of the gains and relative phases makes necessary a mitigation strategy for a robust system operation. Monte Carlo simulations at schematic level of the proposed circuitry show that σ_A can reach up to 10%, translating to a rejection of 38 dB for the 3rd harmonic and 46 dB for the 7th harmonic, as shown in Fig. 10 (a). Additionally, σ_ϕ can reach up to 2%, leading to a rejection of 40 dB according to Fig. 10 (b).

A direct practical solution would consist of reducing σ_A and σ_ϕ by design. However, this would lead to increasing the area and power budget dedicated to the gain stages and clock generation circuits. Instead of this, in this work, we have introduced a set of tuning knobs, labeled as RV1 to RV4 in Fig. 7, that, together with a dedicated calibration algorithm, allow us to compensate for the degradation of HRR due to process and mismatch variations.

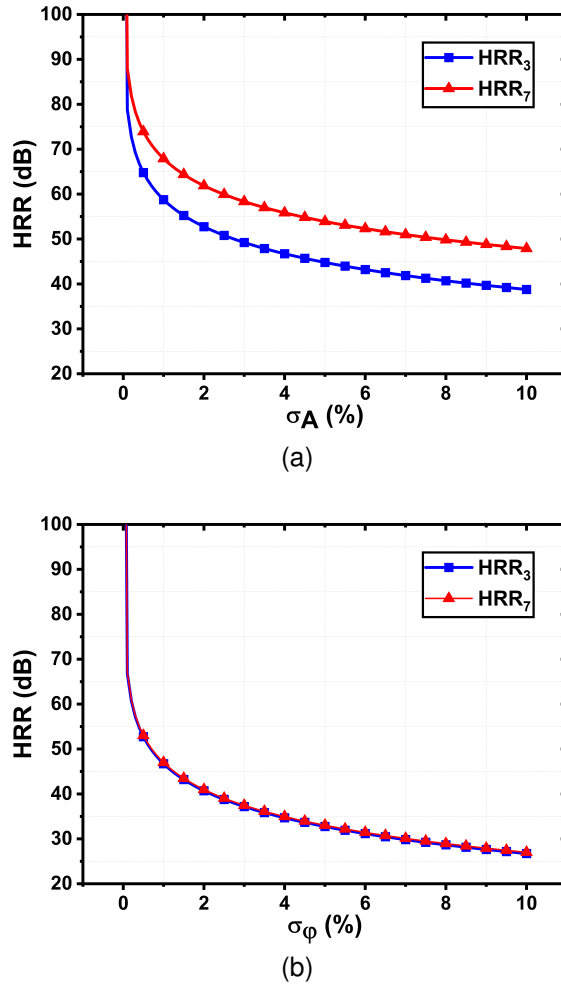


Fig. 10: HRR for the 3rd and 7th with respect to the (a) gain mismatch in % (for $\sigma_\phi = 0$) and (b) phase mismatch in % (for $\sigma_A = 0$).

B. Machine Learning-Based Calibration Algorithm

As explained in a previous section, the four implemented tuning knobs RV_1 to RV_4 allow compensating sample-to-sample process and mismatch variations by controlling the bias voltages of the balun and differential gain stages. In this regard, the goal of the calibration algorithm would be to find the combination of tuning knob values that maximizes HRR for each fabricated circuit sample. Formally, the problem can be expressed as a multi-objective optimization for maximizing function $F(RV_i)$, $i = 1, \dots, 4$ defined as,

$$F(RV_i) = \sum_{j=3,5,7} \alpha_j HRR_j, \quad (9)$$

where α_i are weighting factors, with the constraints,

$$\begin{aligned} RV_i &\in [RV_{i,min}, RV_{i,max}], \quad \forall i \\ HRR_j &> HRR_{j,min}, \quad \forall j \\ Gc &> Gc_{min}, \\ NF &< NF_{max}, \\ Pdc &< Pdc_{max}, \end{aligned} \quad (10)$$

where $RV_{i,min}$ and $RV_{i,max}$ are the minimum and maximum voltage values for tuning knob RV_i , respectively, and $HRR_{j,min}$, Gc_{min} , NF_{max} , and Pdc_{max} are the minimum target specifications for the system.

The standard approach to solving this problem relies on using an iterative test-and-tune calibration loop to explore the space of available tuning knob values. In each iteration of the calibration loop, the circuit is measured under a given set of tuning knobs conditions, the obtained performance is compared to the performance targets and, if necessary, a search algorithm is employed to propose a new set of tuning knob values for the next iteration of the calibration loop. Multiple algorithms are available to guide the iterative search, such as gradient descent, particle swarm optimization, genetic algorithms, etc. However, the process is lengthy and requires a large number of iterations, and hence multiple circuit measurements, to converge to a solution.

In this work, we propose a solution to reduce the number of necessary iterations and circuit measurements required for calibration. The proposed calibration algorithm employs a surrogate model of the circuit under calibration to directly evaluate the cost function (9), [28], [29]. This surrogate model is built at the same time that the algorithm explores the tuning-knob space and it is fine-tuned in each iteration of the algorithm. The calibration procedure can be detailed as follows. Once the optimization problem is defined in terms of design goals and constraints, the first iteration of the algorithm starts by defining a set of fixed values for the tuning knobs RV_i to roughly cover the search space (e.g., a usual starting point may be to consider the minimum, maximum and nominal values for each tuning knob). The performance of the circuit is then measured for each of the selected set of tuning knob positions. The resulting dataset, i.e., the employed values of RV_i and the corresponding circuit performance figures in terms of HRR_j , Gc , NF , and Pdc , is then employed to build a surrogate model $S(RV_i)$ of the circuit under calibration as,

$$S(RV_1, \dots, RV_4) = \{HRR_3, HRR_5, HRR_7, Gc, NF, Pdc\}. \quad (11)$$

In this work, we employ a simple perceptron neural network to build this surrogate model. The surrogate model is then employed to evaluate the cost function F in (9) and find the RV_i values that maximize it while complying with the constraints in (10). The surrogate model allows to approximate the complete tuning knob space while drastically limiting the number of required measurements. The iteration ends by actually measuring the performance of the circuit using the tuning knob combinations proposed by the algorithm and comparing the results to the surrogate model predictions and the optimization targets. If the actual performance is far from the predicted and target values, it means that the surrogate model does not approximate well the actual behavior of the circuit and needs to be refined in subsequent iterations. Then, the following iterations of the algorithm start by proposing new combinations of tuning knob values around the solution proposed in the previous iteration. Thus, the surrogate model accuracy is improved (as more data is made available for

the training of the regression functions), and a new search is then performed. The process continues until the algorithm converges to a solution compatible with the optimization targets.

V. EXPERIMENTAL RESULTS

The chip is fabricated in a 28-nm FDSOI process with an active area of $0.62 \times 0.22 \text{ mm}^2$, and it is packaged in a 44 QFN (see Fig. 11). A PCB has been designed to perform the measurements, which includes the chip with SMD decoupling capacitors to reduce noise, voltage fluctuations, and interference. As explained in the previous sections and shown in Fig. 6, four trimmers are also mounted on the testing board and tuned to adjust the voltage/current flow into the circuit. The fabricated chip of the HR-10PMeq is shown as well in Fig. 11 where different blocks are highlighted: the amplification stage including the balun and the RF amplifiers with a gain series [1:1.62:1], the 10-phase clock generator, the 5 capacitive paths with additional baseband buffers, and decoupling capacitors. The total power consumption of this circuit is 22.3 mW and it is provided per block in Table III where the amplifiers consume 88% of the whole consumption, and the remaining 12% is coming from the clock buffers knowing that the passive mixer itself consumes no power.

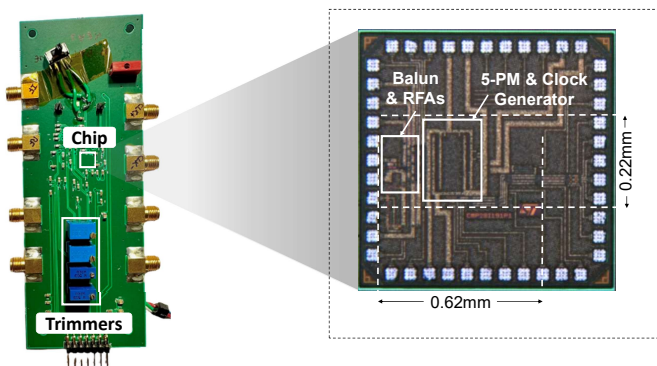


Fig. 11: Evaluation board photograph and the 28nm FDSOI fabricated chip indicating some functional blocks.

A. Measurement Setup

Fig. 12 represents the setup of the measurement bench. The VNA (ZNB40) is employed for calibrating the LNA in order to achieve optimal matching and minimum gain and

phase deviation errors as possible. The clock signals are generated from an external arbitrary wave generator (AWG-70000), while the RF input signal is provided from the RF generator (410A). The IF output signal is analyzed using a spectrum analyzer (RS@FSL18). The oscilloscope (54855A) is utilized to examine the clocks, phase error, input, and output waveforms.

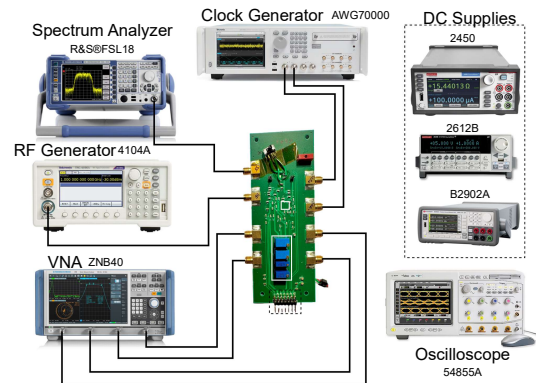


Fig. 12: Representation of the measurement setup.

B. Machine Learning-Based Circuit Calibration

The fabricated circuit has been calibrated for maximizing rejection of the 3rd, 5th, and 7th harmonic components by employing the machine learning-based calibration algorithm proposed in the previous section. The calibration algorithm has been experimentally implemented with the design goals and optimization constraints listed in Table IV.

The test setup for experimentally implementing the calibration loop includes a spectrum analyzer to measure the circuit performance and programmable DC sources to set the tuning knob voltages, while the learning algorithm runs in a dedicated computer. It can be pointed out that the whole calibration loop can be easily automated for production line calibration since both the spectrum analyzer and the programmable sources can be accessed and controlled by the computer running the calibration algorithm. Moreover, due to the inherent lightweight of the employed learning model, an integrated solution including the learning algorithm and dedicated DACs for tuning knob control could be also considered. Nevertheless, this is out of the scope of the present paper and will be considered for future extensions of this work.

The first iteration of the algorithm considers three different values for each of the tuning knobs (0 V, 0.42 V, and 1.04 V).

TABLE III: MEASURED POWER CONSUMPTION

Consumption (mW)	RFA	Mixer + CLK - Buff	Total
Measurement	19.6	2.7	22.3

TABLE IV: CALIBRATION GOALS

Specification	HRR_i $i = 3, 5, 7$	G_c	NF	Pdc
Target	maximize, > 45 dB	maximize, > 10 dB	minimize	minimize

The algorithm converges in the second iteration, where the surrogate model is fine-tuned by evaluating 10 additional tuning knob combinations around the first iteration solution.

The solution space predicted by the surrogate model after two iterations of the calibration algorithm is represented in Fig. 13. For a simple interpretation of this multidimensional space, Fig. 13 represents two-dimensional projections representing the harmonic rejection ratios versus the conversion gain. Interestingly, the algorithm predicts a single optimum value for the duplet $\{HRR_3, G_c\}$, while the maximum values of HRR_5 and HRR_7 can be achieved for any value of G_c in the considered variation range. These results are in line with the sensitivity analysis in (6), which shows that the rejection of the 5th harmonic component is robust against variations, while the rejection of the 3rd harmonic is the most sensitive to variations. The red star corresponds to the best trade-off solution compatible with the calibration goals in Table IV, maximizing at the same time harmonic rejection and conversion gain while keeping noise and power consumption contained, meaning that choosing the maximum conversion gain might not be the best compromise. The measurements reported in this section correspond to this calibration solution.

C. Harmonic Rejection, Gain, NF, and S_{11}

Following the calibration solution, a -30 dBm power signal is applied at the input of the HR-10PMEq system. The measurements consider an input frequency $f_{RF} = 305$ MHz and LO frequency $f_{LO} = 300$ MHz (after frequency division, with an external clock of 1.5 GHz). When operating with a different LO frequency, it is necessary to re-calibrate the HRR to reach the optimal values at this frequency. The HRR can be calculated by comparing the power difference, measured on a spectrum analyzer, obtained when the RF input signal is applied and when its n th harmonic image is applied. The best compromise with the calibration goals gives $HRR_3 = 48$ dB, $HRR_5 = 49$ dB, and $HRR_7 = 46$ dB. It is important to state that in the multidimensional space, higher values of HRR_7 may coincide with lower values of HRR_3 and HRR_5 , and vice versa, corresponding to a different set of tuning parameters.

Furthermore, the voltage conversion gain G_c of the circuit is measured over different intermediate frequencies (IF) and is shown in Fig. 14. The maximum gain is 13 dB and is achieved for $f_{IF} = 5$ MHz. This gain has a variation lower than 1 dB over the targeted bandwidth, and it reduces as the IF increases till it reaches <-30 dB for high IF. The NF is determined at $f_{RF} = 305$ MHz, yielding a double-sideband noise figure (DSB NF) of 13.3 dB. This value is constant within the whole RF range 0.17-1.2 GHz, as it is highly depending on the LNA contribution to NF, which shows no variation in this frequency range as illustrated in Fig. 8. The graph in Fig. 15 illustrates the measured S_{11} in comparison with the simulated results. Within the RF range 0.17-1.2 GHz, the measured S_{11} consistently registers below -15 dB.

D. Compression Point 1dB and Linearity IIP3

Fig. 16 shows the measured in-band (IB) IIP3 which gives -3.5 dBm. For this measurement, two RF tones are considered

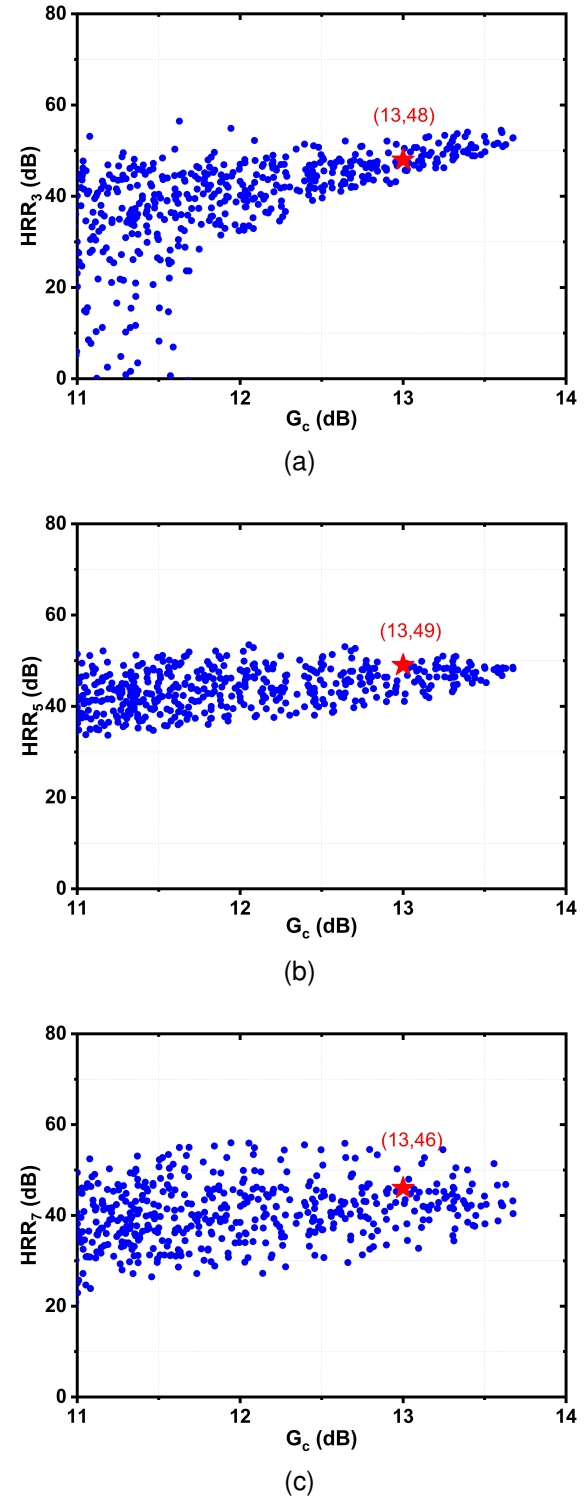


Fig. 13: Performance space corresponding to the measured (a) HRR_3 , (b) HRR_5 , and (c) HRR_7 versus G_c . Each data point corresponds to a tuning knob combination. Blue points correspond to surrogate model predictions. The red star corresponds to the predicted best trade-off solution for the considered design targets (G_c, HRR_n) .

at the input of the circuit in addition to the LO frequency. These two tones are chosen close to the LO frequency so

TABLE V: COMPARISON WITH STATE OF THE ART

Benchmark	Architecture	Frequency (MHz)	NF (dB)	Gc (dB)	Pdc (mW)	In-IIP3 (dBm)	HRR ₃ (dB)	HRR ₅ (dB)	HRR ₇ (dB)	$\rho_1 = \frac{H_r}{H_g}$	$\rho_2 = \frac{H_r}{S_w}$	Tech. node
[15] TCAS-I 2013	Gilbert mixer	48-862	15.7	4.5	10.8	8.2	38	34.5	-	-	-	180 μ m CMOS
[16] CEI 2022	Gilbert mixer	1-1000	9.5-12.87	1.458	11.2	16.21	37.55	67.52	-	-	-	180 μ m CMOS
[17] JSSC 2013	NPM	50-830	11*	12	67	5.4	72	71	67	0.38	0.07	130nm CMOS
[18] RFIC 2013	NPM	500-1500	35	8	17	-3	55	58	-	2	0.5	45nm SOI
This work	NPM	170-1200	13.3	13	22	-3.5	48	49	46	2.667	0.2667	28nm FDSOI

*DSB NF

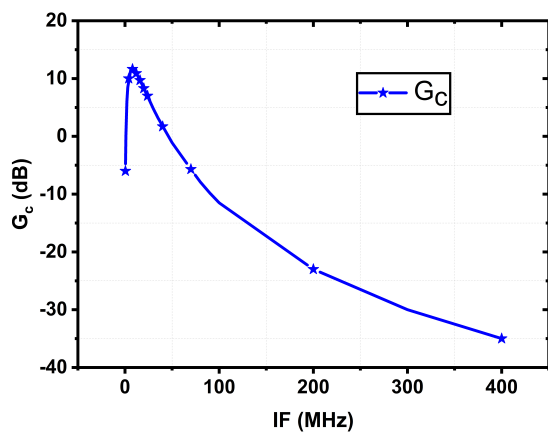


Fig. 14: Measured conversion gain versus IF.

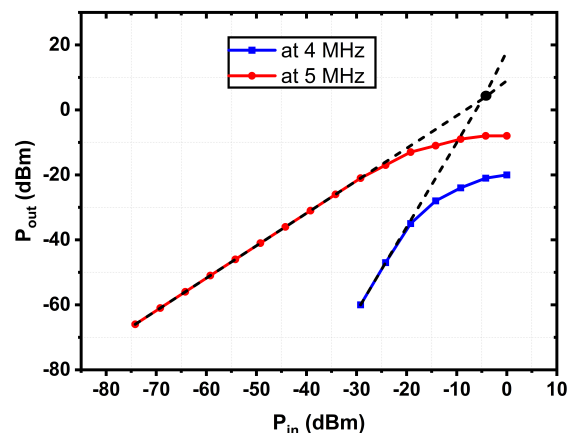


Fig. 16: Measured Input Intercept Point IIP3.

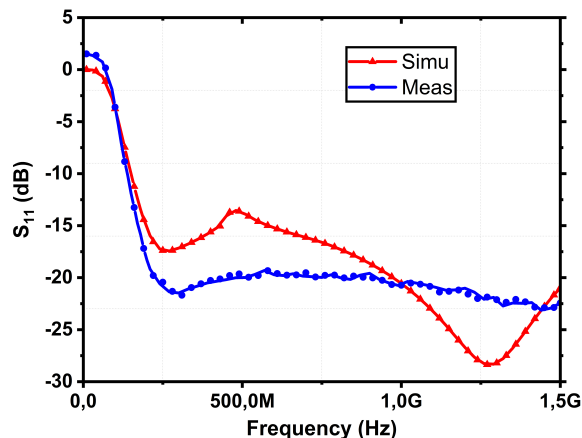


Fig. 15: Measured and simulated S_{11} .

that they are not affected by the IF filtering such that: $f_{RF1} = f_{LO} + f_{IF}$ and $f_{RF2} = f_{LO} + f_{IF} + 1$ MHz for $f_{LO} = 300$ MHz and $f_{IF} = 5$ MHz. The reading at f_{IF} gives the slope 1 ($f_{RF1} - f_{LO}$) and the reading at $f_{IF} - 1$ MHz gives the slope 3 ($2 * f_{RF1} - f_{RF2} - f_{LO}$).

E. Performance Summary and Benchmark

The comparison with the state of the art is shown in Table V. There are three significant parameters in this work: not only harmonic rejection but also power consumption and complexity. Regarding HR, this paper achieves the rejection of the 7th harmonic for only the second time, compared to the previous works. Only [17] proposes to reject the 7th harmonic with an HRR of 67 dB. Even though, in our work, the harmonic rejection is less, our system complexity and power consumption are strongly reduced. This is emphasized by the two figures of merit, ρ_1 and ρ_2 compared in Table V for both this paper's work and the work done in [17]. Moreover, the work in [18] achieves a higher ρ_2 but only rejects up to the 5th harmonic with a very high NF.

VI. CONCLUSION

A calibrated harmonic-rejection N-path mixer is proposed. The calibration methodology addresses the challenges posed by process variation. The HR-NPM presents a wide bandwidth ranging from 0.17 GHz up to 1.2 GHz with a rejection ratio > 45 dB for the 3rd, 5th and 7th LO harmonics thanks to a dedicated machine learning-based calibration algorithm that allows to reach an almost constant HRR for all the considered harmonic components. This is achieved through only one

block of rejection, excluding baseband rejection, which is rarely the case as stated in the introduction. This results in a very reasonable power consumption of 22 mW. The latter can also be imputed to the HR-10PM_{eq}, a simplified version of the HR-10PM, opting for only 5 paths whilst keeping the same rejection band as its counterpart. This mixer offers a conversion gain of 13 dB, a noise figure of 13.3 dB and an IIP3 of -3.5 dBm.

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