



# SiC MOSFET Short-Circuit Protection: a Faster Soft Shut Down Method for Gate Drivers

Julien Weckbrodt, Thanh Long Le, Nicolas Ginot, Christophe Batard, Louison Gouy

## ► To cite this version:

Julien Weckbrodt, Thanh Long Le, Nicolas Ginot, Christophe Batard, Louison Gouy. SiC MOSFET Short-Circuit Protection: a Faster Soft Shut Down Method for Gate Drivers. PCIM Europe 2024 - Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Jun 2024, Nuremberg, Germany. <10.30420/566262014>. <hal-04633714>

**HAL Id: hal-04633714**

**<https://hal.science/hal-04633714v1>**

Submitted on 3 Jul 2024

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



Distributed under a Creative Commons CC BY 4.0 - Attribution - International License

# SiC MOSFET Short-Circuit Protection: a Faster Soft Shut Down Method for Gate Drivers

Julien Weckbrodt<sup>1</sup>, Thanh Long Le<sup>1</sup>, Nicolas Ginot<sup>2</sup>, Christophe Batard<sup>2</sup>, Louison Gouy<sup>2</sup>

<sup>1</sup> Safran Tech, Safran group, Châteaufort, France

<sup>2</sup> Nantes Université, CNRS, IETR, UMR 6164, F-44000 Nantes, France

Corresponding author: Julien Weckbrodt, [julien.weckbrodt@safrangroup.com](mailto:julien.weckbrodt@safrangroup.com)

Speaker: Julien Weckbrodt, [julien.weckbrodt@safrangroup.com](mailto:julien.weckbrodt@safrangroup.com)

## Abstract

Standard short-circuit protection features implemented in gate drivers are often calibrated for IGBT technology. However, the increase in switching slope of the wide-band Gap semiconductors and their lower reliability/maturity is a challenge for securing these new devices against SC events. Decreasing the delays in protection circuits is hence required to secure the operation of high power SiC MOSFETs. This paper presents an Advanced Soft Shut Down method with a reaction delay of 400ns after detection of a 650nH SC. The principle was demonstrated on a 1.2kV SiC module with a bipolar buffer stage based gate driver.

## 1 Introduction

Short-circuit (SC) events can have various origins in a power conversion system: cables manipulation, load failure, insulation material aging, component breakdown, design error... In order to avoid cascading failures, different protection features are implemented in high added value power inverters or critical systems to improve global reliability. Highly inductive SC events coming from the load are generally treated by current limitations and threshold voltages implemented in the software while lowly inductive SC must be treated by hardware protection embedded in the gate driver boards. Indeed, the dynamic of the regulation loops implemented in the control-command systems are unable to react at the  $\mu\text{s}$  scale. The protection features implemented in gate drivers are designed to avoid any destruction of the protected device in case of a fast increase of the drain current. The device is then locked in open circuit and a Fault signal is generally sent to the control unit. This article deals with the hardware implementation of SC protection features on the gate driver and optimizations dedicated to SiC power devices safety.

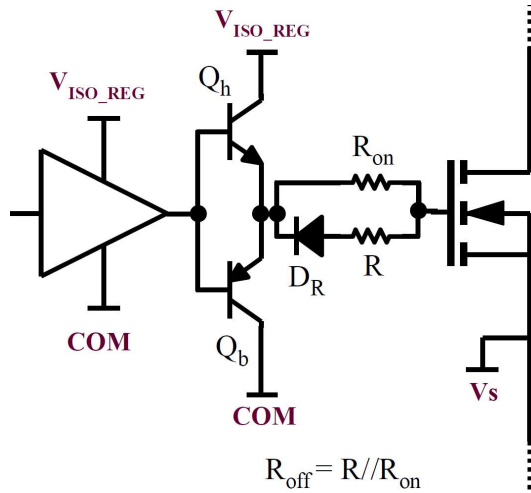
New SiC devices tend to reduce their  $R_{DS(on)}$  to improve the conduction performances. E. Wiesner et al. [1] linked the low on-state resistance of the Silicon Carbide Metal-Oxide-Semiconductor Field Effect Transistors (SiC MOSFET) to their SC energy capabilities, which are lower than their IGBT competitors. An effort is therefore expected on the safety of the SiC devices during SC events.

## 2 Gate driver buffer conventional architectures

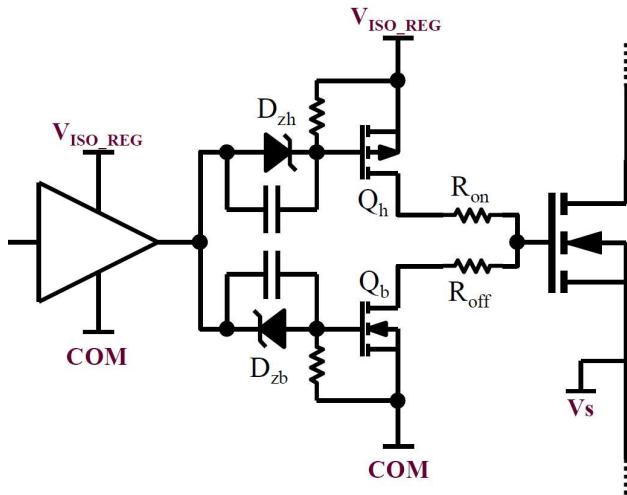
The gate driver buffer stage enables high peak current delivery to the gate input capacitances ( $C_{gs} + C_{gd} = C_{iss}$ ) during the switching events. This transient current is required to achieve a fast switching of the power device leading to lower losses on power switches, which is particularly important for SiC power devices.

In voltage driven gate command, two topologies are commonly used to realize this function: the emitter-follower buffer based on bipolar junction transistors (see Fig.1) and the rail-to-rail push-pull buffer based on MOSFET technology (see Fig.2). Of course, each topology has its own advantages and weaknesses. The bipolar-based structure is easier and safer to use but the gate current injected to the power device highly depends on the current gain ( $\beta$ ) of the bipolar transistors used which cannot be precisely characterized in most cases. The MOSFET-based structure can realize a rail-to-rail operation and deliver a maximal peak current but it is sensible to unintentional short-circuit of the gate driver supply voltage ( $V_{ISO\_REG}$ ) or high-impedance driven gate during the NMOS and PMOS transient transitions.

More complex topologies exist for the gate buffer stage, such as H-bridge gate drivers, resonant gate drivers or current-source controlled gate drivers... These circuits are rarely used in industrial applications and will not be discussed further in this paper.



**Fig. 1** Emitter-follower buffer stage using bipolar transistors



**Fig. 2** Rail-to-rail push-pull buffer stage using MOSFETs

### 3 Conventional SC protection features and typical latencies

#### 3.1 Definitions

Typical Over-Current Protection (OCP) features implemented in gate drivers can be divided in two categories:

- SC detection (e.g. DESAT function)
- SC reaction (e.g. SSD or TLTO)

The detection circuit can identify an abnormal operation characterized by a fast increase of the drain current during the conduction phase. Once a

SC event is identified, an appropriate reaction method is required to extinguish the drain current before the breaking such as Soft Shut Down (SSD) / Safe Turn-Off (STO) or Two-level Turn Off (TLTO) [2], [3]. A reaction circuit is necessary because a regular switching applied on a very high drain current can lead to catastrophic Drain-Source overvoltage due to parasitic stray inductance. This overvoltage can be minimized by an exceptional slower turn-off during a SC event in order to keep  $V_{DS}$  under the Drain-Source breakdown voltage  $V_{(BR)DSS}$ .

Of course, both SC detection and reaction circuits have latencies due to their operating principles and the choice of components. For that reason, we can define 3 times in the SC protection process:

- The blanking time: configurable parameter (about 0.5-5 $\mu$ s);
- The detection delay: latency due to the capacitance charge and propagation delays in components on the SC detection circuitry (about 200-500ns);
- The reaction time: the time required to turn-off and reset the drain current without damage after a SC event detection in the gate driver (variable considering the SC impedance, power device, gate buffer topology, OCP method, components and settings).

The time required to extinguish a SC in a semiconductor power device is therefore the sum of the blanking time, the detection delay and the reaction delay required to reset the drain current to zero. As mentioned above, decreasing the delays in protection circuits is a key point for the safe operation of power SiC MOSFETs.

SC events can also be classified in several categories :

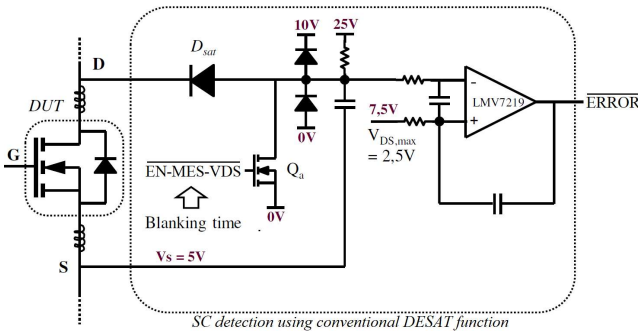
- Lowly inductive SC at turn-on (type I, worst case: requires a blanking time)
- Lowly inductive SC during the conduction (type II, no blanking time = faster detection)
- Highly inductive SC / overload (most of the time due to manipulation or load failures).

Highly inductive SC are generally treated at control level with current limitations implemented in the software since that kind of protection does not require a microsecond reaction; while lowly inductive SC requires the fastest hardware reaction without any control loop delay. It is the responsibility of the designer to check that all probable SC cases are covered by one of these safety features. In this paper, we focus on the protection circuits against lowly inductive SC which are located in the gate driver boards.

### 3.2 SC detection in gate drivers

Regarding SC detection, the well-known desaturation method (DESAT) is now commonly used in gate drivers. The DESAT circuit can identify an abnormal operation characterized by a fast increase of the drain current during the conduction phase. A desaturation diode is used to protect the sensing circuitry against drain potential during the turn-off. If a SC event occurs while the device conducts, the DESAT capacitor voltage increases from the clamped on-state drain-source voltage  $V_{DS(on)}$  of the power device until reaching the pre-set threshold value (typically several Volts). Indeed, during a SC event the on-state drain-source voltage quickly increases due to the saturation behaviour of the MOSFETs under very high drain current. The  $L \cdot di_D/dt$  also contributes to increase the drain-source voltage seen by the gate driver board. In order to prevent false SC detection during normal operation due to a chaotic transient state after the turn-on, a blanking time is generally implemented – about 2-5 $\mu$ s for IGBTs or around 1 $\mu$ s for SiC MOSFETs, depending on the device. The detection circuit is therefore disabled during the blanking time. Sometimes, a template curve using a RC discharge is used at the end of the blanking time to enable the detection feature smoothly. Ideally, both threshold voltage and blanking time should be parametrized by successive SC tests in order to find the best compromise in between false error event immunity (robustness) and safety.

Others detections techniques are investigated in the literature such as Rogowski coil sensors [4], [5], [6] embedded in order to reduce the detection delay to less than 200ns [5]. A Rogowski coil measures the voltage induced by a varying magnetic field, which is proportional to the  $di/dt$ . However, an additional integrator is required and the coil is sensitive to the external magnetic field, which could impede accuracy. A Rogowski coil concept made by printed circuit board (PCB) could be a low-cost solution for SC detection.



**Fig. 3** Typical DESAT circuit for SC detection

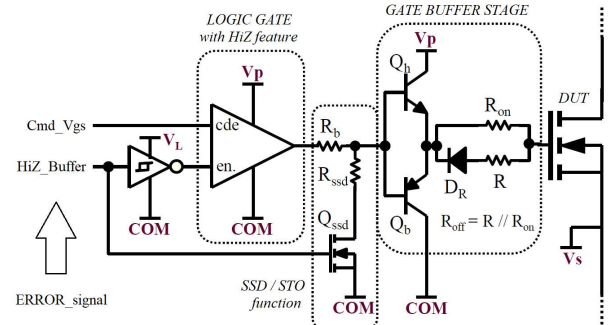
### 3.3 Over current reaction

#### 3.3.1 OCP using Soft-Shut-Down (SSD) / Soft-Turn-Off (STO)

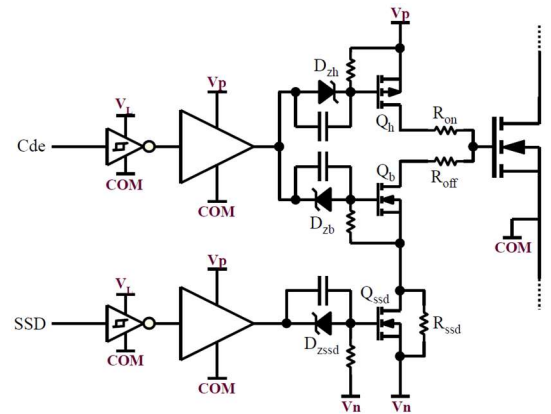
A conventional SSD / STO circuit applied to gate buffer stages are presented in Fig.4 and Fig.5. In both case, the SC reaction is based on an exceptional slower turn-off realized by a gate impedance modification.

In the case of the emitter-follower buffer stage (Fig. 4), the SSD reaction is realized by the  $R_{ssd}$  resistance (470 $\Omega$  in this setup) combined with a logic gate with an embedded high impedance (HiZ) feature. This feature is activated only if the detection circuitry detects a SC event (ERROR signal). In this circuit, the current gain of the bipolar current amplifier ( $\beta$ ) contributes to the SC reaction but it enables the use of a lower power resistance and transistor  $Q_{ssd}$  since the peak current in the SSD branch is divided by the factor  $\beta$ .

In the case of the MOSFET-based buffer stage (Fig. 5), the SSD reaction is realized by an  $R_{ssd}$  resistance exceptionally connected in series with  $R_{g,off}$  when the ERROR signal occurs. The chosen resistance has to support the peak current even if shorted most of the time.



**Fig. 4** SSD / STO protection feature implemented on a bipolar follower gate buffer stage

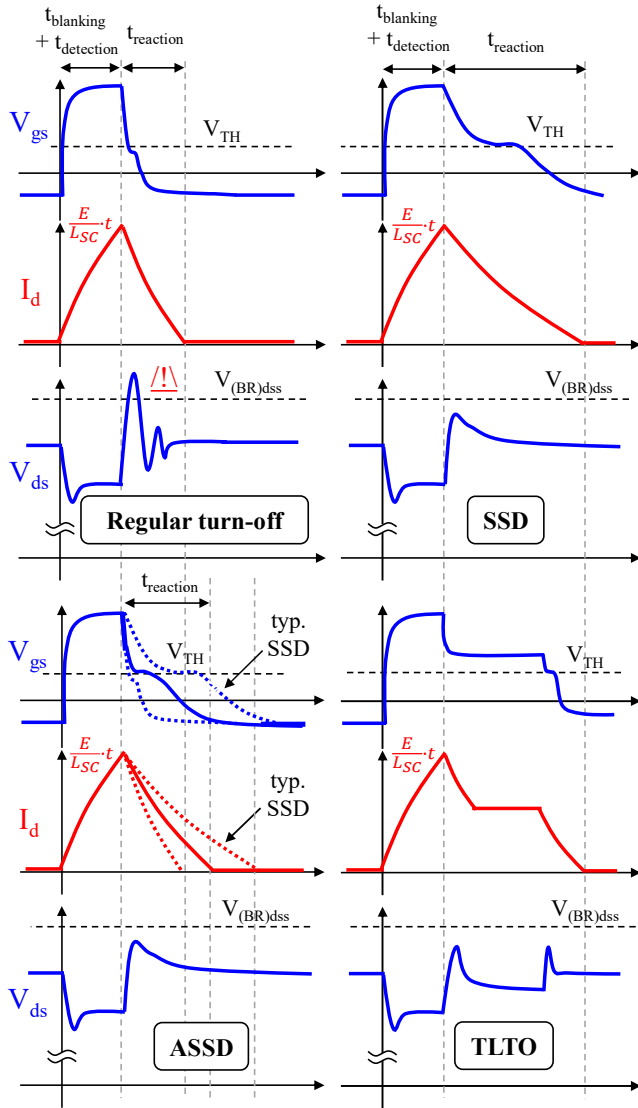


**Fig. 5** SSD / STO function implemented on a rail-to-rail MOSFET-based gate buffer stage

In this setup, the emitter-follower buffer stage was used with a SSD protection feature and a blanking time of  $1\mu\text{s}$  implemented in the DESAT circuit.

### 3.3.2 OCP using Two-level-Turn-Off (TLTO)

The TLTO feature [2], [7], [8] is more and more used for SiC MOSFET protection. The principle consists in reducing the overvoltage using a multi-step gate voltage at the turn-off. The lower gate voltage decreases the value of the saturation current which limits the SC current during the reaction time. Once again, the objective is to keep  $V_{DS}$  under the intrinsic breaking voltage (e.g. 1200V). More than two steps can be used if necessary but this would also increase the complexity of the gate driver.



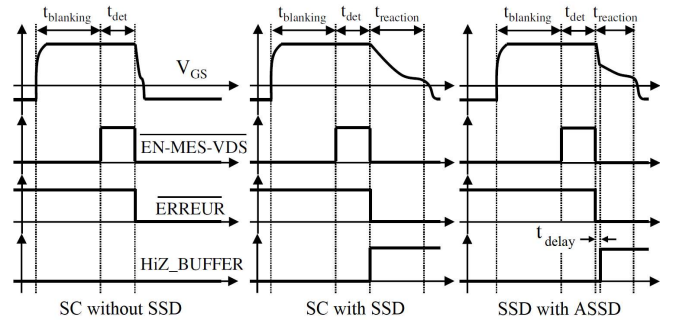
**Fig. 6** Theoretical approach on OCP features: SSD, TLTO and proposed ASSD

### 3.3.3 Other OCP methods

Although conventional protection features are still applicable to SiC MOSFET as explained in [9], it is more and more difficult to guarantee a safe operation in all SC cases due to the faster and less robust nature of SiC MOSFETs compared to their IGBT competitors. Accordingly, it is highly recommended to proceed carefully when applying conventional protection methods to SiC MOSFET. In order to reduce the delay in the SC detection path, a quasi-flying gate concept was introduced in 2023 by M. Picot-Digoix et al. [10]. The principle consist here to put the gate in high impedance (about  $10\text{k}\Omega$ ) while the device conducts. In this case, the gate-source voltage is used to trigger the error signal. Of course, the high impedance mode is disabled before and after the switching transients but more investigations has to be done on the reliability of applying a high gate impedance during normal operation.

## 4 Proposed optimization for a faster SSD reaction: ASSD

The Advanced Soft Shut-Down (ASSD) principle consists in the implementation of a very short delay (e.g.  $t_{\text{delay}}=20\text{ns}$ ) after the SC detection in between the turn-off request and the SSD activation (HiZ\_Buffer signal) when a SC is detected, as described in figure 7. The principle consists in a quick pre-discharge of the gate capacitance  $C_{gs}$  of the SiC device before the real turn-off occurs at the Miller plateau. This optimization consists in connecting the  $R_{ssd}$  at the best moment to obtain both overvoltage reduction and a fast SC reaction. During the delay time, the regular turn-off gate resistance is still connected leading to a fast discharge of the gate-source capacitance  $C_{gs}$ . Characterization has to be done to quantify precisely the optimum delay considering that the SSD mode must be enabled when approaching the turn-off threshold voltage  $V_{th}$  otherwise, an extra overvoltage appears.



**Fig. 7** Chronograms and command signals for the proposed ASSD method



If the introduced delay is too short then the result will be similar to the conventional SSD curve, if it is too long then a maximal overvoltage will occur. The simulations also show that this result is relatively independent from the stray inductance of the SC.

## 5 Simulations based on a SiC MOSFET SPICE model

### 5.1 Model building

Simulations were realized using Wolspeed's SPICE model of the 3<sup>rd</sup> generation SiC power module CAS350M12BM3. The bipolar-based gate buffer was modelled by SPICE NPN and PNP model class with respectively current gains of 140 and 90, corresponding to the components used STN851 and STN951. The short circuit inductance  $L_{SC}$  can be fixed to simulate different cases of SC event such as a half-bridge SC (lowest impedance – about 10nH) or load SC (highest impedance).

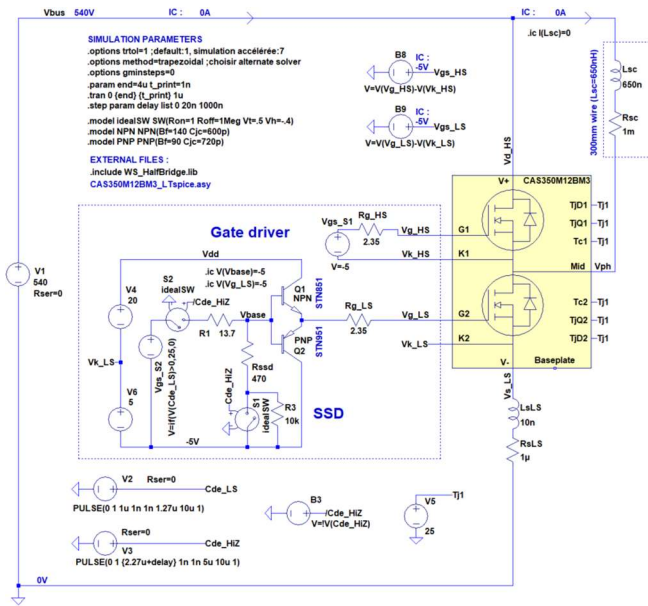


Fig. 8 LTspice model used for parametric analysis

### 5.2 Simulation results

The simulations based on SPICE models demonstrate the existence of an optimal delay time for a given SiC device and its associated gate driver, in the selected settings this optimal time is about 10-20ns. According to these simulations, the STO energy during a SC event can be reduced by -20% while the overvoltage is reduced by -4% using the proposed ASSD method.

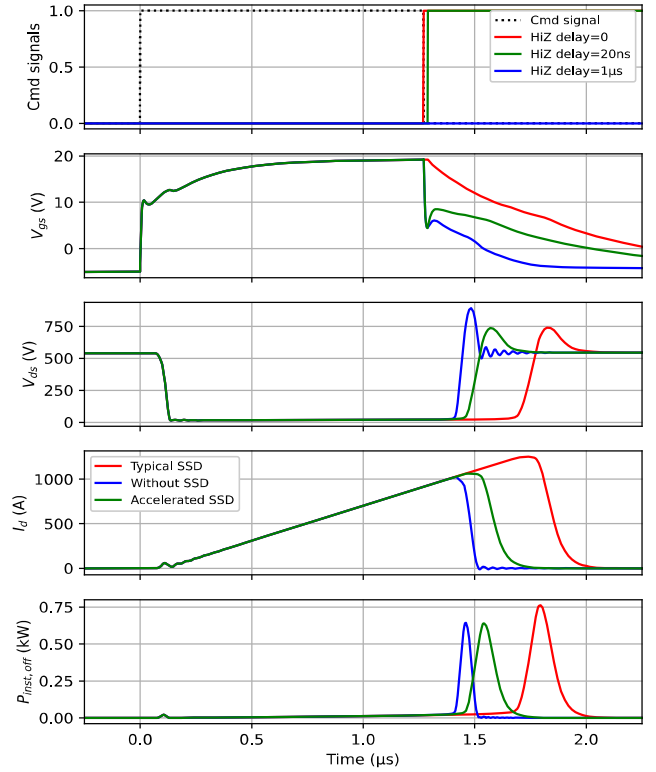


Fig. 9 SC simulation based on CAS350M12BM3 Wolspeed's SPICE model with  $L_{SC} = 650nH$

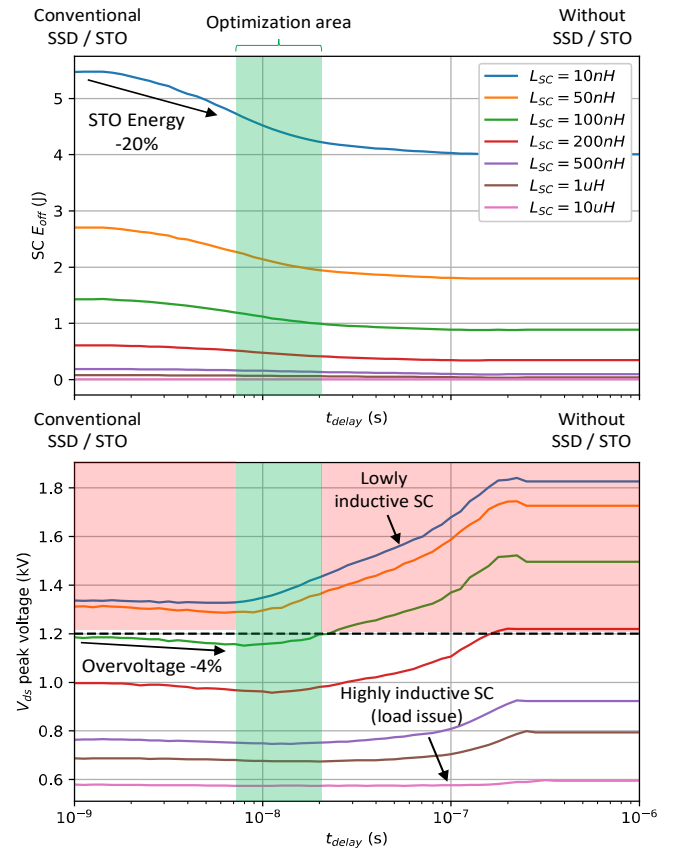
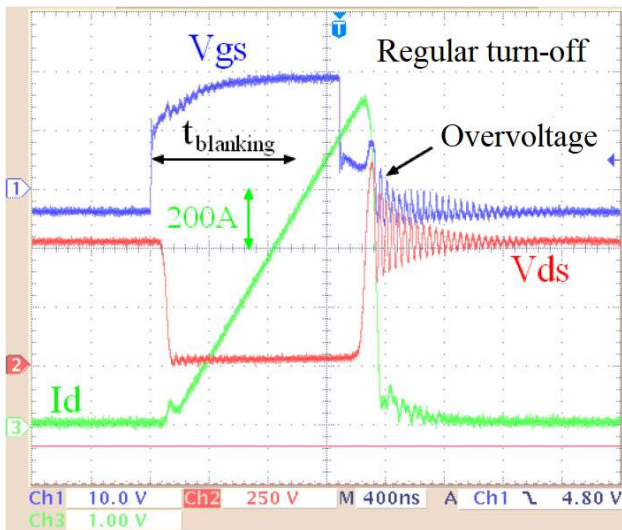


Fig. 10 Parametric simulation results with inductive SC from 10nH to 10μH: STO energy and peak drain-source voltage at turn-off during SC events

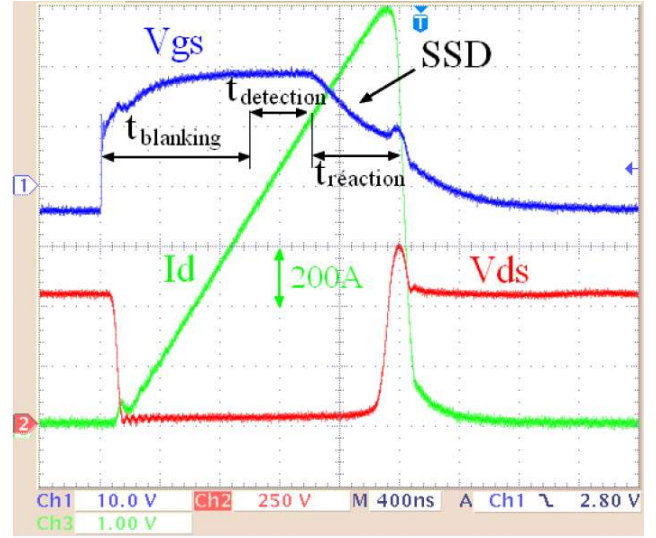
## 6 Experimental results

The method proposed in this article demonstrates a significant reduction of the reaction time of -52% using the same  $R_{ssd}$  value and switching slope. In figure 11, experimental waveforms are shown to highlight the impact of the turn-off under SC condition on the transient low-side (LS) voltages and current. The short-circuit impedance of the 30cm wire used to short the high-side device is here estimated at 650nH considering the current increasing slope. In these conditions, a regular turn-off without any reaction circuitry causes a  $V_{DS}$  overvoltage of 850V while the SSD feature limits it at 720V ( $\Delta V_{DS}$  -42%) for a 540VDC operation. SC with lower impedance will result in a higher overshoot which can cause the voltage breakdown of the SiC device. The resulting overvoltage can be limited by the tuning of  $R_{ssd}$  but it can also increase the turn-off energy during the SC extinguishing  $E_{SC}$ . In addition, the red curve of the figure 13 shows that the drain current continues its increasing during the SSD process until the gate voltage reaches the threshold voltage  $V_{TH}$ . The proposed solution (green curve) takes advantages of the fast discharge of a regular turn-off and the  $R_{ssd}$  resistance connected to the gate buffer during the switching. This method enable both drain-source overshoot limitation and minimization of the soft turn-off energy  $E_{SC}$  dissipated in the SiC power device.

Both the blanking time and the  $R_{ssd}$  value are tunable as well as in the conventional SSD circuit. The blanking time reflects the compromise between robustness and safety while the  $R_{ssd}$  value is the balance between overvoltage tolerance and STO energy/reaction time.

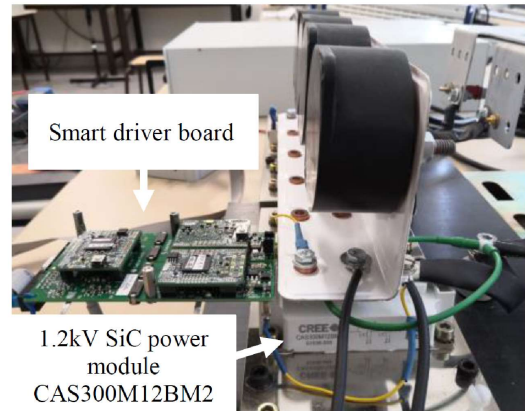
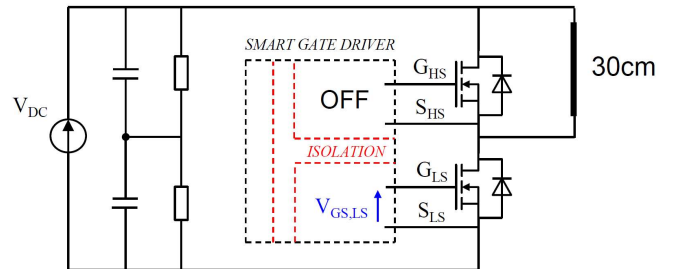


(a)

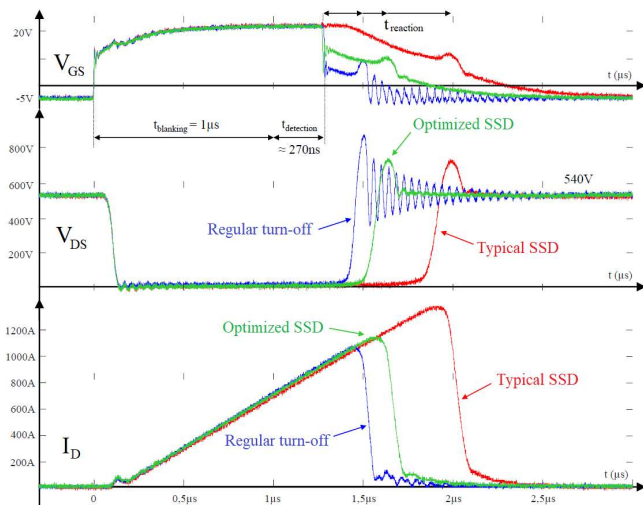


(b)

**Fig. 11** Experimental waveforms for SC tests using a Rogowski sensor at  $V_{DC}=540V$  with  $L_{SC} \approx 650nH$  realized with a CAS300M12BM2 SiC MOSFET : (a) turn-off without SSD; (b) turn-off with SSD ( $R_{ssd} = 470\Omega$ )



**Fig. 12** Experimental setup for SC tests



**Fig. 13** Experimental comparison of SC test results using the ASSD method at  $V_{DC}=540V$  with  $L_{SC} \approx 650nH$  and  $1\mu s$  blanking time

## 7 Conclusion

The safe operating of SiC power devices requires a faster SC protection. Conventional protection methods are still applicable but require some optimizations for SiC MOSFETs. The process of interruption of a SC event can be decomposed into 3 steps: the blanking time, the detection time and the reaction time. The proposed ASSD solution consists in an optimization of the reaction time after SC detection by adding a few nanoseconds delay (e.g. 20ns) in the SSD process to achieve both  $V_{DS}$  overvoltage limitation and fastest reaction. Simulations based on SPICE models have shown the existence of an optimum point for a given SiC device and its associated gate driver. Results have proven a reduction of the reaction time of -300ns, a SC turn-off energy of -20% and an overvoltage reduction of -4% compared to the conventional SSD method using the same  $R_{ssd}$  value. The experimental results were obtained with a SC impedance of 650nH on a CAS300M12BM2 SiC module at  $V_{DC}=540V$ . The ASSD proposed method can be easily realized using a basic RC circuit at the appropriate location on a conventional gate driver.

This optimization was implemented on a bipolar gate driver architecture but the principle can be easily extended to all types of gate drivers and combined with fast SC detection to improve the robustness of SiC devices. Although the optimum delay value can be predicted by an appropriate SPICE simulations, it is highly recommended to set it by several SC tests for a given design. Fur-

ther investigations has to be done to check the repeatability of these SC capabilities considering chips disparities and various devices.

## References

- [1] E. Wiesner, E. Thai, A. Volke, and K. Fink, "Advanced protection for large current full SiC-modules," presented at the PCIM Europe, 2016.
- [2] A. Volke, M. Hornkamp, and J. Wendt, *IGBT modules. Technologies, Driver and application*, Infineon Technologies. 2017.
- [3] N. Ginot, C. Batard, and P. Lahaye, "MOSFET et IGBT : circuits de commande, sécurisation et protection du composant à semi-conducteur," in *Techniques de l'ingénieur*, vol. V1, 2017.
- [4] T. L. Le, J.-S. Ngoua-teu, and T. Youssef, "High power module GaN with integrated current sensor for fast short circuit protection," presented at the EuroSimE, Apr. 2022. doi: 10.1109/EuroSimE54907.2022.9758909.
- [5] J. Walter, J. Acuna, and I. Kalfass, "Design and Implementation of an Integrated Current Sensor for a Gallium Nitride Half-Bridge," presented at the PCIM Europe, Nürnberg, 2018.
- [6] J. Fu, Z. Zhang, Y. F. Liu, P. C. Sen, and L. Ge, "A New High Efficiency Current Source Driver With Bipolar Gate Voltage," *IEEE Trans Power Electron*, vol. 27, no. 2, pp. 987–997, Feb. 2012, doi: 10.1109/TPEL.2010.2077741.
- [7] M. Shim, K. Lee, J. Kim, and K. Kim, "Multistep Soft Turn-Off Time Control to Suppress the Overvoltage of SiC MOSFETs in Short-Circuit State," *IEEE Access*, vol. 10, 2022, doi: 10.1109/ACCESS.2022.3169764.
- [8] Y. Shi, R. Xie, L. Wang, Y. Shi, and H. Li, "Short-circuit protection of 1200V SiC MOSFET T-type module in PV inverter application," presented at the ECCE, Sep. 2016. doi: 10.1109/ECCE.2016.7855428.
- [9] V. Thayumanasamy, C. Fuentes, K. Lenz, I. Rabl, and J. Engstler, "Short Circuit Protection of a Power Module with Trench-SiC-MOSFET. Can DESAT be Fast Enough?," presented at the PCIM Europe, May 2022. doi: 10.30420/565822111.
- [10] M. Picot-Digoix, F. Richardeau, S. Azzopardi, and T.-L. Le, "Quasi-flying gate concept used for short-circuit detection on SiC power MOSFETs based on a dual-port gate driver," *IEEE Trans. Power Electron.*, 2023.