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# Improvement of linearity in trap-rich substrates for radio frequency applications: Which of donor and acceptor trap is the best?

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Justine Philippe,<sup>1,a)</sup>  Jean-François Robillard,<sup>1</sup>  Daniel Gloria,<sup>2</sup> and Emmanuel Dubois<sup>1,b)</sup> 

## AFFILIATIONS

<sup>1</sup>Univ. Lille, CNRS, Centrale Lille, Univ. Polytechnique Hauts de France, JUNIA, UMR 8520—IEMN—Institut d'Electronique, de Microélectronique et de Nanotechnologie, Lille F-59000, France

<sup>2</sup>STMicroelectronics, 850 rue Jean Monnet, Crolles F-38920, France

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<sup>a)</sup>Electronic mail: [justine.philippe@junia.com](mailto:justine.philippe@junia.com)

<sup>b)</sup>Author to whom correspondence should be addressed: [emmanuel.dubois@univ-lille.fr](mailto:emmanuel.dubois@univ-lille.fr)

## ABSTRACT

This paper investigates the effect of volume traps intentionally introduced into a silicon-on-insulator (SOI) substrate by inserting a layer of polysilicon beneath buried oxide. In radio frequency applications, this type of substrate, referred to as trap-rich, is known to considerably reduce the generation of harmonics resulting from the parasitic non-linear charge dynamics introduced by the substrate handler under the buried oxide. This analysis focuses on a test vehicle in the form of an integrated coplanar waveguide on two types of substrates, namely, high-resistivity SOI substrates with and without a trap-rich layer. From a modeling point of view, a simulation methodology is implemented in order to convert the 3D simulation of the coplanar waveguide into a 2D treatment that takes into account the wave propagation effect associated with the distributed nature of the transmission line. As a first step, this modeling strategy is implemented to reproduce the effect of increasing substrate resistivity on 2nd and 3rd harmonic reductions, leading to an excellent agreement with experimental data. Building on this validation of the simulation method, we have opted to simulate the non-linear response of the transmission line on the SOI trap-rich substrate by simplifying the trap distribution model. To avoid the adoption of unverified and strongly process-dependent trap distributions across the bandgap, a midgap monovalent trap density has been introduced, either acceptor or donor density. A monovalent density of acceptor traps with a concentration of  $10^{16} \text{ cm}^{-3}$  and a carrier lifetime of 0.1 ns has been shown to reproduce the experimental data very accurately with a substantial reduction in 2nd and 3rd harmonics. A detailed analysis of the displacement current waveforms explains the beneficial role of acceptor traps compared with donor traps.

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## I. INTRODUCTION

The explosion in wireless services over the last two decades has created a compelling need for high-speed transmission and other functionalities driven by the use of smart phones, tablets, and other connected devices in the Internet of Things (IoT) momentum. In this context, the semiconductor and mobile communications industry has developed broadband technologies, the most recent of which are 4G long term evolution (LTE) and 5G new radio (NR)<sup>1,2</sup> as well as other standards linked to GPS, RFID, and

NFID services. All these developments have resulted in increased requirements in terms of path loss reduction, bandwidth, and signal integrity in the front-end of communications systems.<sup>3</sup> Front-end communication systems involve a multiplicity of signal routing paths via switches, transmission lines, couplers, diplexers, filter banks, and amplifiers, all of which are components posing new challenges as frequency increases. In this respect, CMOS technologies on SOI (silicon-on-insulator) substrates have come to the fore for their distinctive advantages in terms of RF isolation and the ease with which digital and radio frequency functions can be

02 July 2024 14:08:06

co-integrated. While the choice of a high-resistivity substrate (1–10 k $\Omega$ ) helped to reduce RF losses and maintain acceptable linearity for the first communication standards, the level of isolation and harmonic rejection is much more demanding for the 5G standard and the forthcoming 6G standard. Unfortunately, a non-negligible source of harmonics is caused by the non-linear behavior of capacitive coupling between propagation lines located in the interconnect network and the silicon (Si) substrate handler. At high levels of RF power injected in propagation lines, this coupling induces parasitic displacement currents in response to the variation in potential across metal-oxide-silicon capacitance, one component of which, associated with the charge dynamics in silicon, is non-linear. Since the Si handler is the source of non-linearities, a radical and elegant approach is to completely eliminate this carrier substrate and transfer the active region comprising the buried oxide (BOX), SOI layer, and interconnections onto a very low-loss insulating substrate such as glass. In Refs. 4 and 5, techniques of wafer thinning and layer transfer bonding developed for flexible electronics were exploited to demonstrate the decisive advantage of completely eliminating the substrate in order to probe the ultimate margin of 2nd and 3rd harmonics reduction. In a more conservative approach, high SOI substrate suppliers have developed *ad hoc* material engineering solutions to cope with the issue of power loss and linearity. For example, SOI eSI<sup>TM</sup> (enhanced signal integrity) substrates developed by SOITEC<sup>6</sup> incorporate a layer of trap-rich (TR) polysilicon between the BOX and the Si handler, the effect of which is to pin the Fermi level at an energy level close to the dominant charged traps in the bandgap. Depending on the nature of these dominant traps, donor or acceptor, it follows that the electrostatic potential can itself be pinned so that potential variations across the non-linear Si capacitance can be attenuated, thus reducing the non-linear parasitic currents. Compared with a high-resistivity (HR) substrate, literature reports that the TR counterpart has the distinctive advantage of freezing the free carriers of the parasitic surface conduction layer (PSC) induced by a fixed positive charge at the BOX/Si handler interface. The resulting beneficial impacts for components integrated on this type of substrate are the reduction of (i) insertion losses, (ii) non-linear effects, (iii) substrate crosstalk, and (iv) substrate dependence on DC bias.<sup>7–9</sup> With regard to harmonic generation, the understanding and modeling of HR and TR substrates in the large-signal regime is rarely addressed in the literature through a quantitative analysis that takes a detailed account of the PSC layer and trapping mechanisms.<sup>10,11</sup> In this context, this paper addresses the physics of traps in the polysilicon layer buried under the BOX of TR SOI substrates in order to show under what conditions they can contribute to improving the linearity of substrates for RF applications. The test vehicle used to carry out this study is a coplanar waveguide (CPW) deposited on the BOX of an SOI substrate. The aim is to investigate the impact of traps as a function of their nature (acceptors and donors), their energy level in the bandgap, and their lifetimes. To this end, we show the implementation of a simulation methodology that restricts the analysis to a two-dimensional cross section treatment of the CPW by converting the distributed nature of the transmission line into a second-order equivalent lumped circuit whose parameters are determined from the formalism introduced by Elmore<sup>12</sup> for RC networks and extended by Ismail *et al.*<sup>13</sup> to include line inductance. The power

level of 2nd (H2) and 3rd (H3) harmonics obtained by simulation as a function of the injected input power is systematically compared to the measured data to draw conclusions on the respective effects of donor and acceptor traps.

## II. METHODS

### A. Coplanar waveguide description and RF measurements

In this study, the coplanar waveguide (CPW) features a line length  $L = 1$  mm and a width  $W_{\text{sig}} = 8 \mu\text{m}$ . The signal trace is separated from the ground lines by a  $13.5 \mu\text{m}$  gap [Fig. 1]. The  $4 \mu\text{m}$  thick metal trace results from the stacking of four metal layers in the interconnect network. In the first version, the CPW metal tracks are deposited on the  $0.4 \mu\text{m}$  thick BOX layer covering an  $800 \mu\text{m}$  thick HR silicon handler as shown in Figs. 1(c) and 1(d). In the second case, the CPW is fabricated on an HR SOI substrate with an undoped trap-rich (TR) polysilicon layer inserted under the BOX as depicted in Figs. 1(e) and 1(f). In both cases, the substrate handler is n-type and has high resistivity ( $\sim 1 \text{ k}\Omega \text{ cm}$ ). For both types of substrates, ground is applied to the substrate handler by a contact plug through the BOX which is electrically connected to the ground planes of the CPW. No fixed charges are introduced at the BOX/Si handler interface. Harmonic distortion measurements of the above-described CPW have been conducted on-wafer using ground-signal-ground (GSG) RF probes. The complete measurement setup is described in Ref. 14. The H2 and the H3 noise floor were less than  $-140$  and  $-100$  dBm for input powers of up to 20 and 30 dBm, respectively.

### B. Simulation strategy

#### 1. Physics of transport and trap models

To capture the large-signal charge dynamics in the semiconductor, time-dependent charge transport equations are used, with Fourier analysis in a post-processing step to determine the power of harmonics. Transport simulations were carried out using the IMPACT<sup>15</sup> code, a TCAD (technology computer-aided design) in-house device simulation tool, to solve the Poisson equation [Eqs. (1) and (2)] and the electron and hole current conservation equations [Eqs. (5) and (6)],

$$\text{div}(\epsilon \vec{\nabla} \Psi) = -q(p - n + N_d - N_a) - Q_T, \quad (1)$$

where  $\Psi$  is the electrostatic potential,  $\epsilon$  the dielectric constant of the material,  $p$  and  $n$  are volume concentrations of holes and electrons, respectively,  $N_d$  and  $N_a$  are concentrations of dopants and donors or acceptors, respectively.  $Q_T$  represents the ionized charge associated with volume traps. It is developed here in the case of discrete monovalent traps with expressions that differ depending on whether traps under consideration are donors or acceptors with a volume concentration of  $N_{TD}$  and  $N_{TA}$ , respectively. The ionized volume charge is, therefore, given by

$$Q_T = q(N_{TD}^+ - N_{TA}^-), \quad (2)$$

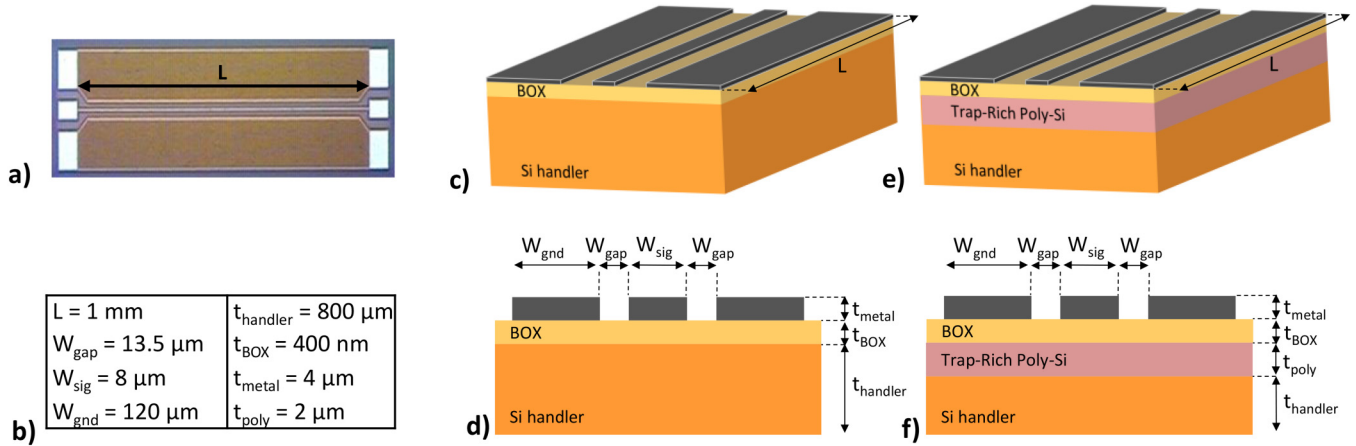


FIG. 1. Description of the considered coplanar waveguide (CPW): (a) optical microscope view, (b) characteristic dimensions, (c) and (d) CPW on an HR substrate, and (e) and (f) CPW on a TR substrate.

$$N_{ID}^+ = N_{ID} \cdot \frac{v_p \sigma_{pD} p + v_n \sigma_{nD} n_i e^{\frac{E_{ID} - E_i}{kT}}}{v_n \sigma_{nD} \left( n + n_i e^{\frac{E_{ID} - E_i}{kT}} \right) + v_p \sigma_{pD} \left( p + n_i e^{\frac{E_i - E_{ID}}{kT}} \right)}, \quad (3)$$

$$N_{IA}^- = N_{IA} \cdot \frac{v_n \sigma_{nA} n + v_p \sigma_{pA} n_i e^{\frac{E_i - E_{IA}}{kT}}}{v_n \sigma_{nA} \left( n + n_i e^{\frac{E_{IA} - E_i}{kT}} \right) + v_p \sigma_{pA} \left( p + n_i e^{\frac{E_i - E_{IA}}{kT}} \right)}, \quad (4)$$

where  $N_{ID}^+$  and  $N_{IA}^-$  represent the volume concentration of donor and acceptor traps being ionized, respectively.  $E_i$  is the intrinsic energy level,  $n_i$  is the intrinsic concentration, and  $E_{ID}$  and  $E_{IA}$  are the donor and acceptor trap energy levels, respectively.  $v_n$  and  $v_p$  are electron and hole thermal velocities, respectively. Finally,  $\sigma_{nD}$ ,  $\sigma_{pD}$  and  $\sigma_{nA}$ ,  $\sigma_{pA}$  correspond to the electron and hole capture cross sections of the considered donor or acceptor trap, respectively. As shown in Fig. 2, the charge state of a donor trap is represented by the notation (0/+), indicating that if the trap is occupied by an electron, i.e., if the energy level of the trap is below the Fermi level, the charge state is zero and is positively charged if above, i.e., unoccupied by

an electron. Similarly, the charge state of an acceptor trap is represented by the notation (-/0), indicating that if the trap is occupied by an electron, it is negatively ionized and neutral if unoccupied. In contrast to doping atoms, it is worth noting that volume traps in polysilicon are more acceptor-like in the upper half and donor-like in the lower half of the bandgap.<sup>16</sup> This type of trap distribution across the bandgap is similar to that of interface traps at the SiO<sub>2</sub>/Si interface.<sup>17</sup>

The current continuity equations reflect charge conservation in response to time varying carrier concentrations and generation/recombination of electron/hole pairs,

$$\frac{\partial n}{\partial t} = \frac{1}{q} \vec{\nabla} \cdot \vec{J}_n + (G_n - R_n), \quad (5)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \vec{\nabla} \cdot \vec{J}_p + (G_p - R_p), \quad (6)$$

where  $\vec{J}_n$  and  $\vec{J}_p$  represent the current surface densities (A/cm<sup>2</sup>) for electrons and holes, respectively, while the term  $(G_{n,p} - R_{n,p})$  stands for

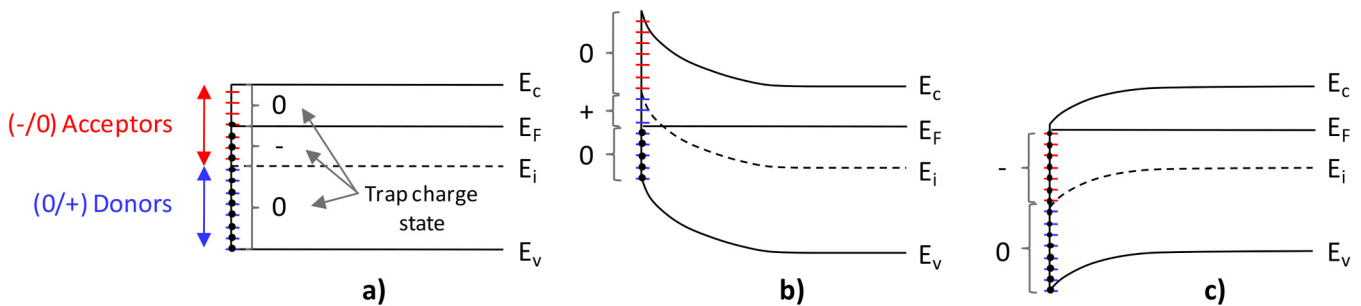


FIG. 2. Band diagram of n-type silicon showing different charge states for an arbitrary distribution of acceptor and donor traps (a) at flatband condition, (b) at inversion with a positive trap charge balance, and (c) at accumulation with a negative trap charge balance.

02 July 2024 14:08:06

the generation/recombination rate ( $\text{cm}^{-3} \text{s}^{-1}$ ) whose expression is described by the well-established Shockley–Read–Hall statistics,<sup>18,19</sup>

$$(R_{n,p} - G_{n,p}) = \frac{np - n_i^2}{\tau_{nX} \left( p + n_i e^{\frac{E_i - E_{iX}}{kT}} \right) + \tau_{pX} \left( n + n_i e^{\frac{E_{iX} - E_i}{kT}} \right)}, \quad (7)$$

where  $E_{iX}$  is the trap energy level,  $\tau_{nX}$  and  $\tau_{pX}$  are electron and hole lifetimes, respectively, which are expressed as functions of trap density  $N_{iX}$ , the electron and hole capture cross sections  $\sigma_{nX}, \sigma_{pX}$ , and the carrier thermal velocity,

$$\begin{aligned} \tau_{nX} &= \frac{1}{N_{iX} v_n \sigma_{nX}} \\ \tau_{pX} &= \frac{1}{N_{iX} v_p \sigma_{pX}}. \end{aligned} \quad (8)$$

In Eqs. (7) and (8), the subscript  $X$  stands for  $D$  in the case of donor-like traps and for  $A$  in the case of acceptor-like traps. In the case of fast varying excitations, the time dynamics of donor and acceptor traps are taken into account using additional rate equations for solving  $N_{iD}^+$  and  $N_{iA}^-$ , as exemplified in Ref. 20, thus reflecting that traps follow a finite-time response. The transient electron and hole capture rates embedded in these rate equations can be introduced as  $R_n$  and  $R_p$  in place of Eq. (7) in the current continuity equations (5) and (6). It is interesting to note that these equations involve the characteristic time constants  $\tau_{nA}$  and  $\tau_{pD}$ , in other words, the trap lifetimes, for the equations governing the dynamics of  $N_{iA}^-$  and  $N_{iD}^+$ , respectively. Insofar, as the lifetimes are shorter than the period of the excitation signal, it can be legitimate and acceptable to consider that the traps reach equilibrium almost instantaneously. In theory, the CPW structure should be simulated in 3D to take into account the wave propagation along the line. Due to the long length of the line (1 mm) compared to the characteristic dimensions of the CPW, mesh refinement requirements in finite element simulation of Poisson and transport equations can rapidly become prohibitive as it requires an extremely fine step (typically 10 nm) under the BOX in order to capture abrupt variations in carrier densities. For this reason, an efficient simulation methodology is proposed in Sec. II B 2 to transform the original 3D problem into a 2D cross-sectional analysis of the CPW capacitance by converting the distributed nature of the transmission line into a second-order equivalent lumped circuit.

## 2. Simplification of the simulation scheme

The aim of this section is to derive a simple equivalent approximation of the propagation line, enabling the analysis to be limited to a two-dimensional cross section perpendicular to the direction of propagation, instead of considering the three-dimensional solution of the transport equations described above. In this way, the distributed line model shown in Fig. 3(a) can be replaced by the one shown in Fig. 3(b), and the values of the lumped elements  $R'$  and  $L'$  can be calculated and fed into a TCAD simulation as described in Fig. 4. Following this approach, the electrical behavior of the non-linear capacitor  $C'$  is solved using the transport equations and trap models described in Sec. II B 1. In the case of a lossy substrate, a shunt conductance should theoretically be associated in parallel with the capacitances shown in Fig. 3. In order to implement the model of Ismail *et al.*<sup>13</sup> described below, we first neglected this conductance in order to derive  $R'$  and  $L'$ . However, in a second step, the TCAD simulation of the 2D cross section of the transmission line augmented by the lumped elements  $R'$  and  $L'$  inherently takes into account the non-linear behavior of line capacitance and shunt conductance. The distributed nature of a transmission line is conventionally represented as shown in Fig. 3(a), to which can be associated a transfer function described by the following relationship where  $a_i$  and  $b_j$  are real coefficients and  $m > n$ :

$$g(s) = \frac{1 + a_1 s + a_2 s^2 + \dots + a_n s^n}{1 + b_1 s + b_2 s^2 + \dots + b_m s^m}. \quad (9)$$

In a 2nd-order approximation, the reduced transfer function can be expressed at the output node  $N$  in the canonical form described by<sup>13</sup>

$$g(s) \sim \frac{\omega_{0N}^2}{s^2 + 2\zeta_N \omega_{0N} s + \omega_{0N}^2}, \quad (10)$$

with the following expressions for  $\zeta_N$  and  $\omega_{0N}$  when referring to the reduced schematic shown in Fig. 3(b):

$$\begin{aligned} \zeta_N &= \frac{1}{2} \frac{R' C'}{\sqrt{L' C'}} \\ \omega_{0N} &= \frac{1}{\sqrt{L' C'}}. \end{aligned} \quad (11)$$

Using the results of Ismail *et al.*<sup>13</sup> and considering the RLC tree of the distributed propagation line diagram in Fig. 3(a),  $\zeta_N$  and

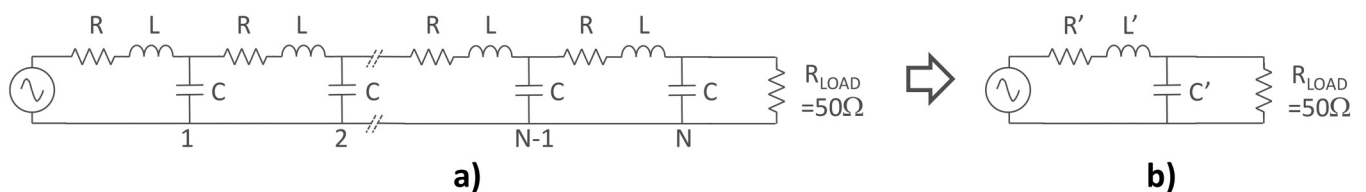
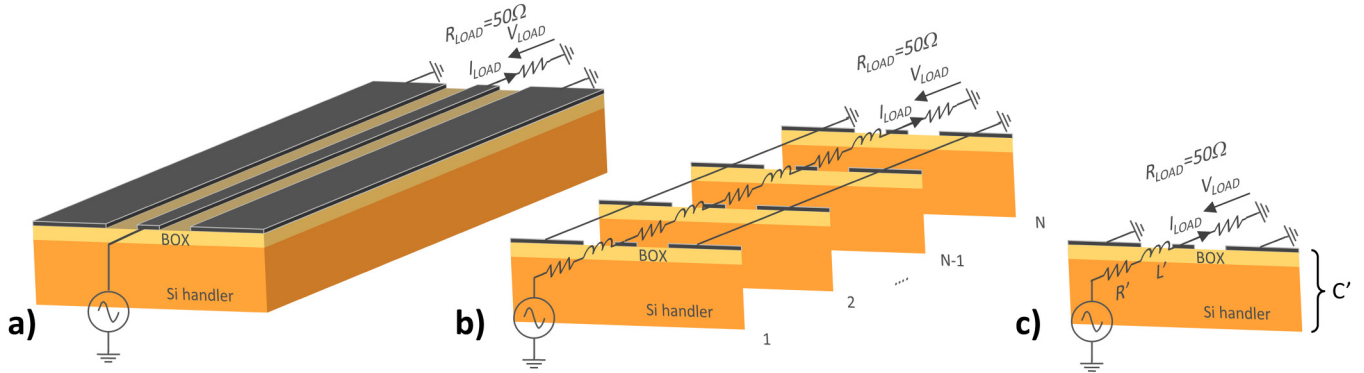


FIG. 3. Electrical schematic of a transmission (a) in its distributed form in  $N$  sections and (b) in its reduced form in a 2nd-order approximation.

02 July 2024 14:08:06



**FIG. 4.** Schematic representation of the coplanar line on an SOI substrate (a) in its monolithic continuous form, (b) in its discretized distributed form, and (c) in its reduced form, following a 2nd-order approximation of the transfer function associated with the distributed representation. For capacitance  $C'$ , the time-dependent current-voltage relation is provided by the 2D TCAD simulation of the 2D cross section of the CPW.

$\omega_{0N}$  can be calculated as

$$\zeta_N = \frac{1}{2} \frac{\sum_{k=1}^N C_k R_{Nk}}{\sqrt{\sum_{k=1}^N C_k L_{Nk}}} = \frac{1}{2} \frac{\frac{N(N+1)RC}{2}}{\sqrt{\frac{N(N+1)LC}{2}}} \quad (12)$$

$$\omega_{0N} = \frac{1}{\sqrt{\sum_{k=1}^N C_k L_{Nk}}} = \frac{1}{\sqrt{\frac{N(N+1)LC}{2}}},$$

where the summation index  $k$  covers  $N$  capacitances in the circuit shown in Fig. 3(a) and  $R_{Nk}$  is the common resistance between nodes  $k$  and  $N$ , starting from the input. Finally, the expressions for  $R'$ ,  $L'$  and  $C'$  can be derived by identifying the expressions of  $\zeta_N$  and  $\omega_{0N}$  in both Eqs. (11) and (12). From this identification, several partition options can be adopted in order to obtain the same expression of the reduced transfer function. The selection is finally made on the basis that the sum of the elementary resistances  $NR$  is equal to the reduced resistance  $R'$ ,

$$\begin{aligned} R' &= NR, \\ L' &= NL, \\ C' &= \frac{(N+1)C}{2}, \end{aligned} \quad (13)$$

where  $N$  represents the number of sections in the circuit. In other words, the CPW can be divided into  $N$  sections along its length, as represented in Fig. 4. Here, the line length is equal to  $1000 \mu\text{m}$  and we take  $N = 1000$  which gives a unitary section length of  $1 \mu\text{m}$ .

### 3. Evaluation of the harmonics power

Based on the simulation scheme described above, the time-dependent output voltage and current in response to a periodic input signal of pulsation  $\omega_0$  are processed by Fourier analysis to

obtain the following series expansions:

$$\begin{aligned} V_{OUT}(t) &= \frac{C_{V_0}}{2} + \sum_{n=1}^{\infty} C_{V_n} \cos(n\omega_0 t - \varphi_n) \\ I_{OUT}(t) &= \frac{C_{I_0}}{2} + \sum_{m=1}^{\infty} C_{I_m} \cos(m\omega_0 t - \theta_m). \end{aligned} \quad (14)$$

The average output power corresponding to the quantity measured experimentally can be computed according to the following equation, which can be used to deduce the power of each harmonic:

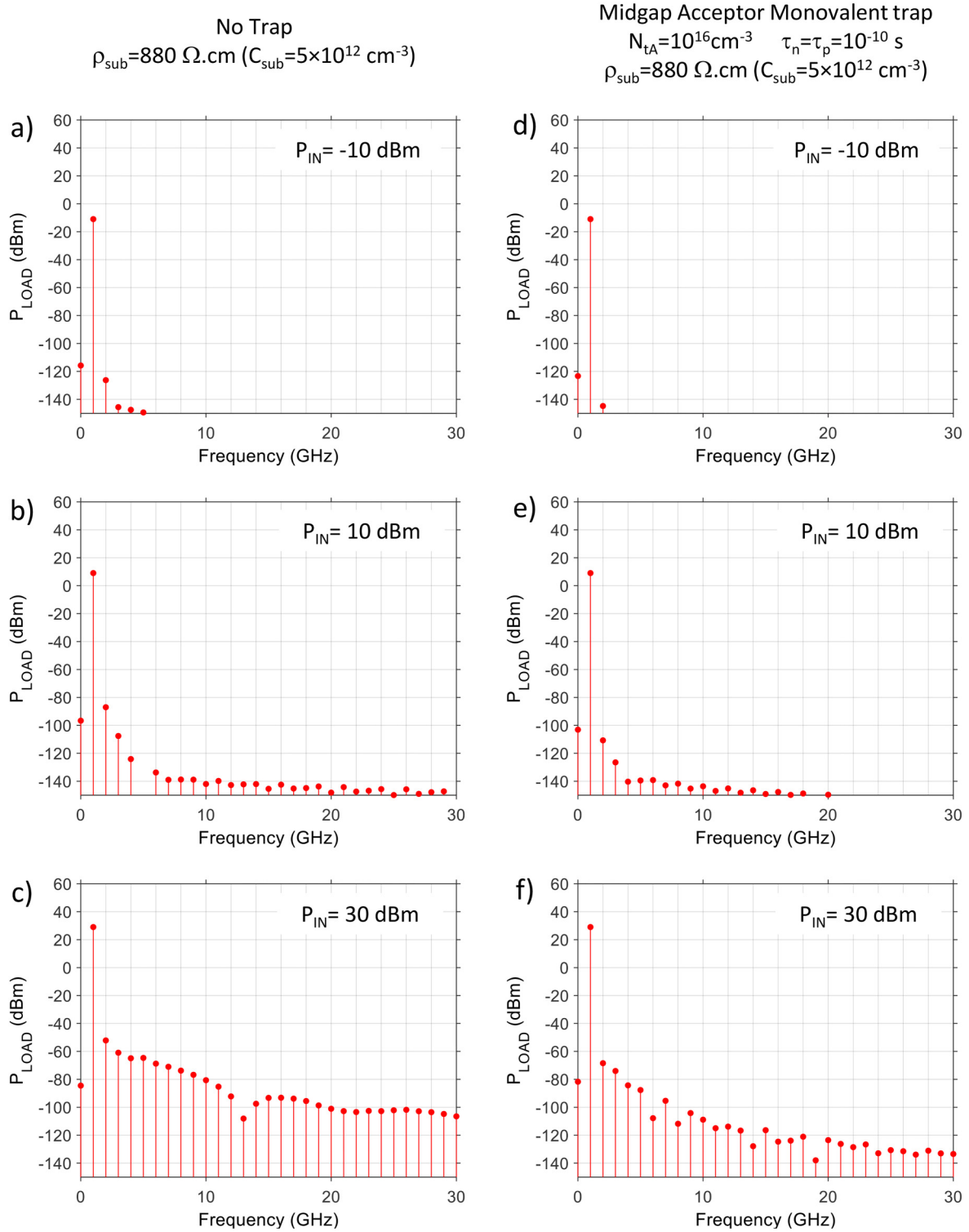
$$\begin{aligned} P_{OUT_{avg}} &= \frac{C_{V_0} C_{I_0}}{4} + \sum_{n=1}^{\infty} \frac{C_{V_n} C_{I_n}}{2} \cos(\varphi_n - \theta_n) \\ &= P_0 + \sum_{n=1}^{\infty} P_{OUT_n}. \end{aligned} \quad (15)$$

For the sake of illustration, Fig. 5 shows typical frequency spectra associated to the power in  $R_{LOAD}$  as obtained by fast Fourier transform (FFT) applied to  $V_{LOAD}(t)$  and  $I_{LOAD}(t)$  over a full period of the excitation signal in accordance with Eqs. (14) and (15). Power spectra are given for HR [Figs. 5(a)–5(c)] and TR [Figs. 5(d)–5(f)] substrates for three levels of input power (H1) at  $-10$ ,  $10$ , and  $30$  dBm. In Sec. III, this type of spectra is used to represent H2 and H3 power as a function of frequency in Figs. 6(b) and 7(c) for HR and TR substrates, respectively. It is worth noting that the average power resulting from the simulation of the capacitor alone, without taking into account the lumped elements of the transmission line, would be zero since voltage and current are in quadrature for a capacitor. This result is consistent with the fact that a capacitor is only the seat of reactive power. It also shows that the pseudo-3D scheme can account for the proper phase shift between voltage and current introduced by the distributed nature of the line.

### 4. Synthesis of the simulation method

The rationale and important details behind the proposed simulation strategy can be summarized as follows:

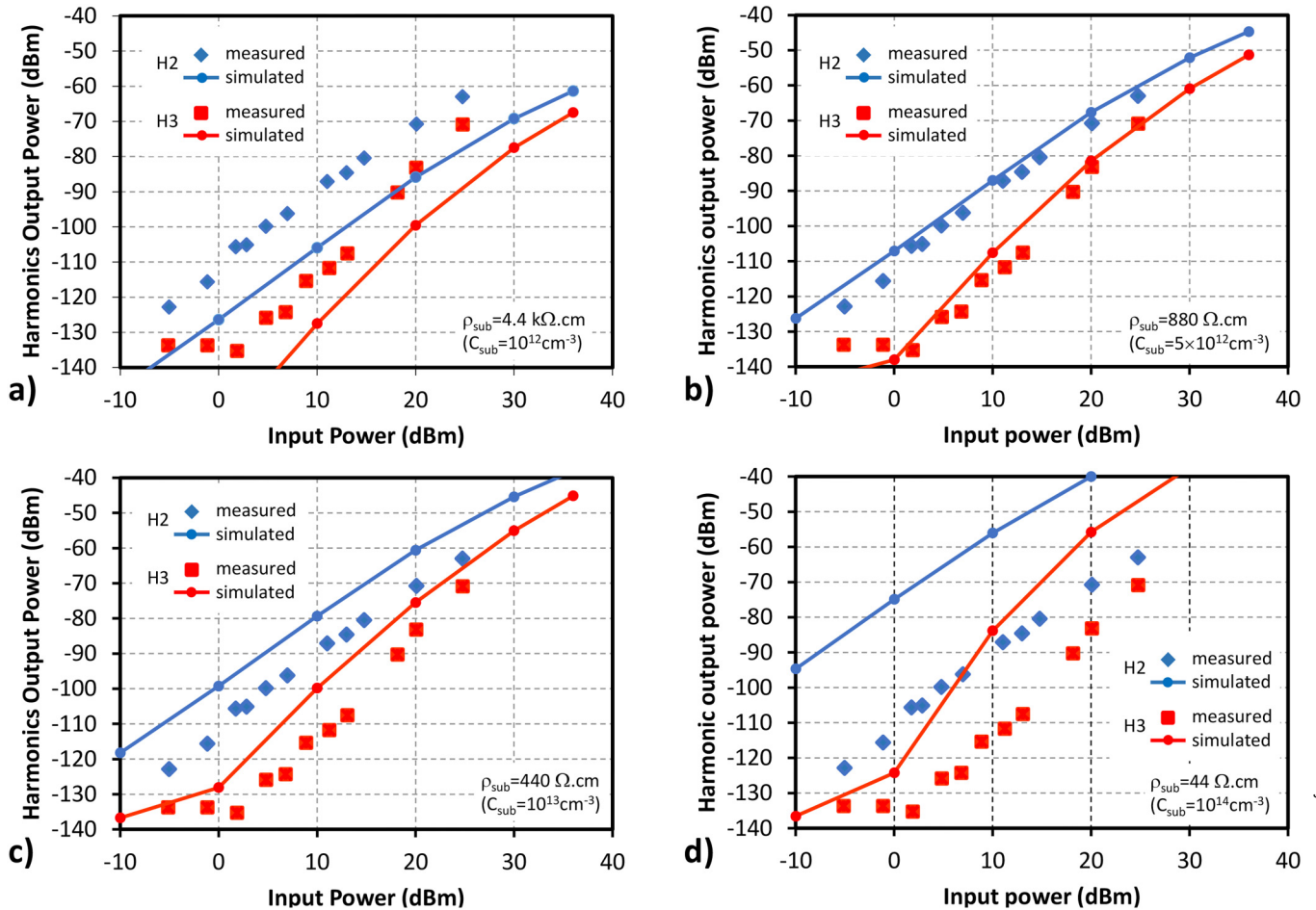
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**FIG. 5.** Spectra associated to power in  $R_{\text{LOAD}}$  deduced from Fourier decomposition of  $V_{\text{LOAD}}$  and  $I_{\text{LOAD}}$ . Graphs (a)–(c) correspond to a simulated CPW of an HR substrate at  $P_{\text{IN}} = -10, 10,$  and  $30 \text{ dBm}$ . Graphs (d)–(f) correspond to a simulated CPW of a TR substrate at  $P_{\text{IN}} = -10, 10,$  and  $30 \text{ dBm}$ .





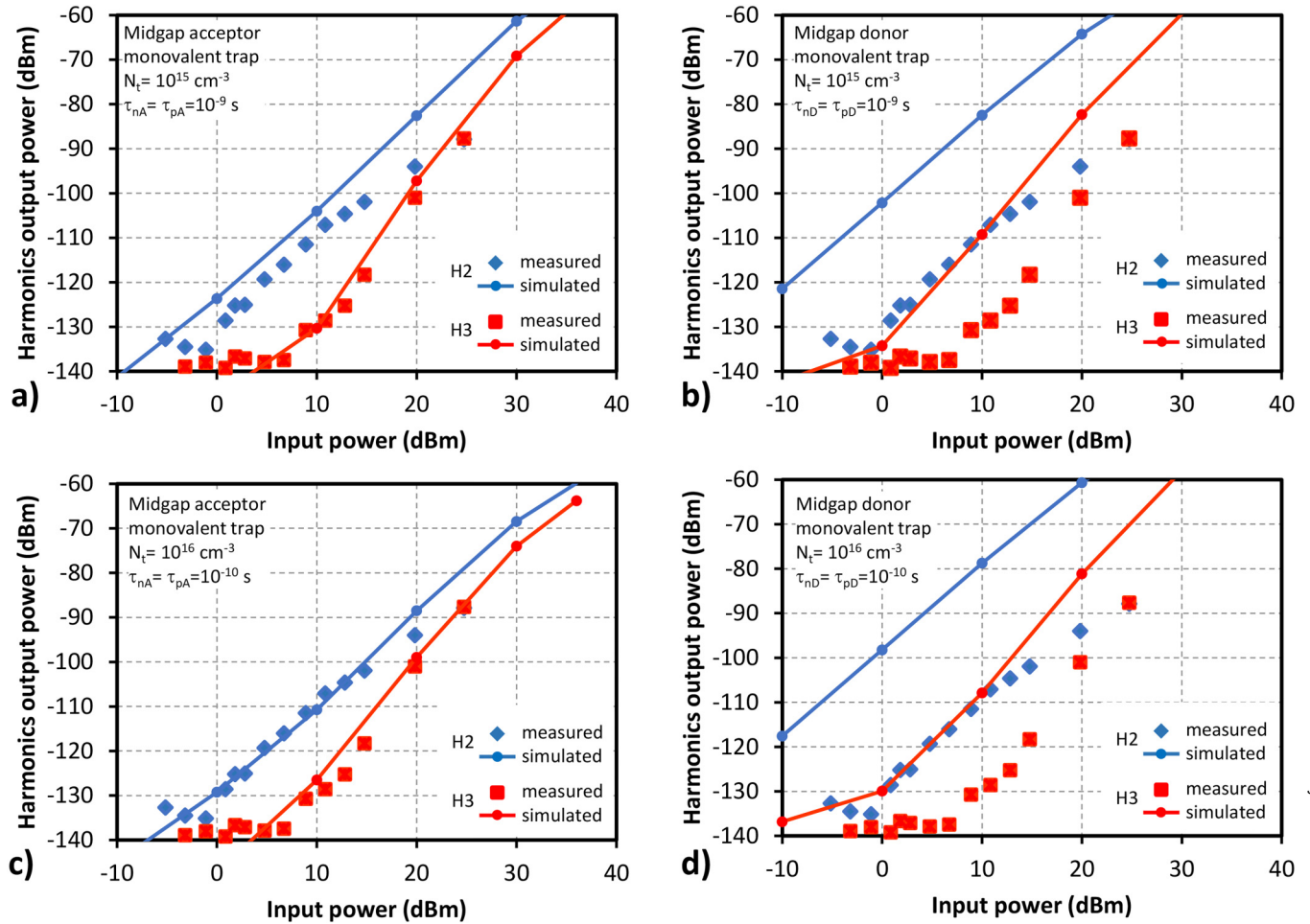
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**FIG. 6.** Second (H2) and third (H3) harmonic power as a function of the injected power in the CPW line on an HR substrate at a frequency of 1 GHz. Full lines represent simulated results and symbols correspond to measurements. Four substrate handler resistivities are considered: (a) 4400 (b) 880, (c) 440, and (d) 45  $\Omega\cdot\text{cm}$ .

- (i) 2D TCAD device simulation employs a finite-difference time-dependent resolution of the Poisson and carrier current continuity equations including the physics for trap modeling as explained in Sec. II B 1. This approach captures the detailed time varying potential and charge dynamics that take place in a domain consisting of a transverse cross section of the CPW line. The 2D TCAD simulation domain is schematically represented by the CPW cross section in Fig. 4(c). This means that the capacitance  $C'$  is replaced here by the TCAD simulation of the 2D cross section of the CPW. In 2D TCAD simulation, the domain width in the direction perpendicular to the 2D cross section is a simple multiplication factor used to scale the current. It is selected according to Eq. (12).
- (ii) TCAD simulations performed in 2D rather than 3D are deliberately chosen for reasons of computational efficiency. However, this approach does not take into account the distributed nature of the line resistance and inductance. These two ingredients are, therefore, re-introduced into the TCAD

simulations in the form of the lumped components  $R'$  and  $L'$ . These elements are determined so as to reflect as closely as possible the 3D behavior of distributed resistance and inductance as explained in Sec. II B 2 based on the work by Ismail *et al.*<sup>13</sup> It is assumed that using a linear RLC network for the sole purpose of estimating  $R'$  and  $L'$  is a reasonable assumption given the low power level of harmonics generated. This method does not in any way affect the ability of the TCAD simulation of the CPW 2D cross section to take full account of the non-linear effects generated by the substrate.

- (iii) In order to reproduce the power measurement setup as closely as possible,  $R_{\text{LOAD}}$  is introduced as a third lumped element in the TCAD simulation to take account of the connection to the power receiver used for measurements. The simulated time-dependent  $V_{\text{LOAD}}$  and  $I_{\text{LOAD}}$  waveforms are processed by FFT to deduce the power of the H2 and H3 spurious harmonics. As shown in Eq. (15), the average power



02 July 2024 14:08:06

**FIG. 7.** Second (H2) and third (H3) harmonic power as a function of the injected power in the CPW line on a TR substrate with a Si n-type substrate handler resistivity of  $880 \Omega \text{ cm}$  ( $C_{\text{sub}} = 5 \times 10^{12} \text{ cm}^{-3}$ ) at a frequency of 1 GHz. Full lines represent simulated results and symbols correspond to measurements. Graphs (a) and (c) correspond to a midgap acceptor monovalent trap with densities  $N_t = 10^{15}$  and  $10^{16} \text{ cm}^{-3}$ , respectively, and lifetimes  $\tau_n = \tau_p = 10^{-9}$  and  $10^{-10} \text{ s}$ , respectively. Graphs (b) and (d) correspond to a midgap donor monovalent trap with densities and lifetimes identical to cases (a) and (c), respectively.

decomposed in Fourier terms is a function of the phase difference between voltage and current, which requires the line resistance and inductance to be taken into account in order to extract harmonic powers representative of the complete transmission line that an isolated 2D cross section cannot capture.

- (iv) From a practical point of view, the 2D simulation domain representing the CPW cross section extends  $100 \mu\text{m}$  above the metal tracks in order to take a proper account of the electric field lines in the air and covers a depth of  $100 \mu\text{m}$  in the substrate handler so as not to impose a boundary condition that disturbs the charge dynamics in the polysilicon region. The ground is applied to the substrate handler under the BOX on either side of the CPW ground tracks to reproduce

their physical connection using a plug through the BOX. A sinusoidal voltage of frequency  $f_0 = 1 \text{ GHz}$  is applied to the input of the device shown in Fig. 4(c). The peak value of the excitation voltage determines the input power  $P_{IN} = 10 \log_{10} \left( \frac{V_{\text{peak}}^2}{2 \times 50 \times 10^{-3}} \right)$  in dBm on a  $50 \Omega$  reference impedance. Particular attention is paid to control the time step of the TCAD simulations, which is taken to be a constant and equal to  $15.625 \text{ ps}$ , resulting in 64 calculated samples over a period. Time sampling with a constant step size eliminates the artifacts associated with interpolation during FFT processing. Four complete periods of the excitation signal are simulated in order to eliminate the spurious transient due to the initialization of the simulation, in particular, the transient due to the initialization of the trap models.

Only the fourth period is used to calculate harmonic power using FFT. It has been verified that the results remain unchanged even when the second or third period is used, thereby confirming that the initial parasitic transient has been completely eliminated.

### III. RESULTS

#### A. Impact of the HR substrate handler resistivity on harmonic generation

Before studying the impact of traps on harmonic generation for a propagation line on a TR substrate, the first step was to simulate the non-linear behavior of the CPW described in Sec. II on an HR substrate. The advantage of this hierarchical approach is twofold. On the one hand, it validates the modeling methodology based on the simplification introduced by the pseudo-3D method. On the other hand, this exercise provides a means to quantify and calibrate the resistivity of the substrate, which will subsequently be introduced into the simulation of the TR substrate. Simulations were, therefore, carried out for four values of HR substrate doping, namely,  $C_{sub} = 10^{12}, 5 \times 10^{12}, 10^{13},$  and  $10^{14} \text{ cm}^{-3}$  associated with n-type resistivities of  $\rho_{sub} = 4400, 880, 440,$  and  $45 \Omega \text{ cm}$ . The results presented in Fig. 6 show the evolution of H2 and H3 harmonics as a function of the input power injected into the transmission line. The power level is calculated by Fourier analysis as described in Sec. II B 3. The non-linear nature of the parasitic MOS capacitance under the buried oxide is responsible for generating harmonics at the line output. It is interesting to note that the level of various harmonics decreases as the substrate resistivity increases.

This is due to the fact that the MOS capacitance contribution associated with the charge variations in silicon under the BOX varies as a square root of the doping level in the accumulation and depletion regimes.<sup>21</sup> Since the resistivity of the substrate handler varies as the inverse of doping, this capacitance, which is a source of non-linearity, generates less harmonics as the resistivity of the substrate handler increases. At low resistivity (44 and 440  $\Omega \text{ cm}$ ), Figs. 6(c) and 6(d) show that harmonics are overestimated and at too high resistivity (4.4 k $\Omega \text{ cm}$ ), Fig. 6(a) reveals that they are underestimated. Finally, a resistivity of 880  $\Omega \text{ cm}$  provides an excellent agreement between simulation and measurement, thus enabling a reference resistivity to be established for CPWs fabricated on an HR substrate.

#### B. Impact of traps on the non-linearity induced by the TR substrate handler

It is clearly established that polysilicon is the host of significant trap densities linked to its polycrystalline nature and, in particular, to the presence of grain boundaries. By definition, any perturbation of the silicon crystal such as surface termination<sup>17</sup> or grain structuring<sup>16</sup> results in the creation of defects whose density, energy distribution over the bandgap, and nature are strongly dependent on the polysilicon deposition process. Even in the case of devices with a single grain, trap distribution is generally represented by a combination<sup>22,23</sup> of (i) two deep-level bands, both acceptor-like and donor-like, with a maximum in the midgap and (ii) two one-sided exponential or Gaussian tails with high density

TABLE I. Trap model parameters for CPW simulation on a TR substrate.

Case	Trap type	Trap density $N_t$ ( $\text{cm}^{-3}$ )	Trap energy (eV) at 300 K	Electron lifetime $\tau_n$ (s)	Hole lifetime $\tau_p$ (s)	Substrate doping $C_{sub}$ ( $\text{cm}^{-3}$ )
a)	Acceptor	$10^{15}$		$10^{-9}$	$10^{-9}$	
b)	Donor		$E_V + E_G/2^a$			$5 \times 10^{12}$
c)	Acceptor	$10^{16}$		$10^{-10}$	$10^{-10}$	
d)	Donor					

<sup>a</sup> $E_G = 1.12 \text{ eV}$  at 300 K for silicon.

near the valence band or the conduction band for the donor and acceptor states, respectively.

In an attempt to model semiconductor devices, the use of such distributions can both provide precision in the way the G–R and the charge state of traps are taken into account but can lead to increased difficulty in interpreting the results and extracting understanding tracks and optimization guidelines. As a general observation, it should also be noted that the generation–recombination mechanism involves the emission and capture of electrons and holes, the occurrence of which is more likely for a trap position at the midgap.<sup>24</sup> In this context, in order to model the behavior of a CPW fabricated on a TR substrate, we have opted to simplify the trap model, namely, the generation–recombination and the trap charge, by only introducing a density of monovalent traps, either acceptors or donors, located at the midgap. The simulation treatment of the CPW on the TR substrate is the same as that used for the HR substrate, with the addition of the charge term in the Poisson equation and the G–R term in the conservation equations for the electron and hole currents. The TR substrate doping level, set at  $5 \times 10^{12} \text{ cm}^{-3}$ , was adjusted in the HR substrate study to obtain the best agreement between simulated and experimental H2 and H3 powers. The results for a reduced set of trap parameters are

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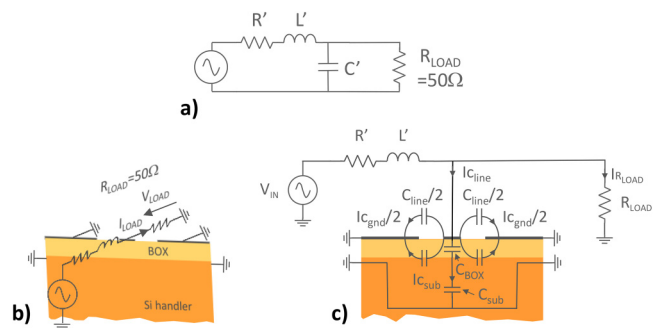
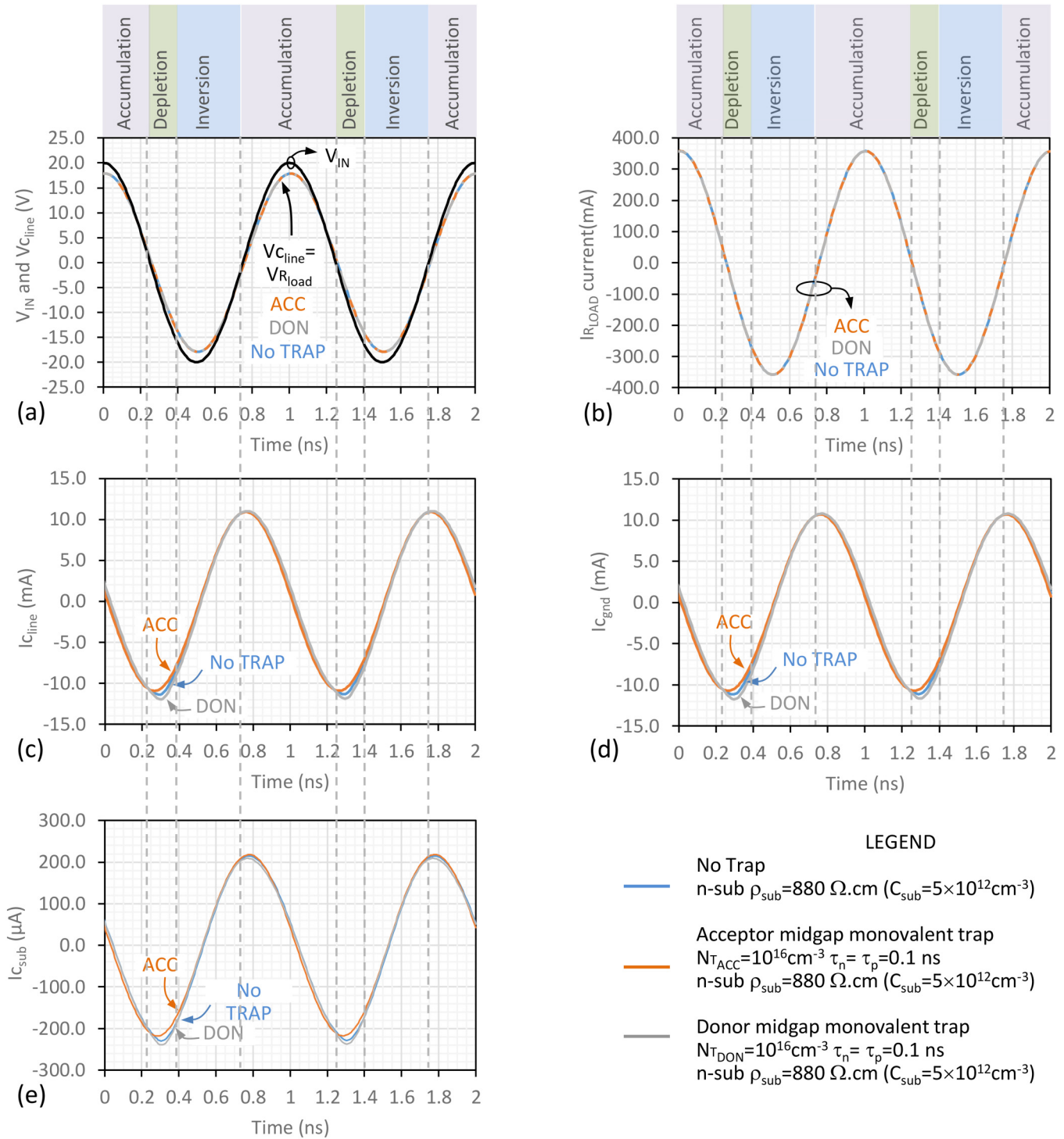


FIG. 8. Schematics of the transmission line based on the pseudo-3D method. (a) Equivalent electrical circuit according to the equivalent RLC Elmore delay.<sup>13</sup> (b) Detailed diagram showing the 2D physical cross section of capacitance  $C'$  and (c) Identification of the various capacitive coupling currents.



02 July 2024 14:08:06

**FIG. 9.** Voltage and current waveforms associated with the electrical schematic in Fig. 8(c). Three cases are considered with the introduction of donor (DON) or acceptor (ACC) traps or without volume defects (No TRAP): (a) input voltage  $V_{IN} = V_{RLOAD} = V_{Cline}$  sine wave at 1 GHz with a peak voltage of 20 V corresponding to a power of 36 dBm, (b)  $I_{RLOAD}$ , current in the resistive load  $R_{LOAD}$ , (c)  $I_{Cline}$ , total displacement current entering the coplanar line capacitor, (d)  $I_{Cgnd}$ , upper partial displacement current coupling to the ground lines, and (e)  $I_{Csub}$ , lower partial displacement current coupling to the ground lines.

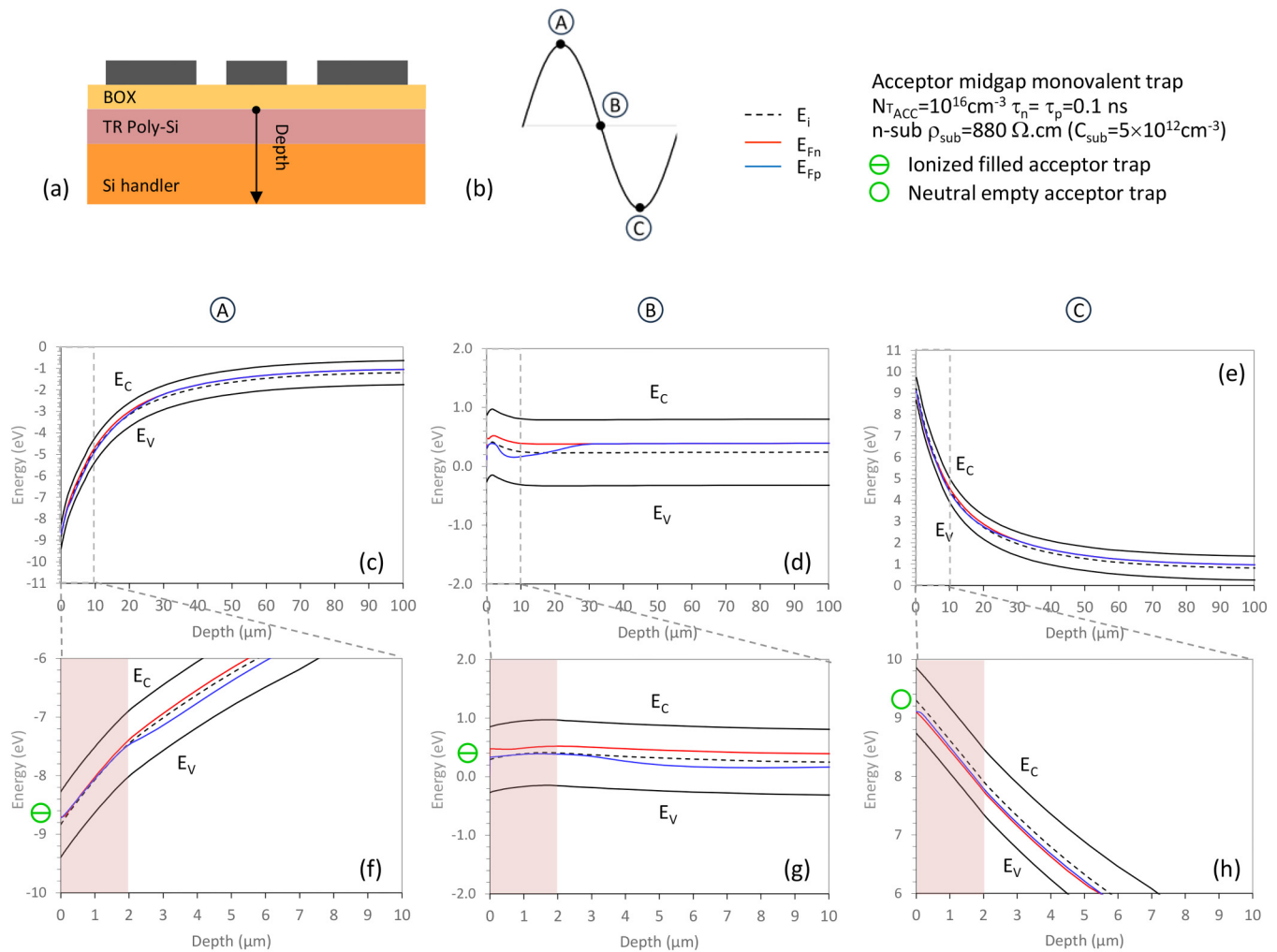
reported here to highlight the most relevant findings. The simulation cases are summarized in Table I.

The results presented in Fig. 7 show the evolution of H2 and H3 harmonics as a function of the input power injected into the transmission line, taking into account volume traps in the polysilicon layer located under the BOX. Figures 7(a) and 7(c) correspond to a monovalent midgap acceptor trap. The simulated results show the beneficial effect of such a defect on minimizing harmonic distortion. On the other hand, Figs. 7(b) and 7(d) corresponding to the introduction of midgap donor monovalent traps with densities and lifetimes identical to cases (a) and (c) suffer a slight

degradation compared with the simulation case without traps [Fig. 6] and a fairly wide discrepancy with the measured data.

#### IV. DISCUSSION

In order to gain a better understanding of the antagonistic effects obtained by the introduction of acceptor and donor traps, this section proposes a detailed analysis of the charge dynamics involved in the silicon substrate handler close to the BOX and the polysilicon layer. To this end, Fig. 8 first provides two equivalent schematics of the transmission line based on the pseudo-3D

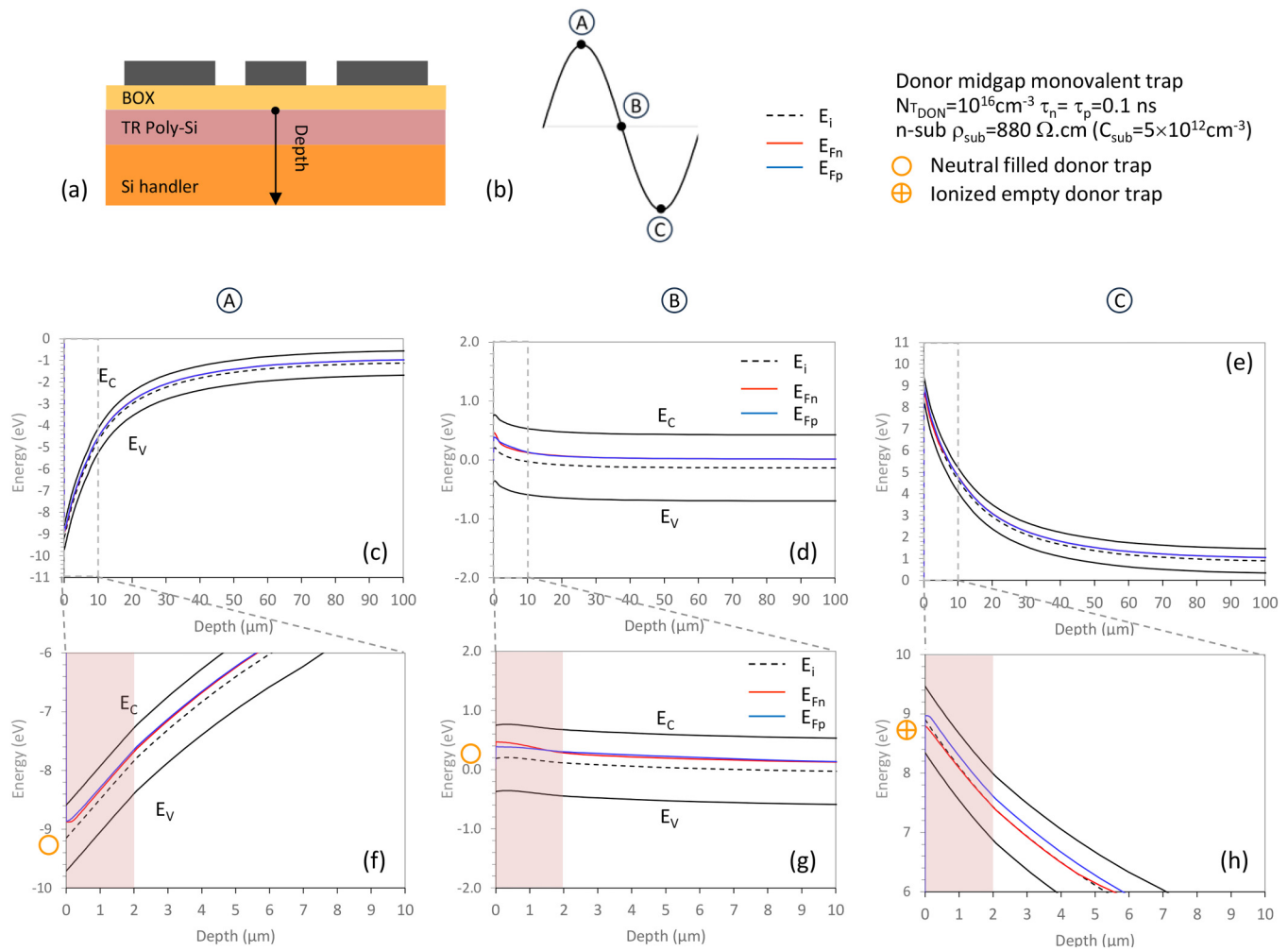


02 July 2024 14:08:06

**FIG. 10.** Case of a monovalent acceptor trap. Energy band diagrams extending from the underside of the BOX into the trap-rich polysilicon layer and the silicon substrate handler. (a) The outline is taken under the central track of the CPW. Energy diagrams are the result of a time-dependent simulation with excitation at 1 GHz. (b) The three cases A, B, and C correspond, respectively, to the positive peak voltage of 10 V (accumulation), 0 V (depletion), and the negative peak voltage of -10 V (inversion) of the excitation wave. (c)–(e) The series of three graphs in the middle shows the curvature of the bands over the entire depth of the simulation domain. (f)–(h) The series of three graphs at the bottom shows a zoom of the band structure extending over the first 10  $\mu\text{m}$  of depth with the trap-rich layer shown by a colored background.  $E_C$ ,  $E_V$ , and  $E_i$  are the conduction, valence, and intrinsic energy levels, respectively, and  $E_{Fn}$  and  $E_{Fp}$  are the quasi-Fermi energy levels for electrons and holes, respectively.

method developed in Sec. II. In particular, Fig. 8(c) details different components of the total current  $I_{c_{line}}$  entering the capacitance. It comprises the coupling current to the ground planes of the coplanar line ( $I_{c_{gnd}}$ ) and the coupling current with the silicon substrate ( $I_{c_{sub}}$ ). Clearly, the  $I_{c_{sub}}$  current is non-linear because the space charge in the polysilicon layer and the substrate handler varies non-linearly with the potential. It should be noted that the  $I_{c_{gnd}}$  component is also likely to introduce a non-linear deviation insofar, as the field lines between the central track and the ground planes of the coplanar line partly intercept the substrate handler.

In quantitative terms, Fig. 9 describes the waveforms associated with the different currents and voltages depicted in Fig. 8. Each waveform is represented for three cases associated with the presence of acceptor traps (ACC), donor traps (DON), or without traps (No TRAP), respectively. First, Fig. 9(a) shows the time evolution of the line capacitance voltage. The latter is slightly shifted in phase and attenuated with respect to the input voltage, as expected, but without any appreciable distortion with respect to the sine wave. The same observation is valid in Fig. 9(b) for the current flowing through the load, whose peak value reaches  $\sim 350$  mA and for which non-linear



**FIG. 11.** Case of a monovalent donor trap. Energy band diagrams extending from the underside of the BOX into the trap-rich polysilicon layer and the silicon substrate handler. (a) The cutline is taken under the central track of the CPW. The energy diagrams are the result of a time-dependent simulation with excitation at 1 GHz. (b) The three cases Ⓐ, Ⓑ, and Ⓒ correspond, respectively, to the positive peak voltage of 10 V (accumulation), 0 V (depletion), and the negative peak voltage of  $-10$  V (inversion) of the excitation wave. A sinusoidal excitation signal with a peak voltage of 10 V was used to facilitate the graphical representation of the bands and to reduce the variation range in a situation of strong curvature. (c)–(e) The series of three graphs in the middle shows the curvature of the bands over the entire depth of the simulation domain. (f)–(h) The series of three graphs at the bottom shows a zoom of the band structure extending over the first  $10 \mu\text{m}$  of depth with the trap-rich layer shown by a colored background.  $E_C$ ,  $E_V$  and  $E_i$  are the conduction, valence, and intrinsic energy levels, respectively, and  $E_{Fn}$  and  $E_{Fp}$  are the quasi-Fermi energy levels for electrons and holes, respectively.

deformations are not visually detectable. Figures 9(c)–9(e), respectively, describe the line capacitance currents  $I_{C_{\text{line}}}$ ,  $I_{C_{\text{gnd}}}$ , and  $I_{C_{\text{sub}}}$  functionally related by the conservation law  $I_{C_{\text{line}}} = I_{C_{\text{gnd}}} + I_{C_{\text{sub}}}$ . These currents, whose amplitudes are much smaller than the current flowing in the terminal load, bear notable non-linear deformations at the negative end of the waveform for the no trap (No TRAP) and donor traps (DON) cases. On the other hand, the introduction of acceptor-type volume traps (ACC) does not lead to any appreciable degradation of the waveform compared with the ideal harmonic wave, which represents a significant improvement in terms of harmonic reduction compared with the other two cases.

The modeling results shown in Fig. 9 legitimately raise two questions:

- (i) Why are non-linear deformations only observable at the negative end of the current waves?
- (ii) What is the mechanism underlying the decrease in non-linear effects in the presence of acceptor traps and their increase in the case of donor traps?

In order to answer the first question, it is important to remember that the characteristic describing the variations of a metal-oxide-semiconductor (MOS) capacitor as a function of the metal (here, the central track of the CPW) voltage exhibits a highly non-linear behavior.<sup>21</sup> The total MOS capacitance is made of the series combination of the BOX capacitance and the semiconductor capacitance. The total capacitance is reduced to the BOX capacitance in the strong inversion and accumulation regimes because the capacitance that develops in silicon is extremely large. The non-linear operation can also be attributed to the depletion mode of operation. Referring to Figs. 9(c)–9(e), it is possible to associate the operation in the depletion mode with the negative ends of the waveform of currents  $I_{C_{\text{line}}}$ ,  $I_{C_{\text{gnd}}}$ , and  $I_{C_{\text{sub}}}$  where non-linear signal distortions are noticeably involved. The time intervals 0.25–0.40 and 1.25–1.40 ns are identified as corresponding to the depletion mode of operation for which the total line capacitance exhibits a strong non-linear behavior.

In order to address the second question on the mechanism underlying the decrease in non-linear effects in the presence of acceptor traps and their increase in the case of donor traps, it is instructive first to examine the charge state of the acceptor or donor traps as a function of the operating mode of the MOS capacitance associated with the CPW on the TR substrate. With regard to the case of monovalent acceptor traps, Fig. 10 shows energy band variations as a result of a time-dependent sine wave excitation at 1 GHz. The cutline extends from the underside of the BOX into the trap-rich polysilicon layer and the silicon substrate handler. The three cases (A), (B), and (C) correspond, respectively, to the positive peak voltage of 10 V (accumulation), 0 V (depletion), and the negative peak voltage of –10 V (inversion) of the excitation wave. Here, a sinusoidal excitation signal with a peak voltage of 10 V was used to facilitate the graphical representation of the bands and to reduce the variation range in a situation of strong curvature. At both peak values (A) and (C), significant band bending is observed in silicon, resulting from the rapid variations in the electric field under 1 GHz excitation. These variations in the electric field are responsible for the displacement current in the MOS structure, which largely

dominates the electron and hole conduction currents. The graphs referred to in Figs. 10(f)–10(h) show a close-up view of the trap-rich polysilicon layer. In case (A), it can be clearly observed that the Fermi level pinning to the trap energy (midgap) remains effective in the trap-rich layer where both quasi-Fermi levels coincide. It should also be noted that there is a favorable situation in which the negative charge carried by the ionized acceptors compensates for the positive depletion charge at the origin of the non-linear effects.

Figure 11 represents for donor traps what Fig. 10 is for acceptors. The same type of band bending is observed at first inspection, with the notable difference that no Fermi-level pinning results from the presence of the donor traps. On the contrary, between (B) and (C), the transition from a neutral state to a positively charged state of the ionized donors does not counterbalance the depletion charge but contributes to its strengthening.

## V. CONCLUSION

Using a test vehicle consisting in a coplanar waveguide (CPW) deposited on the BOX of an SOI substrate, we have developed a modeling strategy based on the time-dependent resolution of the Poisson and current continuity equations to properly capture the charge dynamics accounting for the non-linear effects. Time-dependent periodic voltage and current waveform are subsequently processed using Fourier analysis to deduce the power of generated harmonics. Based on a reduction method proposed by Ismail *et al.*,<sup>13</sup> we have shown that it is possible to restrict the analysis to a two-dimensional cross section treatment of the CPW by converting the distributed nature of the transmission line into a second-order equivalent lumped circuit. This approach made it possible to reproduce the effect of increasing the substrate resistivity on the reduction of the 2nd and 3rd harmonics, resulting in an excellent agreement with the experimental data when the resistivity of the HR substrate is set to 880  $\Omega$  cm. Based on this validation of the simulation method, we chose to simulate the non-linear response of the transmission line on the trap-rich SOI substrate by simplifying the trap distribution model. To avoid the adoption of an unverified trap distribution across the bandgap<sup>16,22,23</sup> known to be strongly dependent on the polysilicon deposition process, a midgap monovalent trap density was introduced, either acceptor or donor density. A monovalent density of acceptor traps with a concentration of  $10^{16}$   $\text{cm}^{-3}$  and a carrier lifetime of 0.1 ns enabled the experimental data to be reproduced very accurately, with a substantial reduction in the 2nd and 3rd harmonics. A detailed analysis of the displacement current waveforms explains the beneficial role of the negatively ionized acceptor traps in compensating for the positive depletion charge near the polysilicon/substrate handler interface. This scenario of charge compensation is not found to be possible in the case of donor traps.

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02 July 2024 14:08:06

## AUTHOR DECLARATIONS

## Conflict of Interest

The authors have no conflicts to disclose.

## Author Contributions

**Justine Philippe:** Formal analysis (equal); Investigation (equal); Methodology (equal); Software (equal); Validation (equal); Writing – original draft (equal). **Jean-François Robillard:** Investigation (equal); Supervision (equal); Validation (equal); Writing – review & editing (equal). **Daniel Gloria:** Funding acquisition (equal); Resources (equal); Supervision (equal); Validation (equal); Writing – review & editing (equal). **Emmanuel Dubois:** Conceptualization (lead); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Supervision (equal); Validation (equal); Writing – original draft (lead); Writing – review & editing (lead).

## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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