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Streamlined Models of CMOS Image Sensors Carbon Impacts

Olivier Weppe

Univ. Rennes, INSA Rennes
CNRS, IETR - UMR 6164
F-35000 Rennes, France
olivier.weppe@insa-rennes.fr

Jérôme Chossat

STMicroelectronics
AMS/ Imaging Division
Grenoble, France
jerome.chossat@st.com

Thibaut Marty

Univ. Rennes, INSA Rennes
CNRS, IETR - UMR 6164
F-35000 Rennes, France
thibaut.marty@insa-rennes.fr

Jean-Christophe Prévotet

Univ. Rennes, INSA Rennes
CNRS, IETR - UMR 6164
F-35000 Rennes, France
jean-christophe.prevotet@insa-rennes.fr

Maxime Pelcat

Univ. Rennes, INSA Rennes
CNRS, IETR - UMR 6164
F-35000 Rennes, France
maxime.pelcat@insa-rennes.fr

Abstract—With the escalating concern about global warming, the environmental impact of electronic devices must be scrutinized. Life Cycle Assessments (LCA) reveal that Integrated Circuits (ICs) are the primary contributors to greenhouse gas emissions in these devices. However, performing an inventory to determine the ICs impact is a complex task due to missing data and the existing studies on ICs have been neglecting CMOS Image Sensors (CIS).

Despite the surge in CIS usage, particularly in smartphones, there is a lack of comprehensive models to assess their environmental impact. This paper proposes a multi-level set of models that leverage available information while considering the specificities of CIS. The most comprehensive model incorporates factors such as the total silicon area, geographical location (influencing the energy mix), and the technology node. To accommodate scenarios with incomplete data, subsequent models are designed to effectively utilize averaged parameters.

The proposed models are applied to sensors manufactured by STMicroelectronics and Sony, and the results are compared with existing LCA results from Fairphone. Our approach provides a more comprehensive understanding of the environmental impact of CIS, contributing to the broader goal of reducing the carbon footprint of electronic devices. Our results suggest that the carbon impact of a Fairphone 4 image sensor is likely higher than previously estimated, with a significant gap between our findings and the expected value.

Index Terms—Carbon Footprint, CMOS Image Sensors (CIS), Environmental Impact, Greenhouse Gas Emissions, Integrated Circuits (ICs), Life Cycle Assessment (LCA)

I. INTRODUCTION

The escalating carbon impact of the electronics industry underscores the global urgency to adhere to the 2050 Paris Agreement [1]. As the environmental footprint of electronic devices continues to grow, it becomes imperative to enhance their sustainability.

Over the past two decades, the electronics industry has made significant strides in managing the energy consumption of devices in their usage phase, primarily to ensure adequate battery life for the user. However, as these devices become increasingly complex, the carbon impact of portable terminals is

now predominantly concentrated in the manufacturing process, with integrated circuits playing a major role [2].

The scarcity of detailed information pertaining to the fabrication process poses significant challenges in accurately assessing the carbon footprint of silicon-based devices. In this study, we propose a methodology that relies on existing data from literature coupled with available technical information. We demonstrate how this can be leveraged to assess the environmental impact of imaging sensors.

Our contributions are:

- We propose three models to estimate the carbon emission of a CIS, usable in accordance with the available information about the component.
- We show that current LCA studies underestimate the carbon impact by a factor 2 when neglecting the strong impact of wafer stacking, which doubles the silicon area in CIS.

II. MOTIVATION

While there is a correlation between carbon emissions and semiconductor node [3], the device's primary System-on-Chip (SoC) area remains relatively stable, with an area around 1 square centimeter as shown in Figure 1. Nonetheless, the total

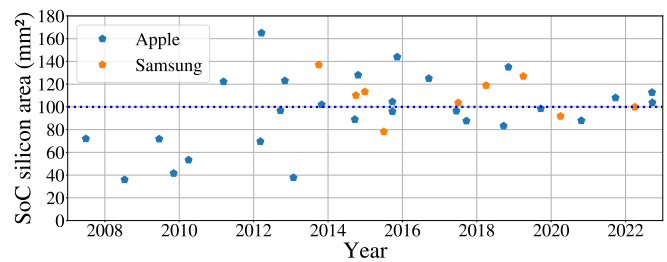


Fig. 1. Smartphone SoC silicon area from Apple and Samsung, based on data from [4] and [5]

silicon area in a mobile phone continues to expand. This trend

is partly due to the increasing area and number of CIS in terminals. This escalation is primarily driven by the pursuit of higher resolution while preserving sensitivity and providing effects similar to Digital Single-Lens Reflex cameras (DSLRs) like depth of field and bokeh¹, which are promoted as selling points, especially for high-end products [6]. The environmental impact of these sensors must be seriously considered as they start to contribute significantly to the Global Warming Potential (GWP) of a device.

Mobile phones began capturing images in the early 2000s. Initially, the image quality provided by CMOS sensor technology was subpar. However, as the technology evolved, mobile cameras are now often used as substitutes for full-frame regular cameras [6]. The industry adapted to this evolution by offering more capable cameras as a differentiation factor in the competition [7]. The compactness of the device necessitates some compromises on the embedded camera. The main issue with the lack of space, especially in depth, is the limited capabilities of the optical path, restricting light sensitivity and flexibility like variable magnification factor. To address this issue, phone vendors started to provide multiple sensors in a single device [6]. For instance, one sensor is dedicated to general high-quality pictures, one for a large field of view, another for long-range, and one on the display side of the camera dedicated to visual calls or “selfies”. This trend towards a higher number of CIS in a single phone is illustrated in Figure 2. On this graph, the number of available cameras per device is shown for each phone found on a large cell phone database [8], where each point represents a model of a “camera-phone” among 2348 references. As the points are displayed in chronological order, it is clear that there was a surge in the number of CIS in the 2010s. The first “smartphones” in the 2000s were limited to a single camera (iPhone 1, Samsung Galaxy S), whereas in the 2020s, high-end devices commonly use 4 or 5 cameras (for example, the iPhone 14 Max or the Samsung Galaxy S23 Ultra).

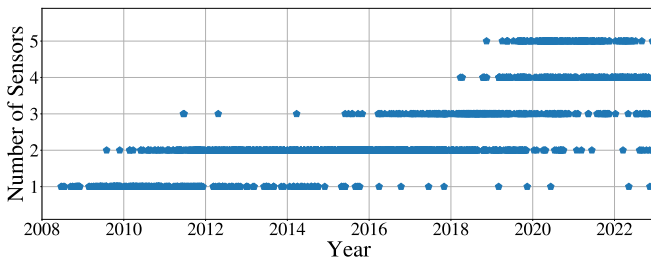


Fig. 2. Number of camera sensors per smartphone

The increase in the total area of silicon is not solely attributable to the rise in the number of cameras. Despite the pressure of compactness, the size of the sensors tends to increase, especially for the main sensor. Indeed, the main sensor is the “go-to” camera that will suit most purposes for

¹Blur effect produced in the out-of-focus parts of an image, typically achieved through a large aperture or a specific lens design, that draws attention to the subject.

the user. This sensor receives most of the attention during the terminal design, as its specifications are determinant for the client. It usually supports a large number of pixels (up to 20 MPixels [9]) and has a large die to increase their sensitivity in dim light situations. Figure 3 shows the millions of pixels supported by the main camera of the phones from the same database [8].

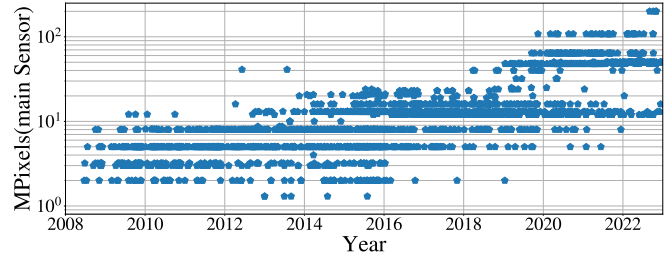


Fig. 3. Millions of pixels in the main camera for each smartphone

As a result, CIS have emerged as a significant factor in the carbon footprint of smartphones. The details pertaining to the production process of semiconductors are often classified as confidential, as they could provide an advantage to competitors, making it challenging to obtain the necessary data for a comprehensive Life Cycle Assessment (LCA) inventory. To address this issue, we suggest an approach that utilizes streamlined models dependent on readily accessible information. Although this research primarily concentrates on GWP, other aspects like water consumption or power usage can be examined similarly.

III. RELATED WORK

In 2002, Williams et al. published a pioneering work on the environmental impact of integrated circuits [10]. This work details the workflow, materials, and energy required to fabricate a silicon chip. Despite the tremendous evolution in the technology and processes used to produce an integrated circuit over the last two decades, this work is one of the first attempts to highlight the significant carbon impact of silicon die fabrication.

Boyd et al. of [11] have conducted extensive work on characterizing the environmental impacts of integrated circuits. This work lays the foundation and methodology for a more precise evaluation of chemical, water, and power usage. While many aspects of this work remain valid, the ecological footprint of IC manufacturing has grown significantly since its publication. A notable conclusion of this study is the predominance of the use phase relative to the fabrication of the circuits. This trend has now reversed, particularly with the latest technology nodes, which are much more complex and therefore more resource-intensive [1].

In more recent work, authors of [3] developed a model to estimate the impact of fabricating a silicon wafer based on various parameters. A particular point of interest is the model support for technologies ranging from 32 nm to 3 nm. By merging the results from [11] and [3], the entire range of

technologies from 350 nm to 3 nm is covered. However, in a comprehensive survey of the existing literature, Pirson et al. [12] highlight the discrepancies that stand out when comparing the results provided by different LCA studies.

Some studies propose distinct models for different CMOS chip categories (DRAM, CPU, Flash) [13], [11], [14]. Indeed, the internal structure and packages of these components are quite different from one another, necessitating a specific model. To the best of our knowledge, none have been established for CIS. However, the internals of image sensors, with specific features like pin-diodes, micro-lenses, or colour filters [15], are also very different and require a dedicated model.

The Life Cycle Analysis (LCA), as described in ISO 14044, is based on an inventory [16] of the elements (flows) that make up the component, called the Life Cycle Inventory (LCI). Like other silicon devices, CMOS image sensors suffer from a lack of information [17].

In [18] Eeckhout et al. propose a different approach based on macroscopic parameters, which makes the carbon impact estimation much more feasible in practice. This latter methodology is particularly interesting because it relies on easily available data, which can be broadly used. In our study, we apply this concept to the specific case of image sensors.

IV. METHODOLOGY

The evaluation of the carbon impact of silicon devices encompasses three phases of the component's life:

- The impact of fabrication, also known as embodied emissions, includes the extraction of materials at mines, the energy and chemicals used during the production of the pure silicon crystal, and the integration of the design onto the silicon die.
- The use phase accounts for the electrical energy used during the capture of an image (Active power), as well as the electrical power drawn when the device is powered up but not in use (Idle power).
- The end-of-life phase regroupes the impacts related to the end-of-life of the device. Due to the very low recycling level for semiconductors, the end of life will not be considered in this study (assumed as zero). However, recycling CIS should be possible, especially with high-end (and expensive) devices [19].

The total carbon impact of a CIS, expressed in equivalent CO₂ (CO₂e) [20], is the sum of the impact resulting from all three phases, and can be summarized in Equation 1, where G is the total GWP for the device, G_{fab} is the GWP of the fabrication, G_{use} is the GWP due to the electrical energy consumption during the use phase of the device and G_{EOL} is the GWP of its end-of-life.

$$G = G_{fab} + G_{use} + G_{EOL} \quad (1)$$

A. CMOS image sensor life cycle

1) *Use phase*: As energy consumption is key information when engineering a portable device for critical battery lifetime reasons, power usage is often provided in the documentation

of the sensors. Typically a component datasheet exhibits an Idle power and a Use power. The difference between those two states comes from the fact that the sensor consumes much more energy when a picture is being captured, which includes video recording, still image capture, as well as continuous image preview. There is usually a large gap between idle power p_{idle} and use power p_{use} , which can lead to strong variation between the different use cases considered. The Functional Unit (FU) used in the LCA must reflect a typical usage of the device. Equation (2) considers a Use time t_{use} and an Idle time t_{idle} . Several use cases can be studied to give an overview of the variety of FUs that can apply to the CIS. For instance: the life-cycle of a surveillance camera providing a continuous stream of images (always in Use power mode) or a cellphone camera (mostly in Idle power mode). After the total energy is calculated to determine the global warming impact of the use phase, the energy mix in the location where the device is used must be introduced to convert the energy value into GWP impact using carbon intensity T_{loc} in g/W h, which translates the electrical energy used into equivalent CO₂ emission. This is summarized in Equation (2), in which all parameters are easily accessible, once a proper use scenario is determined. Depending on country of use, T_{loc} ranges from 60 g CO₂e/kWh to 1 kg CO₂e/kWh.

$$G_{use} = T_{loc} \cdot (p_{use}t_{use} + p_{idle}t_{idle}) \quad (2)$$

2) *Fabrication*: The fabrication phase of semiconductor devices is known to have a significant share in the GWP impact [1]. However, finding precise data to estimate the carbon impact of a silicon device is not always possible. This study will focus on this aspect to provide streamlined models to determine this part of the carbon contribution of a given CIS. The main factors that affect the GWP of an imaging device are its silicon area (S), the process operations to build the component ($Proc$), and the location of the facility (Loc_{fab}). We need to determine a model such that:

$$G_{fab} = f(S, Proc, Loc_{fab}) \quad (3)$$

One important factor to notice is that image sensor features, especially photodiodes, are quite large compared to state-of-the-art transistors embedded in digital computing devices, thus a larger process node is often used. The first CMOS sensors were produced in 1200 nm [21] and technology shrinking has done its work, especially for compact embedded devices. As of 2024, cell phone sensors use technologies in the range of 40 nm. For bigger sensors, used in DSLRs, larger pixels are used for which it is easier to rely on larger technology. Figure 4 shows the typical structure of a Back-Side Illumination (BSI) pixel.

We will restrict the range of possible technology nodes between 180 nm and 40 nm to match state-of-the-art. The work of [11] compiles the GWP for the technologies within this range. Having these results from the same study is particularly relevant since the environmental impact assessment of each technology node is based on a common methodology. This reduces the strong variability observed between studies [12].

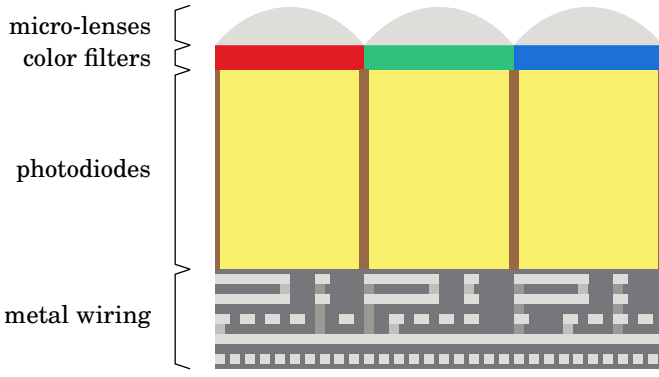


Fig. 4. Structure of a back-side illumination pixel

Fetching the GWP for each technology node from different studies would have led to inconsistent figures and therefore more complex to interpret.

B. Main parameters

Fabrication impact is a function highly dependent on the silicon area. A typical simplification in life cycle analysis methodologies is to provide the carbon impact per silicon area. A typical simplification is to assume that the GWP is proportional to the area of the device. This simplification is common in LCA studies, where a practical reference flow is either a wafer or a die. The proportional relationship hypothesis stands as long as the area is not too large as the yield may be reduced with larger devices (much larger than 1 cm^2) due to the increased probability of defect on a large silicon area. Regarding this aspect, CIS benefit from a particularity compared to other CMOS chips: its die is directly visible, and measuring the surface area may seem like a straightforward operation. Furthermore, this information is often made publicly available in datasheets of the components, mainly to help in the design of the optical path to the sensitive surface.

However, the area is not sufficient by itself, because there is a significant variability between process nodes [12]. The technology used to produce the silicon die is therefore a significant parameter too.

At last, the GWP emission depends on the electrical energy needed to produce the component. The location of the factory is important due to differing energy mixes. As most factories are located in Asia, they rely on fossil fuel, especially coal which has a higher impact of about $1\text{ kg CO}_2\text{e/kWh}$.

Unfortunately, those 3 parameters (Silicon Area, Process node, Factory location) are not usually covered in the component documentation. However, some partial information can be gathered to increase the precision of the fabrication impact estimation. In this case G_{fab} is expressed as (4), where S is the silicon area, $Proc$ is the technology node and Loc_{fab} is the location of the factory:

$$G_{fab} = S \cdot h(Proc, Loc_{fab}) \quad (4)$$

To refine this equation, we split the embodied GWP into two parts. The first one, associated with the electrical energy consumption at the factory site, is dependent on the local energy mix as expressed in the carbon intensity T_{loc} . The second one, for which the electrical carbon intensity cannot be determined precisely, is related to the fabrication of the silicon substrate in the form of silicon ingots, and later blank silicon wafers. Those are done by an external provider, and so are the chemicals used for the fabrication of the image sensors. For this reason, the impact of the electrical energy E used for the fabrication of the device must be separated in Equation (4) from the impact of infrastructure, factory, chemicals and raw materials K that we will name *ancillary impact*. We will then propose a general model in the form of Equation (5).

$$G_{fab} = S \cdot (E \cdot T_{loc} + K) \quad (5)$$

In order to determine the values of E and K , the extensive data reported in [11] has been used. Despite being quite old regarding technical progress in wafer fabrication, the technologies nodes used by CIS are covered. However, getting access to precise values of E and K is not straightforward. Indeed, in Boyd's work, embodied GWP is reported in detail for different aspects of the process: fabrication, infrastructure, chemicals, silicon and transport. Unfortunately, values called *fabrication* and *infrastructure* are composite values, comprised of the impact of electric energy during the fabrication E , and ancillary emissions K . Knowing the electrical conversion factor used in Boyd's work, we were able to separate parameters K and E . Table I summarizes these results for technology nodes ranging from 180 nm to 32 nm.

TABLE I
GWP FROM EMISSIONS AT VARIOUS STEPS OF THE MANUFACTURING PROCESS PER mm^2 IN gCO_2e ADAPTED FROM [11]

process node nm	ancillary carbon emission (K) $\text{g CO}_2\text{e}/\text{mm}^2$	Electrical energy (E) Wh/mm^2
180	16.4	87
130	11.7	77
90	14.5	85
65	16.0	99
45	19.2	121
32	20.1	129

Once the electrical power consumption is known, we need to apply a carbon intensity factor to assess the GWP due to electricity. In fact, knowing the vendor gives us the fabrication site(s) location(s), which has a strong impact on the estimated GWP. This value can be deduced by identifying the corresponding energy mix. Table II shows the estimated factory location dedicated to CIS fabrication based on official communication from main vendors [22], and the corresponding carbon intensity [23].

When considering the location reported in this table, even though major silicon manufacturers have wafer production sites scattered across the globe [24], there's a noticeable

TABLE II
LOCATION (2023) AND ASSOCIATED CARBON INTENSITY (2022) PER CIS
FOR MAJOR VENDORS

Name	Market share	Location	Intensity (T_{loc}) g CO ₂ e/kWh
SONY	42%	Japan	435
Samsung	19%	South Korea	438
OmniVision	11%	China	534
ST Micro	6%	France	85
Onsemi	6%	USA	368
SK Hynix	5%	South Korea	438

correlation between the nationality of the vendor and the location of the CIS fabrication site. However, this information is subject to change as new factories are being built. The reality is even more complex as several factories, in different locations, can be involved in the complete fabrication of the final chip.

C. Models

Once the most significant parameters have been identified, it is possible to propose models to assess the GWP due to CIS fabrication.

1) *Area + Vendor + Technology node*: When both the process node and the factory location are known, we propose a model of the GWP for the imaging device as shown in Equation (6) where E_{nm} and K_{nm} are the electrical energy consumption and the ancillary GWP emissions respectively for the considered technology node as given in Table I, T_{loc} is the electrical carbon intensity from Table II and S is the silicon area:

$$G_{Fab} = S \cdot (E_{nm} \cdot T_{loc} + K_{nm}) \quad (6)$$

Despite the advantage of having an accessible die area, the reality is more complex: as technology evolves, CIS designers maximize the exposed sensitive area for a given package size. This leads to the BSI technology that gets rid of the metal traces that obstruct the photodiodes. Then, a new generation of CIS uses wafer stacking to locate control, memory and processing directly below the sensitive area, on a separate die that is connected to the sensor die using direct bonding [25], as illustrated in Figure 5. In the case of a CIS using wafer stacking, the silicon area from each layer must be added to determine the total carbon impact. Sony also demonstrated 3-stacked-layer devices [26], which renders the GWP estimation more difficult, but stacking 3 layers of wafers is uncommon, mainly due to the technology costs involved. Since 2-layer stacking has become predominant in the CIS production, especially for embedded devices like smartphones, the methodology for the evaluation of the environmental impact of CIS requires taking into account this key characteristic. To the best of our knowledge, this work is the first to consider stacking when evaluating GWP of an image sensor.

For multi-layer sensors, the total GWP is the sum of the impact for each layer. A more general expression of the model

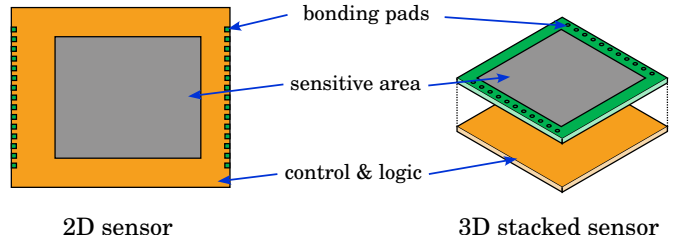


Fig. 5. Traditional 2D sensors (left) expose the whole die surface, while 3D stacked sensors hide the logic surface below the sensitive surface (right)

for N layers is shown in Equation (7), where, for each layer, S_i is the silicon area, E_i is the electrical energy consumption for each technology node and K_i is the GWP emissions due to the fabrication.

$$G_{Fab} = \sum_{i=1}^N S_i \cdot (E_i \cdot T_{loc} + K_i) \quad (7)$$

2) *Area + Vendor*: Without additional prior knowledge about the process node used to produce the wafers, an average technology can be selected. We choose an average technology of 65 nm for K_{avg} and E_{avg} with respective values of 16.0 g CO₂e/mm² and 99 Wh/mm² from Table I. In this case, when the 3D stacking technology is used, all the silicon layers are supposed to be based on this same average technology node. The total surface of silicon S_{total} must be determined to account for silicon area of the different silicon layers.

$$G_{Fab} = S_{total} \cdot (E_{avg} \cdot T_{loc} + K_{avg}) \quad (8)$$

3) *Area model*: When most information is missing, a simple way to estimate the carbon impact of a CIS is to only rely on the silicon area (S). This is the model with the highest uncertainty, as the dependencies on the location or the process are unknown. We can use in the model 1) a global average factor K_{glob} , that is independent on the factory location and the type of process used.

$$G_{Fab} = S_{total} \cdot K_{glob} \quad (9)$$

Without prior assumption about the technology used, we propose an average of 3 kg CO₂e/cm² for K_{glob} , as it is a middle point for the technologies of interest for CIS [12].

In some cases, even the silicon area can be missing, for instance, if the evaluation must be done without physical access to the component. In this case, the proxy can be used thanks to the available resolution and pixel size. Those parameters are more commonly available than the die area. Multiplying the pixel area (Pix_W , Pix_H) by the resolution (Res_X , Res_Y) gives a very close approximation to the sensitive surface. However, it is important to notice that the sensitive surface does not cover the whole die. The resulting GWP from the calculation will be lower than what it would have been using the actual die surface. An extra 0.3mm on each dimension may be added to account for the space and margin needed

for the external connectivity, as observed in most sensors. The resulting area approximation, noted \hat{S} , is given in the following formula (10):

$$\hat{S} = (Res_X \cdot Pix_W + 0.3 \text{ mm}) \cdot (Res_Y \cdot Pix_H + 0.3 \text{ mm}) \quad (10)$$

V. RESULTS

A. Fairphone 4

There are a few examples of Life Cycle Assessments (LCAs) that include an image sensor. A recent example is the Fairphone series, specifically the most recent Fairphone 4 LCA reported in [27]. Although detailed numbers for this analysis are not publicly available, the provided information can serve as a basis for comparison.

In the Fairphone 4 study, the "Rear cameras module" is reported to account for a total of 2.460 kg CO₂e. Both rear cameras are Sony IMX582, as stated in the device's commercial description. To apply the relevant model to the sensor, we first determine the following information:

- Silicon area: The component's datasheet is not publicly available. However, an approximation of the die surface can be obtained using the pixel size and resolution with equation (10). For a resolution of 8000×6000 and 0.8 μm pixels, and by adding 0.3 mm to each dimension, the resulting sensitive surface is approximately 34 mm².
- Technology node: Due to the lack of documentation, the fabrication process is unknown. A default technology node must be assumed. Given the component's recent release date (2018), a 65 nm process can be considered a conservative choice.
- Factory location: As Sony is the vendor, the Japanese Carbon Intensity factor of 435 g CO₂e/kWh will be used.

With this information, it is possible to apply the model 2) to the sensor. From the tables given in section IV, we can determine the constants:

- Surface $S = 34 \text{ mm}^2$
- Electric Energy $E_{sensor} = 99 \text{ W h/mm}^2$
- Carbon intensity of Japan $T_{loc} = 0.435 \text{ g/W h}$
- Ancillary impact $K_{sensor} = 16.0 \text{ g/mm}^2$

The resulting value is 2.008 kg CO₂e in GWP. As the device has two identical cameras, the total amount of embodied CO₂ in the camera sensors is estimated at 4.016 kg CO₂e. This number does not include packaging and neither the optical part of the camera. Using this model, even though some parameters were known to be undervalued, we can already see a significantly higher value than in the original LCA study (2.460 kg CO₂e).

This estimation did not take into account the wafer stacking. Recent sensors use at least 2 wafers to maximize light sensitivity while keeping the component's footprint small. If we assume the IMX582 to have a logic section below the sensitive area, we need to add the embodied carbon impact to the estimation given above. For this logic portion of the device, it is safe to assume a 45 nm technology, with the actual

design probably being in a more recent technology. This time, we apply the model with updated constants for 45 nm:

- Surface (assume same size as a sensor) $S = 34 \text{ mm}^2$
- Electric Energy (45 nm) $E_{sensor} = 121 \text{ W h/mm}^2$
- Carbon intensity of Japan $T_{loc} = 0.435 \text{ g/W h}$
- Ancillary impact $K_{sensor} = 19.2 \text{ g/mm}^2$

This gives 2.442 kg CO₂e for the logic part of the device, for a total of 4.451 kg CO₂e for the full component. Doubling this value for the two devices, the total estimated embodied carbon is 8.901 kg CO₂e. This result is substantially bigger from the value reported in the Fairphone 4 LCA by a factor of 3.6.

B. Impact of energy mix

In another example, we can apply the same model to a different component having the same silicon area but produced in a location with a different energy mix. The VD1940 [28] sensor from STMicroelectronics has a similar silicon area as the Sony IMX582. We determined this area using the same technique (10) with a resolution of 2560×1984 for a pixel size of 2.25 μm, the approximate silicon area of the sensitive part is around 29 mm². The vendor provided the real silicon surface value of 35 mm². In this case, the technology used is made public in the component documentation. The 3D stacking is described as 65 nm and 40 nm technology nodes. As 40 nm is a shrunk evolution of 45 nm process [29], we will use the same values for 40 nm as for 45 nm. The parameters used and the results are shown in Table III.

TABLE III
COMPARISON OF GWP ESTIMATION USING THE MODEL FOR EACH SENSOR

Model Vendor	IMX582 SONY	VD1940 STMicroelectronics
Surface (mm ²)	34	35
Sensor Technology node (nm)	65	65
Logic Technology node (nm)	45	40
Sensor Electric Energy (W h/mm ²)	99	99
Logic Electric Energy (W h/mm ²)	121	121
Factory location	Japan	France
Electric Intensity (g/W h)	0.435	0.085
Sensor ancillary impact (g)	16.0	16.0
Logic ancillary impact (g)	19.2	19.2
Total GWP per sensor (g)	4451	1886

The two sensors compared here share common parameters: the sensors use 3D stacked technology with similar surfaces. The technology node used for the sensitive die and the logic one is similar. The main difference is the location of the factory, and consequently, the electric intensity. The result shows the strong impact of the energy mix when producing silicon devices.

C. Model comparison

Selecting the relevant model depends on the available information. Figure 6 illustrates the difference in the values

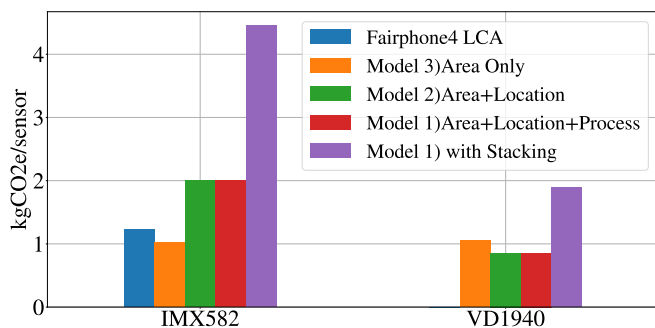


Fig. 6. Comparison of GWP estimations using the proposed models for IMX582 and VD1940 sensors. The result from the Fairphone 4 LCA is provided as a reference for the IMX582 sensor.

resulting from the application of our models to both Sony and ST sensors.

A reference value of 1.230 kg CO₂e per CIS from the Fairphone 4 LCA is shown in blue. When the simplest area model is applied (shown in orange), resulting estimations are similar with 1.020 kg CO₂e (−17% compared to the reference LCA) and 1.050 kg CO₂e for IMX582 and VD1940 respectively. The difference becomes significant when fabrication location is considered: due to the large difference in the carbon intensity between Japan and France, applying the Area+Location model yields opposite trends with 2.008 kg CO₂e (+63% compared to reference LCA) and 0.854 kg CO₂e for IMX582 and VD1940 respectively. As the default 65 nm process is actually used in the fabrication of these devices, there is no change when switching to the Area+Location+Process model. Finally, the most significant change occurs when the two layers of silicon are considered. This effect more than doubles the results of the previous model, with 4.450 kg CO₂e (+262% compared to reference LCA) for IMX582 and 1.886 kg CO₂e for VD1940.

This comparison demonstrates the importance of considering 3D die stacking over the carbon footprint of devices. In this example, the logic section is made using a more carbon-intensive technology (40 nm) than the sensitive surface (65 nm). As a result, when 3D stacking is taken into account, it more than doubles the GWP of the devices.

D. Model sensitivity

All models proposed in our study rely on a proportional relationship with the silicon area. Consequently, obtaining an accurate evaluation of the die area is a crucial factor in determining the GWP of a CIS. Apart from area, the Area+Location+Process model depends on two variables that need to be obtained or estimated. A sensitivity analysis has been conducted on these two parameters in order to determine their relative impact on the GWP estimation. Figure 7 shows the relative variation of GWP estimation in comparison to a reference point set using the parameters used for IMX582 (65 nm technology, factory located in Japan). The parameters were varied exhaustively to sweep all the combinations of values given in Tables II and I.

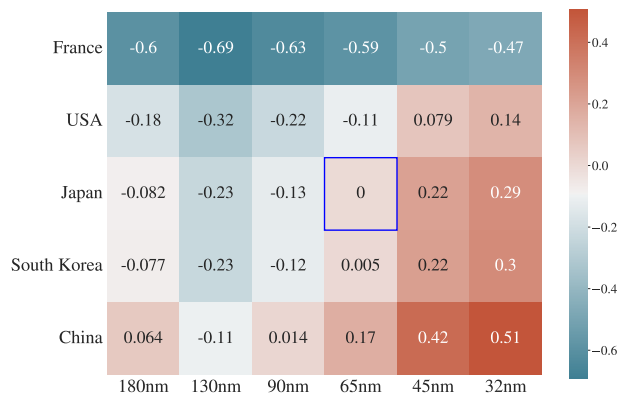


Fig. 7. Sensitivity analysis of the model 3) with regard of factory location and technology node. The data is expressed as a relative deviation from the reference point (65 nm, Japan) that was used to estimate the GWP of IMX582.

This analysis shows a strong dependence of the GWP on factory location. Changing the location of the factory to use a different energy mix can decrease GWP by 59% or increase it by 17%.

The technology node has a lesser impact, with a variation in the range of −23% up to +29% with the most significant impact for the technologies below 65 nm (45 nm and 32 nm). These technologies are uncommon for the sensitive part of CIS but may be used for the logic portion in a 3D stacked device.

These results highlight the importance of electric energy consumption when estimating the carbon impact of the fabrication of CIS. Consequently, it is essential to get a proper estimation of the factory location, otherwise, the estimation may differ significantly with an error that can reach 59% in this example.

VI. CONCLUSION

Through the use of streamlined models, we propose a methodology to approximate the carbon impact of the fabrication process for CMOS sensors. This methodology is subject to numerous uncertainties and approximations inherent in both the model itself and the selection of parameters. The high variability observed across different studies demonstrates that achieving a precise assessment is challenging.

Our study suggests that the carbon impact of CIS is currently underestimated. The increasing number of cameras and their growing complexity have rapidly shifted the significance of smartphone cameras to the level of SoC or memory.

The rise of wafer stacking technology complicates these estimations. Life Cycle Analysis (LCA) ignoring this parameter may significantly underestimate the carbon impact (and other impacts) by assuming that silicon devices are made using a single layer of silicon wafer. As 3D technologies become increasingly commonplace, the multi-layer aspect of CIS must be considered to accurately reflect environmental impact.

This study underscores the need for more readily available data. While publicly available models exist, like the IMEC database, assessments could be made with greater precision if manufacturers were to provide more data.

Other types of silicon technologies could benefit from the simplification offered by this type of study. For instance, DRAM and Flash memories, which share common characteristics as those also utilize wafer stacking, and the location of factories can be identified by the vendor. The compilation of an open, common database with unified information and models would significantly improve the assessment of the carbon impact of electronics, and broaden the application of LCA practices for electronic equipment to a wider audience.

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