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► To cite this version:

Toru Tsuboyama, Maximilian Babeluk, Marlon Barbero, Pierre Barrillon, Jerome Baudot, et al.. The Vertex Detector Upgrade of the Belle II Experiment. 31st International Workshop on Vertex Detectors, Oct 2022, Chiba, Japan. pp.011013, 10.7566/JPSCP.42.011013 . hal-04631585

HAL Id: hal-04631585

<https://hal.science/hal-04631585>

Submitted on 8 Jul 2024

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The Vertex Detector Upgrade of the Belle II Experiment

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(*) Supported by JSPS KAKENHI 20H01922, 19H00692 and 21K18633. (**) Supported by Grant RYC2020-029875-I funded by MCIN/Agencia Estatal de Investigación (Spain) and has received funding from European Union's Horizon 2020 Research and Innovation programme under grant agreement no. 101004761 (AIDAInnova) and NextGenerationEU/PRTR.

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(Received February 28, 2023)

The SuperKEKB accelerator and Belle II experiment have started full operation in 2019, establishing in 2022 a world record with an instantaneous luminosity of $4.7 \times 10^{34}/\text{cm}^2/\text{s}$. To reach the nominal luminosity parts of SuperKEKB will be modified with a time frame currently predicted to be around Long Shutdown 2 in 2026. Thus, the Belle II collaboration is considering the possibility to install an upgraded vertex detector (VXD) system on the same time scale. Such an upgrade should provide a sufficient safety factor with respect to the background rate expected at the nominal luminosity ($6.5 \times 10^{35}/\text{cm}^2/\text{s}$) and possibly enhance performances for tracking and vertexing.

Several technologies are under consideration for the upgrade. One approach is to improve the performance of the technologies present in Belle II: faster DEPFET sensors [1] for the innermost layers, thinner and more granular double-sided silicon strip detectors (DSSDs) for the remaining layers. New monolithic technologies for pixel sensors are also under discussion, namely SOI (Silicon-on-sensor) and CMOS. They offer a combination of granularity, speed, low material budget and radiation tolerance matching well Belle II requirements and could be exploited to design a fully pixelated VXD, also benefiting from significant developments made in recent years for other experiments. Following this last concept, both simplified and complete simulations have been conducted to evaluate tracking and vertexing performance with various geometries (e.g. number of layers) and technical specifications (e.g. granularity, speed).

This article reviews the context of the proposed VXD upgrade in Belle II, providing some details of the existing technological proposals and discussing performance expectations from simulations.

KEYWORDS: Super KEKB, vertex detector, luminosity, radiation tolerance, physics performance

1. Introduction

Super KEKB is an asymmetric energy e^+e^- collider at the $\Upsilon(4S)$ energy [2]. Belle II aims to study, primarily, the B meson decays in high statistics [3]. As the B mesons move along the beam direction (z), the time dependence of the B decay can be measured by using the vertex detector (VXD). Therefore, the position resolution in z is equally important as in the transverse direction ($r - \phi$). The current Belle-II VXD, as shown in Fig. 1, consists of two-layer DEPFET pixel detectors (PXD) [4] and four-layer double sided strip sensors (SVD) [5]. The Belle II VXD covers the angular acceptance of $17^\circ < \theta < 150^\circ$.

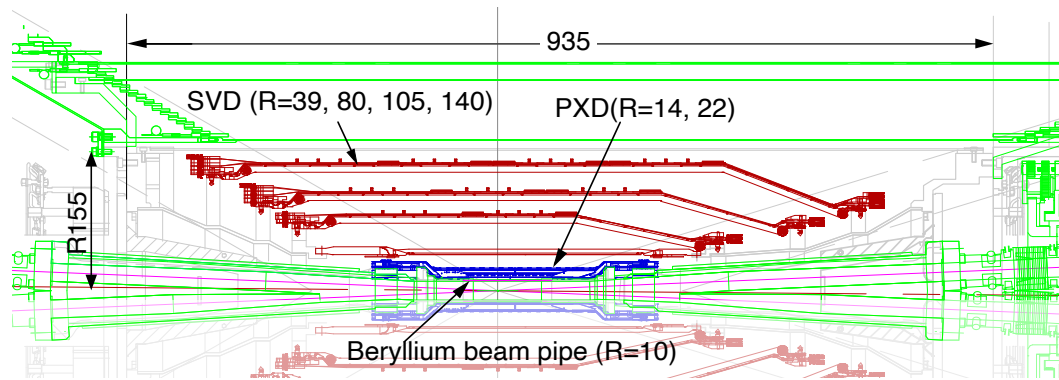


Fig. 1. The schematic cross section of the Belle II interaction region. (unit= mm). The electron and positron beams collide at the center of Beryllium beam pipe. The vertex detector consists of two DEPFET (PXD) layers and four Silicon strip detector layers (SVD). support of SVD ladders.

Table I. The layer structure of the Belle II vertex detector, the material thickness of pixel and strip layers includes the material for support

Layer	Component	Material	Radius (mm)	Thickness (mm)	Material thickness of the layer (% X_0)
	Gold plating	Au	10	0.01	0.3
	Beam pipe	Be	10	1.0	0.3
1	Pixel	Si	14	0.075	0.2
2	Pixel	Si	22	0.075	0.2
3	Strip	Si	39	0.32	0.7
4	Strip	Si	80	0.32	0.7
5	Strip	Si	105	0.32	0.7
6	Strip	Si	140	0.32	0.7

The PXD and SVD have been working successfully since 2019. The performance of the present VXD is described in the proceeding papers of this conference [6, 7].

In 2022, the peak luminosity of the Super KEKB reached to $4.7 \times 10^{34}/\text{cm}^2/\text{s}$ at beam current of 1 A (e^+) and 1 A (e^-) and Belle II has accumulated data corresponding to an integrated luminosity of 428 fb^{-1} .

To achieve the luminosity goal of $6.5 \times 10^{35}/\text{cm}^2/\text{s}$, the Super KEKB will be upgraded in two steps. In July 2022, Super KEKB entered the Long Shutdown 1 (LS1) period. The main purpose

Table II. Background level at the innermost layer of VXD assumed for the VXD upgrade.

Background hit rate	113 M hits/cm ² /s
TID Level	100 kGy/year
NIEL Fluence	5×10^{13} n _{eq} /cm ² /year

of LS1 is to replace the DEPFET pixel detector [1] with the complete two layer system. The Long Shutdown 2 (LS2) is scheduled in 2026. In LS2, the Super KEKB accelerator will be reinforced to reach to the luminosity goal and collect data corresponding to 50 ab⁻¹, as shown in Fig. 2.

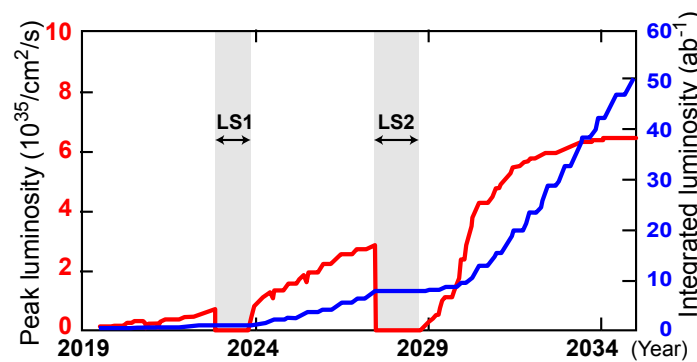


Fig. 2. Prospect of the Luminosity improvements of Super KEKB. The red line shows the peak luminosity in unit of 10³⁵/cm²/s. The zero luminosity periods for the short shutdown are not shown. The blue line shows the integrated luminosity in unit of ab⁻¹. LS1 and LS2 indicate the long shutdown periods scheduled from 2022-2023 and 2027-2029.

The Belle II VXD will be upgraded in LS2 in order to improve the background immunity and physics performance. To start the design of the VXD upgrade, the beam background from the Super KEKB was estimated. Table II shows the background level at the innermost layer of the VXD at the luminosity of 6.5×10^{35} /cm²/s with a $\times 5$ safety factor [8]. The upgraded sensors should be safely operated at the harsh radiation condition. The optimization of the material budget and position resolution is also needed to improve the physics performance of Belle II.

In this article, the following upgrade activities [8] will be described: (a) DMAPS (fully-Depleted Monolithic Active Pixel Sensor), (b) SOIPIX (Silicon on Insulator Pixel sensor), and (c) TFP (Thin Fine-Pitch silicon strip sensor).

2. DMAPS - Depleted CMOS Active Sensor

The DMAPS (Depleted MAPS) technology is an improvement of the CMOS Active Sensor. The CMOS circuit is developed in the deep p-well region above the *p*-type epitaxial layer as shown in Fig. 3. A full CMOS circuit can be integrated in the deep p-well region. The sensitive region is fully depleted with the bias voltage. The small charge collection node makes the charge collection fast and efficient. The DMAPS technology is radiation hard enough for the upgrade plan.

2.1 TJ-MONOPIX2 pixel sensor

TJ-MONOPIX2 was originally developed for ATLAS and has been identified as a good candidate for the Belle II VTX upgrade. The specifications of MONOPIX2 are shown in Table III. The chip includes fast-shaping front end and time-over-threshold circuit for the cluster charge measurement.

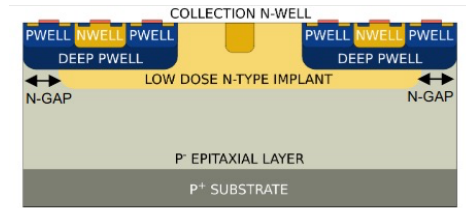


Fig. 3. DMAPS structure. The wafer is P^- type high resistivity silicon. The CMOS circuit is integrated in the deep p-well. The charge is collected by the collection N-well. The P^- or epitaxial region can be depleted by the detector bias. The low dose N -implant region and N gap forms the electric field for fast and efficient charge collection.

The MONOPIX2 chips were installed to a pixel telescope and the detection efficiency and position resolution were measured at the DESY 5 GeV e^- beam. Fig. 4(a) shows that the detection efficiency was $> 99\%$ independent of the wafer type. The residual distribution of the cluster position (Fig. 4(b)) was consistent with $(\text{pixel size})/\sqrt{12}$. The details of the MONOPIX evaluation are described in [9].

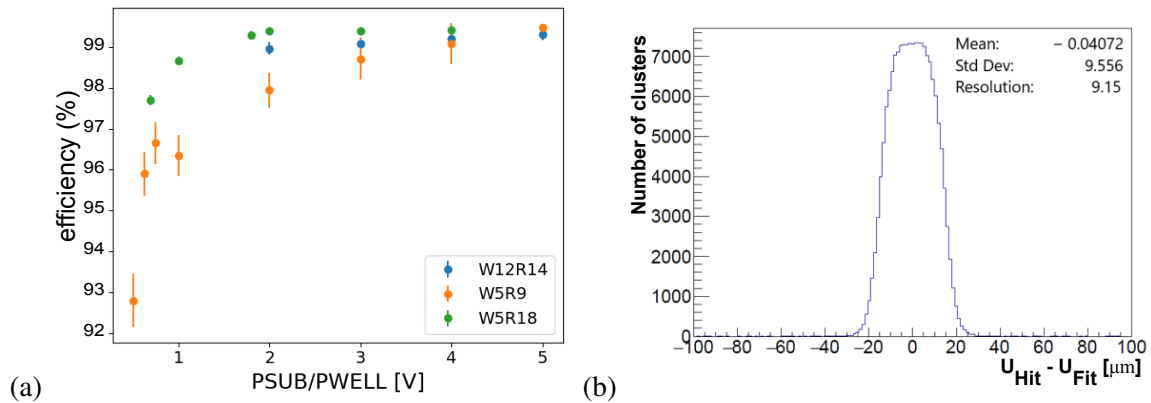


Fig. 4. Test beam result of TJ MONOPIX2 sensor. (a) Detection efficiency vs the bias voltage for different wafer types. W12R14, W5R9 and W5R18 corresponds to Cz-bulk, epi $30\ \mu\text{m}$ and epi $30\ \mu\text{m}$, respectively. (b) Spatial resolution for perpendicular incident tracks. Horizontal axis shows the residual of position measured by the DUT (device under test) and the telescope.

Table III. The main characteristics of TJ-MONOPIX2

Technology	Tower Jazz $0.18\ \mu\text{m}$ CMOS
Chip size	$20\ \text{mm} \times 20\ \text{mm}$
Active area	$17\ \text{mm} \times 17\ \text{mm}$
Pixel pitch	$33\ \mu\text{m} \times 33\ \mu\text{m}$
Substrate	Epi ($\sim 1\ \text{k}\Omega\text{-cm}$) / Cz ($> 1\ \text{k}\Omega\text{-cm}$)

2.2 OBELIX pixel sensor

Following the TJ-MONOPIX2, the first chip implementing the specific needs of Belle II is designed, OBELIX (Optimized BELLe II pIXel) [10] pixel sensor as shown in Table IV is in progress. The chip will include the necessary functions for the Belle II operation environment: the fast-shaping front end, charge digitization with ToT circuit, trigger-hit matching and zero suppression logic. The OR of the pixel signal will be produced for the fast hit information to the Belle II trigger. The first prototype of the OBELIX sensor will be submitted in 2023.

Based on the OBELIX sensor, the mechanical design of the vertex detector (VTX) system is in progress. In VTX, not only the pixel layers but also the strip layers of the current Belle II VXD will be replaced with the pixel layers. VTX will consist of two inner layers (iVTX, $R=14$ mm and 22 mm) and three outer layers (oVTX, $R=39$ mm, 90 mm and 140 mm). To simplify the system, the whole VTX will be built with a single sensor design. For the iVTX four consecutive chips on a wafer are cut out as one self-supporting module. The interconnections between the chips and the readout electronics will be realized as a high density interconnect layer. Air cooling will be possible thanks to the small power consumption (200 mW/cm²). In the oVTX modules, the OBELIX sensors will be assembled with truss-shape carbon fibre support. Water cooling with polyimide tubes has been tested successfully. The total material thickness will be kept below 2 % radiation length (X_0) to improve the physics performance, whereas the material thickness of the current Belle II VXD is 0.4 % X_0 (PXD) and 2.8 % X_0 (SVD) [11].

Table IV. The main characteristics of OBELIX pixel sensor

Technology	Tower Jazz 0.18 μ m CMOS
Chip size	32.2 mm \times 18.3 mm
Active area	31.6 mm \times 18.1 mm
Pixel size	33 μ m \times 33 μ m

2.3 Expected physics performance

The physics performance of Belle II after the VTX installation is estimated by using the Monte-Carlo simulation. The effect of the increased beam background for the nominal luminosity is taken into account. Figs. 5 (a) and (b) shows the comparison of the reconstruction efficiency of soft pions (π_s) from D^* meson decay. Thanks to the small material thickness and the high spatial resolution, the reconstruction efficiency of the π_s will improve by 50-80 %. The efficiency improvement will result in higher sensitivity to the new physics phenomena.

3. SOI - Silicon on Insulator

The SOI is a standard technology for producing high-performance CMOS circuit. The SOI wafer consists of the substrate silicon and the silicon layer for the CMOS circuit separated by a thin SiO₂ layer (Buried oxide or BOX), Figure 6. In the SOI sensor, a sensor grade wafer is used. With impurity injection, a complex sensor structure can be designed in the substrate. The charge generated by the radiation is processed in the circuit layer.

Fig. 6 shows the structure of PDD (Pinned Depleted Diode). The impurity structure is designed so that the charge carrier induced by radiation drifts to the collector node smoothly, therefore, the efficient and fast charge collection is realized. The BPW (Buried P-well) region is set to a fixed voltage, V_{BPW} which prevents the substrate potential affecting the operation of the CMOS circuit above the BOX layer. Thanks to the small collection node, the sensor capacitance is as small as 3 fF. The DuTiP, Dual Timer Pixel sensor, concept is designed for the Belle II upgrade. using Lapis 0.2 μ m

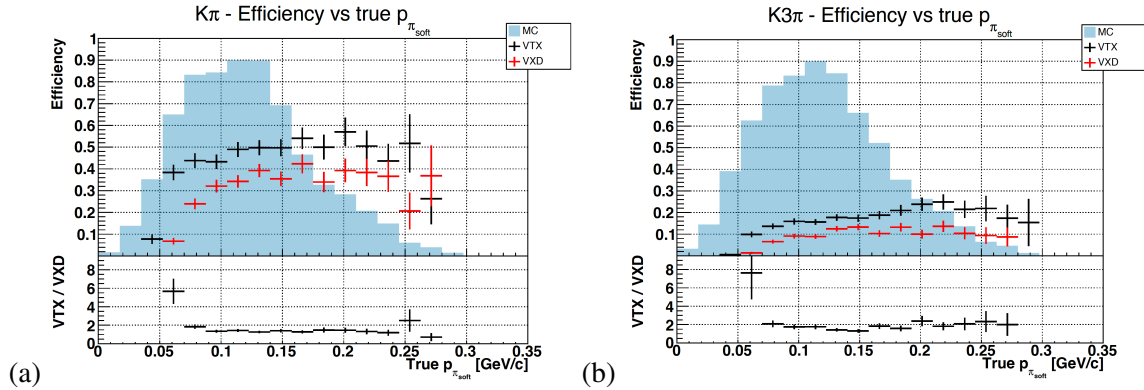


Fig. 5. Reconstruction efficiency of soft pions in (a) $B \rightarrow D^* \mu \nu, D^* \rightarrow \pi_s K \pi$ and (b) $B \rightarrow D^* \mu \nu, D^* \rightarrow \pi_s K \pi \pi$. Red points show the Belle II VXD and black points, the VTX detector concept. The reconstruction efficiency improves by 50-80 %. Lower limit of π_s reconstruction is extended from 75 MeV/c to 50 MeV/c.

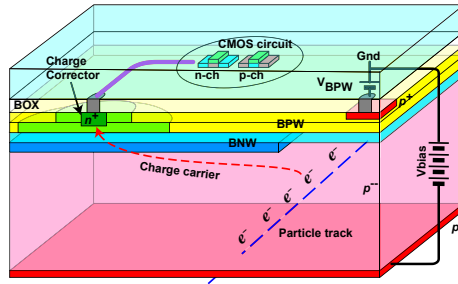


Fig. 6. A typical SOI pixel sensor with PDD (Pinned Depleted Diode) substrate structure. The wafer is high-resistivity p^- type. The p -type and n -type impurities are implanted to form the electric field fast and efficient. The CMOS circuit is integrated on the buried oxide (BOX) layer.

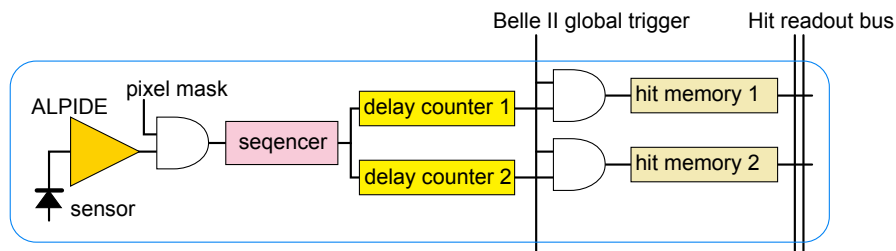


Fig. 7. The pixel circuit of the DuTiP. The hit charge in the wafer is picked up by the sensor node and processed by the ALPIDE amplifier. The delay counter-1 and -2 are used to delay the hit signal for the trigger decision time of Belle II global trigger. If the delayed hit signal coincides with the Belle II trigger, the hit will be read out through the hit-readout bus and sent to the Belle II data acquisition system.

SOI pixel sensor technology. The pixel circuit is shown in Fig. 7 [12]. The ALPIDE-type front end [13] is adopted for low power consumption. The hit signal is delayed with the delay counter (timer) and the coincidence with the Belle II global trigger is taken. The coincidence reduces the background hit occupancy efficiently. Two timer are integrated in each pixel to secure hits arriving within the trigger decision time. The hit information is sent first to the column FIFO and then to the global FIFO for the readout. The trigger ID is added to each hit inside the chip. Simulation study shows the hit

Table V. The specifications of the DuTiP pixel sensor

Wafer	High resistivity p-type FZ silicon(6-8 kΩcm)
Buried oxide (BOX)	140 nm SiO ₂
Silicon	20 nm low resistivity
Sensor structure	Pinned Depleted Diode
Chip size	17.2 mm × 29.6 mm
Pixel size	45 μm × 45 μm
Active area	14.4 mm × 28.8 mm

occupancy can be reduced $< 0.1\%$ under the 113 MHz/cm² background hit condition. Efficiency data transfer is expected with the two stage FIFO [12]. Two prototypes have been produced as shown in Table VI. DuTiP1 (2021) was designed to study the DuTiP pixel circuit, especially, the performance of the two-timer concept. DuTiP2 (2022) is a full size sensor in the column direction and intended to study the readout sequence for the DuTiP. Both chips are under evaluation.

Table VI. The specifications of the DuTiP pixel sensor

	DuTiP1	DuTiP2
Chip size	6 mm × 6 mm	6 mm × 18.4 mm
Pixel size	45 μm × 45 μm	45 μm × 45 μm
Pixel array	64 × 64	64 × 320

4. TFP - Thin Fine Pitch double sided detector

The silicon strip sensor is a suitable for covering a large area in the outer layers. Double-sided silicon strip detectors (DSSDs) with a thickness of $\approx 300\ \mu\text{m}$ were used in outer four layers of the Belle II VXD (Table I). In the forward region $17^\circ < \theta < 45^\circ$, the crossing angle of the charge tracks to the sensor layers becomes large. The cluster shapes are elongated and the position resolution in z rapidly degrades. The sensors in the forward region are therefore slanted (Fig. 1) to recover the position resolution. The TFP (thin fine-pitch) DSSD group proposed to replace the existing SVD with new double-sided strip sensors made from 150-μm thick silicon wafer [14]. To reduce the hit occupancy and to improve the spatial resolution especially in z , the readout pitch is reduced from 240 μm to 75 μm (z -measurement) and 75 μm to 50 μm ($r - \phi$ -measurement).

A dedicated readout ASIC, SNAP128A, has been produced with the Silterra 180 nm CMOS technology [14]. SNAP128A was designed to be operated in the expected high background environment of the target luminosity. The front end is a charge sensitive amplifier with a shaping time of 100 ns optimized for the 150-μm thick DSSD sensor. The signal polarity inverter is implemented for the p -side and n -side readout. After the comparator, the hit signal is delayed by a 2 kbit digital pipeline. When a trigger is received, the data one or more cells of the digital pipeline are read out. The hit information is sent to the LVDS driver. For the trigger purposes, the SNAP128A will provide a hit-OR signal to the Belle II trigger system. The TFP hit signal is useful for generating the fast track information.

A prototype TFP sensor with a size of 59 mm × 52.6 mm was fabricated by Micron (UK). The test result will be reported in this proceedings [14]. The TFP sensor and the SNAP128A chip have been irradiated with an electron beam to measure the TID and NIEL radiation hardness. The analysis is in progress.

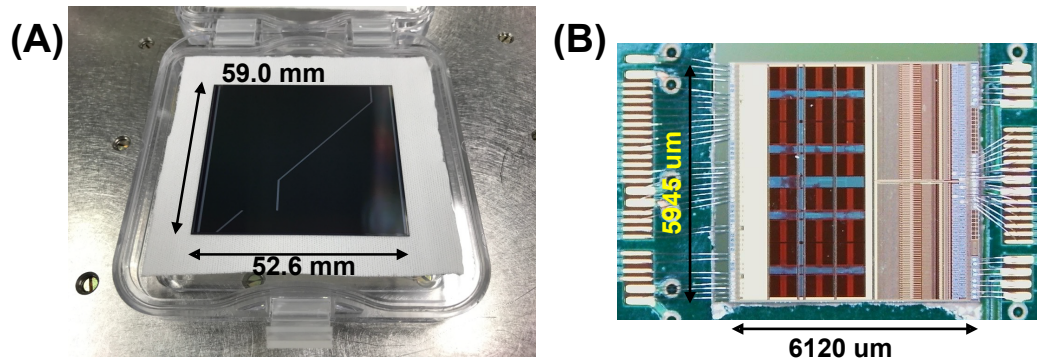


Fig. 8. (A) A prototype TFP DSSD: The wafer thickness is $150 \text{ }\mu\text{m}$. Strip pitch on p-side and n-side is $50\text{-}\mu\text{m}$ and $75\text{-}\mu\text{m}$. (B) The SNAP128A chip on the test PCB.

The concept of the module structure is shown in Fig. 9. An aluminum flex layer (Al $15 \text{ }\mu\text{m}$) will be introduced for the power rails. Although each sensor is read out by 14 SNAP128A chips, the generated heat can be removed by the water cooling at 5°C , whereas the coolant is circulated in thin stainless steel tubes.

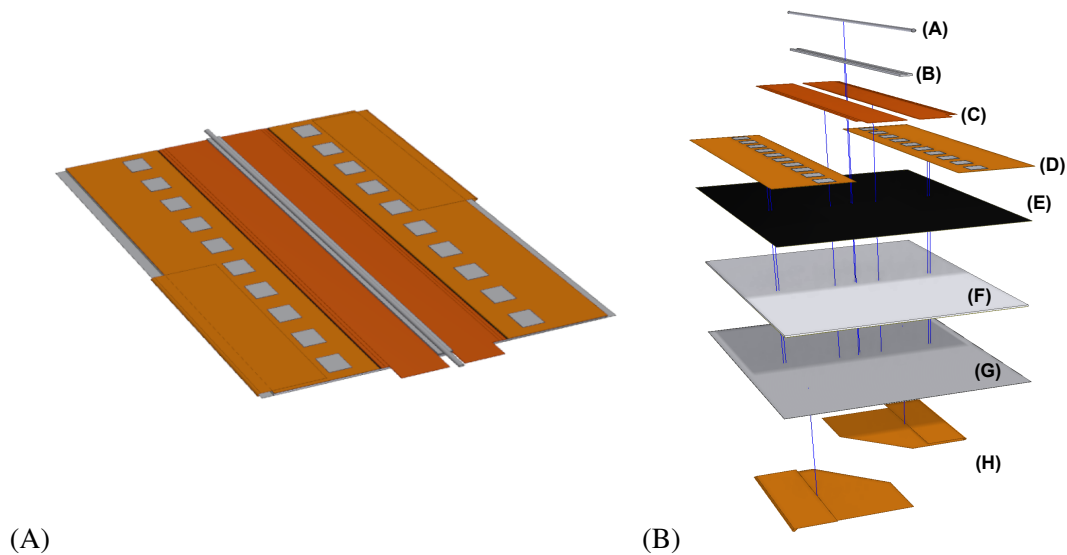


Fig. 9. The breakdown of the TFP module structure: (A) the stainless cooling tube, (B) thermal conductive film, (C) aluminum flex for the powering, (D) ASIC flex for signal transfer, (E) graphite heat spreader, (F) thermal insulator, (G) TFP DSSD sensor, (H) Fanout for the bottom-side signal

5. Summary

The upgrade activity of the Belle II vertex detector (VXD) has been presented. The progress of DMAP, DuTiP and TFP is remarkable. Recently, a new discussion of replacing several inner-wire

layers of the Central Drift Chamber (CDC) with TFP detector layers has started, because the CDC wire efficiency would be degraded by the high backgrounds at the luminosity goal after the LS2 upgrade. Summarizing the progress of R&D, the preparation of the Conceptual Design Report for LS2 upgrade is in preparation.

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