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# High temperature evolution of a confined silicon layer

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## ABSTRACT

The temperature-induced phase and morphology changes of a thin layer sandwiched between two substrates which it partially wets are investigated using transmission electron microscopy, scanning electron microscopy, and x-ray scattering techniques. For this, SiC wafers were bonded with Si layers of various thicknesses and annealed at temperatures below and above the Si melting point. Below the melting point of Si, solid-state dewetting occurs. It starts with the heterogeneous nucleation of pits at the Si/SiC interfaces and progresses to their partial transformation into voids crossing the whole film. The further growth of voids is accompanied with an increase in the Si film thickness. Final equilibrium is shown to be impacted by Si crystallographic state evolution. Above the Si melting temperature, liquid Si drives SiC interfaces step bunching. When high steps and large terraces are formed over the two SiC surfaces, Si is shown to be trapped within quasi-closed pockets. Eventually, the interface locally closes around these Si inclusions with the creation of SiC/SiC direct contacts. The influence of both annealing temperatures and Si film thickness on all these processes is discussed.

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## I. INTRODUCTION

Silicon carbide is a widely used material for power electronics thanks to its wide bandgap and high thermal conductivity.<sup>1,2</sup> Stacking of thin SiC layers of a different quality or doping level through wafer bonding is of particular interest for applications in electronics devices.<sup>3–5</sup> As direct SiC/SiC bonding may prove difficult, a layer of intermediate material playing a role of glue can be used to ensure a good binding between the two SiC substrates. The high temperature needed for power device fabrication requires studying the evolution of such bonding layers under high temperatures.

Although SiC/SiC bonding with a SiO<sub>2</sub> layer has been demonstrated and well-studied in the literature,<sup>6</sup> it is incompatible with applications-specific requirement for a conductive interface between the stacked substrates. Bonding with metallic layers is also conceivable, but it is fraught with contamination issues.<sup>7,8</sup> Silicon can be considered as a valuable alternative to all these materials thanks to its semi-conductor behavior and its general use in the microelectronics industry. In this work, we addressed such a possibility.

We studied the structure evolution of a few nanometer-thick amorphous Si layer sandwiched between two monocrystalline SiC substrates subjected to annealing at high temperatures below and above the Si melting point. We focused our attention on understanding the impact of as-bonded Si layer thickness and isothermal or isochronal thermal annealing on the Si layer and the Si/SiC interface morphologies.

In the first part of the article, we address the changes in the morphology of the Si films after annealing at a relatively low temperature aimed at crystallization of initially amorphous layers. The effect of a second additional isochronal or isothermal annealing at higher temperatures not exceeding the Si melting point,  $T_{mp}$  is presented in the second part of the paper. The third one describes the reconstruction of the SiC/Si interfaces under silicon liquefaction induced by annealing at temperatures exceeding  $T_{mp}$ . Then, we discuss the essential results and propose a consistent scenario for the system evolution.

## II. EXPERIMENTS

Bonded structures are prepared using atomic diffusion bonding (ADB) technique applied at room temperature. This

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process consists generally in the deposition of thin films by sputtering on the two wafers followed by a direct vacuum bonding of the two capped substrates. This bonding process was developed by Shimatsu and Uomoto.<sup>9–12</sup>

For Si deposition, we used two (0001) 4H-SiC single crystal wafers with different C- and Si-termination of their surfaces. The wafers present a 4° offcut obtained by a (0001) plane rotation around the in-plane [1100] direction. The C-face SiC substrate was implanted with H<sup>+</sup> ions to a depth of 800 nm. Amorphous Si films were deposited to a thickness of 4, 10, and 20 nm on both substrates. While preserving coaxial orientation of crystallographic directions in both wafers, the substrates were bonded at room temperature bringing the two Si surfaces in contact under vacuum. The resulting thickness of the sandwiched Si film is, thus, doubled. Note that the eventual Si layer is in contact with Si-face and C-face SiC surfaces from different sides resulting in two distinct interfaces.

After bonding, the SmartCut™ process was applied resulting in a transfer of a 800 nm-thick C-face SiC layer on the Si-face substrate. During this first procedure, the sandwiched structure received a thermal budget equivalent to typically 900–1000 °C. Then, the SiC/Si/SiC substrates were cut into pieces and isochronally or isothermally annealed for a second time at different temperatures ranging from 1100 to 1700 °C and annealing time varying from 4 min to 4 h.

The evolution of the bonding interface is then analyzed as a function of annealing temperature, annealing time, and the Si film thickness.

Scanning electron microscopy (SEM) was used to visualize the morphology of one of the Si layer surfaces. For this, the transferred C-face SiC layer was removed by cleavage. The images were obtained detecting secondary electrons, which provides a direct and large-scale top-view imaging of the Si layer surface. ImageJ software<sup>13</sup> was used for the analysis of the SEM images.

Atomic force microscopy (AFM) surface imaging of the pristine C-face and Si-face substrates was performed for surface roughness estimation. AFM scans were also performed on the Si layer surface to study its topography, once the top layer has been removed by cleavage.

Cross-sectional transmission electron microscopy (TEM) technique was applied to identify the structure and morphology of the interfaces and to determine the crystalline phases and their orientation. The images were obtained in the SACTEM-Toulouse (Tecnai-FEI) and Jeol2010 microscopes operating at 200 kV. FEI Helios Nanolab 600i focused ion beam (FIB) was used to prepare less than 70 nm-thick lamellas using a standard lift-out procedure followed by milling with 30 kV Ga ions and cleanup procedure at 2 kV.

X-ray diffraction (XRD) measurements were carried out at the BM32 beamline of the European Synchrotron Radiation Facility (Grenoble, FRANCE) providing insight on the crystalline texture and strain in silicon and SiC layers. X-ray reflectivity (XRR) was used for the measurement of the Si layers thickness.

### III. RESULTS

#### A. First anneal

After sputtering deposition and bonding procedure at room temperature, the silicon films were found amorphous.<sup>14</sup>

After the SmartCut™ procedure involving a first anneal at 900–1000 °C, the silicon films became polycrystalline. Top-view SEM images acquired after cleaving out the transferred layers reveal the presence of pits in the structures of different Si film thicknesses [Fig. 1(a)].

TEM images [see insert in Fig. 1(a)] reveal a similar depth of 5–10 nm for all the pits. Thus, except for a 8 nm-thick Si film, no pit is able to cross the whole Si film. A few pits with a lateral size of 50 nm are observed in the 20 nm-thick Si layer. However, for all the samples, we found that the overwhelming majority of pits have a similar average lateral size of  $20 \pm 5$  nm and a density of  $60 \mu\text{m}^{-2}$ . Pit density is independent of the Si film thickness and their nucleation might depend on some particular properties of the C-face and Si-face SiC/Si interfaces, like, for example, their roughness.

Prior to Si deposition, we measured using AFM the roughness of C- and Si-terminated surfaces of the SiC wafers. The RMS roughness is found to be around 2–3 Å for the C-face against less than 1 Å for the Si-face. To verify whether the higher roughness of one face with respect to the other one is responsible for the preferential nucleation of pits, the Si-terminated SiC substrate was subjected to mechanical grinding prior to Si deposition. The sandwiched structure with a 20 nm-thick Si film was then annealed as for the previous samples.

Figure 1(b) (left) shows the top-view SEM image obtained after cleaving out of the C-terminated substrate in such a sample. Two classes of objects are observed. The first class consists of the randomly distributed shallow pits nucleated from the C-face SiC surface, which have the average size and density similar to that observed in the previous example. The second class of objects consists of much deeper and larger pits (voids) well aligned along the grinding lines. The voids have a lateral size of about 200 nm, a density of  $10 \mu\text{m}^{-2}$ , and a line density of  $4 \mu\text{m}^{-1}$ . Cross-sectional TEM images show that these voids cross the entire Si layer [Fig. 1(b), right].

In this case, the voids were nucleated from the scratches added to the Si-face of the bottom substrate. Thus, Si/SiC interface defects promote formation of pits that could eventually lead to Si film piercing.

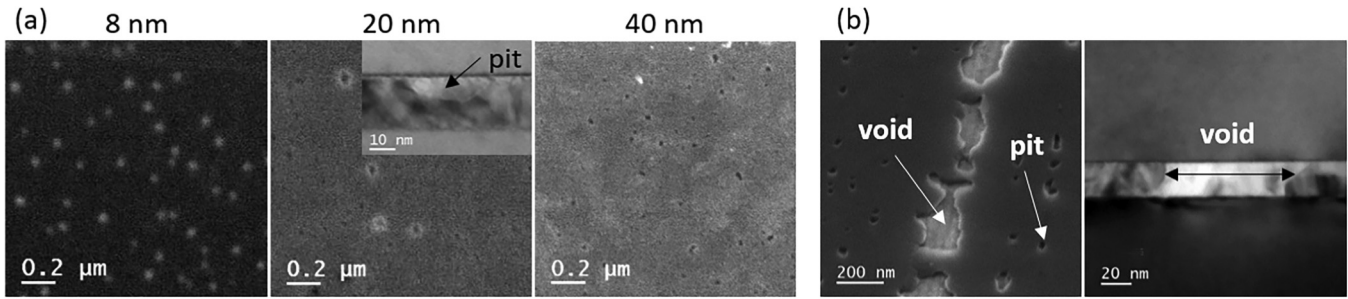
#### B. Second isochronal anneal at $T < T_{\text{mp}}$ for 30 min

In this part, we study Si film morphology evolution under subsequent second isochronal annealing at different temperatures for 30 min.

Figure 2(a) shows the top-view SEM images of the corresponding structures arranged as a function of the Si film thickness (lines) and annealing temperature (columns).

The sample with a 8 nm-thick Si layer does not contain any pit after annealing at all the temperatures. Instead, quasi-cylindrical faceted voids, piercing the Si film, are formed. The sample with a 20 nm-thick Si layer contains both pits and voids after annealing at 1100 °C and only voids after annealing at higher temperatures. The sample with a 40 nm-thick Si layer contains only pits, both pits and voids, and, finally, only voids after annealing at 1100, 1300, and 1400 °C, respectively.

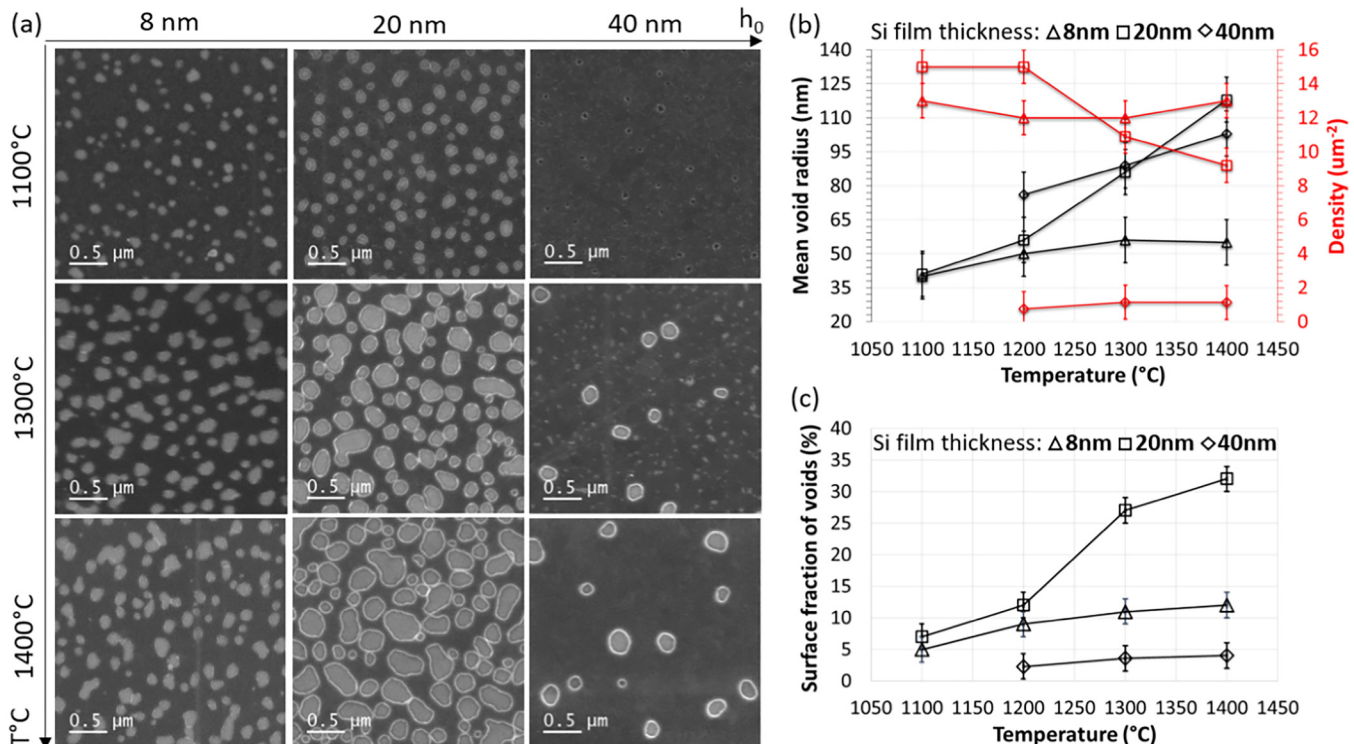
The voids formed in all the samples after annealing at 1100 °C remain well isolated one from another. They obey a quasi-circular



**FIG. 1.** Defects formed in the Si films of different thicknesses after the first anneal at 900 °C–1000 °C: (a) SEM images of pits formed in the Si layers at the Si/C-face SiC interface; (b) left: 52° tilted SEM image and right: cross-sectional (1100) HRTEM image of pits formed at the Si/C-face SiC interface and voids formed from the Si-face SiC/Si interface subjected to grinding prior to bonding.

faceted base. The similar isolated objects are found in the sample with a 40 nm-thick Si layer after annealing at higher temperatures. In contrast, the samples with a 8 nm-thick and a 20 nm-thick Si layer subjected to annealing at 1300 and 1400 °C contain a fraction of the voids with an irregular shape. This suggests that they were formed as a result of coalescence events. Coalescence may explain evolutions in voids size and density. The voids formed in the

8 nm-thick layers have a quasi-constant density of  $13\mu\text{m}^{-2}$  independently of annealing temperature [Fig. 2(b), red triangles]. Such a value is about —four to five times lower than the density of pits formed after the first annealing. The absence of pits in this sample after the second annealing at 1100 °C indicates that 75%–80% of preexisting pits were healed, while 20%–25% transformed into voids. The void average radius monotonically increases with



**FIG. 2.** Defects formed in the Si films of different thicknesses after the second isochronal anneal at different temperatures for 30 min: (a) top-view SEM images; (b) average void size and density; and (c) surface fraction, measured from (a) as a function of temperature for the three thicknesses.

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temperature from 40 nm after annealing at 1100 °C to a value of 55 nm at 1300 °C which remains the same after annealing at 1400 °C [Fig. 2(b), black triangles]. The surface fraction occupied by the voids exhibits similar behavior, increasing monotonically from 5% at 1100 °C to 12% at 1300 °C before saturating with further increase in the temperature.

For the 20 nm-thick layer, the density of voids of  $15\mu\text{m}^{-2}$  is only slightly larger at 1100 and 1200 °C than that found for the thinnest Si layer, i.e., it still amounts to 1/4 of the preexisting pit density. After annealing at 1300 and 1400 °C, the void density drops to a constant value of  $10\mu\text{m}^{-2}$ . An average radius of voids increases from 40 nm at 1100 °C to 56 nm at 1200 °C, i.e., it remains similar to that found in a 8 nm-thick Si layer. A further increase in temperature results in a stepwise increase in radius up to a value of 85 nm at 1300 °C and then of 120 nm at 1400 °C, which is induced by the coalescence process. The thermal behavior of a surface fraction occupied by the voids further confirms such a finding. While it increases from 7% to 13% when the temperature increases from 1100 to 1200 °C, it changes abruptly to 27% at 1300 °C and then increases to 32% at 1400 °C.

The sample with a 40 nm-thick Si layer does contain some pits larger than most of the pits presenting in the layer after annealing at 1100 °C. However, they do not pierce the whole Si layer and, thus, cannot be considered like the voids. The voids start to appear only after annealing at 1200 °C (not shown). Once formed, their density remains constant with temperature and has a relatively low value of  $1\mu\text{m}^{-2}$ . Their size increases monotonically with temperature and remains systematically slightly lower than that found in the sample with a 20 nm-thick Si layer which is probably due to the lack of coalescence between the voids at such low density. The surface fraction of the voids linearly increases with temperature and remains below 5%.

From this part of the experiment, we learned that the pit nucleus density does not depend on the Si layer thickness and is defined by the roughness property of the C-face SiC substrate. The pits can be preserved or evolve with temperature following two competing processes like healing or transformation into voids. The effectiveness of pits healing increases with reduction of the Si layer thickness and increasing annealing temperature. Only a fraction of pits become voids. For a given Si layer thickness, the void density remains quasi-constant with temperature except for its reduction due to coalescence events. The average size of the void's base increases with temperature. For the thinnest Si layer, both the void density and size saturate when the annealing temperature increases above 1300 °C. All together, these data indicate that void growth is a thermally activated process which occurs from a non-equilibrium state of the Si layer. The formation of pits and voids only occurs in the early stages of annealing at a high enough temperature. However, their evolution with temperature stops after some time, indicating the system has reached an equilibrium state. The latter is achieved earlier for thinner Si layers. We address the morphology and phase changes in the Si layers in the next part of this work. For this, the samples were studied by cross-sectional TEM imaging, XRR, and XRD techniques.

Figure 3(a) shows the cross-sectional TEM images of the Si films formed after annealing at 1300 °C for 30 min arranged as a function of their nominal thickness (from left to the right) and

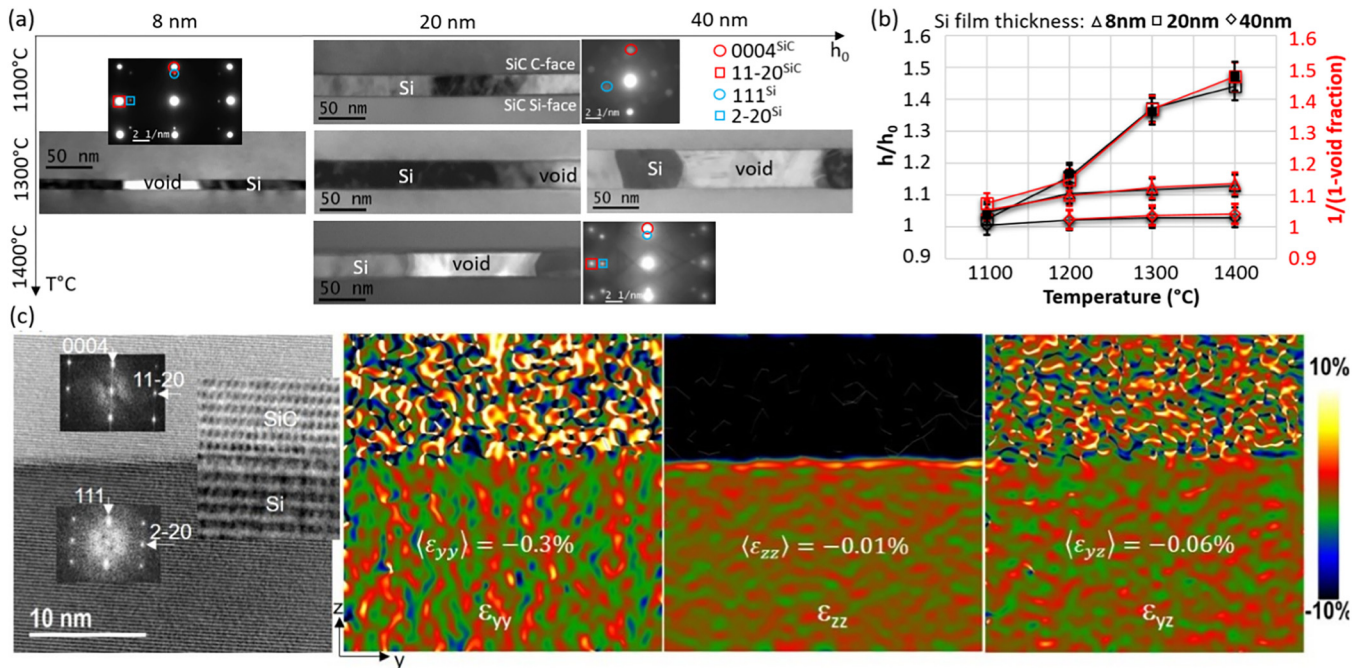
that of the film with a nominal thickness of 20 nm arranged as a function of annealing temperature of 1100 to 1400 °C (from top to the bottom). The C-face SiC/Si interface is located above the Si-face SiC/Si interface in these images.

Let us focus on the evolution of the nominally 20 nm-thick Si film with annealing temperature (middle column). Whatever the temperature, the Si film seems to be polycrystalline. However, the size of the grains increases with temperature, from several nanometers at 1100 °C to much larger values at 1300–1400 °C. The large Si grains tend to reach an epitaxial relation with the SiC wafers as seen from the diffraction patterns shown in insets.

The effect of a Si film thickness on the grain size and Si structure reorganization can be elucidated following the middle line of the images corresponding to the structures annealed at 1300 °C [Fig. 3(a)]. While the 40 nm-thick film remains randomly polycrystalline, a well pronounced increase in the lateral size of grains and epitaxial relation with the SiC substrate is reached in the nominally 8 nm-thick film: the film becomes completely monocrystalline. This is a new equilibrium state of the Si layer. According to the diffraction pattern (see the inset), the following crystallographic relationship between Si and SiC structures is satisfied:  $(111)^{\text{Si}}//(\text{0001})^{\text{SiC}}$ ,  $[1\bar{2}1]^{\text{Si}}//1\bar{1}00^{\text{SiC}}$ ,  $[10\bar{1}]^{\text{Si}}//11\bar{2}0^{\text{SiC}}$ .

Because single crystal Si films are found to be in epitaxial relation with SiC, we address the strain within such a Si structure. For this, we have used a cross-sectional  $(1\bar{1}00)^{\text{SiC}}$  high-resolution scanning transmission electron microscopy (STEM) High-Angle Annular Detector Dark-Field (HAADF) image of the structure with a 20 nm-thick Si layer annealed at 1400 °C for 30 min [Fig. 3(c), on the left]. C-face SiC and a part of the Si film are imaged over the upper and bottom parts of the field of view, respectively. We detect the appearance of shallow steps and (0001) terraces at the SiC inner surface. SiC surfaces reconstruction and terraces creation by step bunching leads to the preferential alignment of silicon crystallites with SiC. The Fast Fourier transforms (FFT) shown for Si and SiC parts of the image confirm the previously found crystallographic relationship between them. The image was corrected for all the distortions using the AbStrain procedure<sup>15</sup> and strain tensor components were extracted in the Si part with reference to the Bravais lattice of Si [Fig. 3(c), in-plane, out-of-plane and shear strain components]. The average values of all the strain components shown in the images are very small indicating that the Si layer is quasi-relaxed. Some small compression of this structure measured with reference to the Si Bravais lattice might result from the CTE difference between SiC and Si during cooldown or might indicate carbon atoms incorporation into the Si structure to a concentration not exceeding at most 0.5%.<sup>16</sup>

The measurement of the Si film thickness for all the samples indicates that their eventual values exceed the nominal ones. The evolution of the ratio  $h/h_0$  with temperature extracted for all the samples, where  $h_0$  is the nominal thickness,  $h$  is the measured thickness, is plotted in Fig 3(b) (black symbols). We can observe that for 1100 °C,  $h/h_0$  equals 1 for  $h_0 = 40$  nm and it is only a few percent greater than 1 for the other samples. When temperature increases, the ratio increases differently for different  $h_0$ . The smallest ratio change is seen for  $h_0 = 40$  nm, where it increases by only a few percent at 1400 °C. When  $h_0 = 8$  nm, the ratio rises above 1.1–1.15, staying constant between 1300 and 1400 °C. The strongest



**FIG. 3.** (a) Bright-field cross-sectional  $(1\bar{1}00)^{\text{SiC}}$  TEM images and diffraction patterns of the SiC/Si/SiC structures subjected to annealing at  $T < T_{\text{mp}}$  for 30 min. From left to the right:  $T = 1300$  °C,  $h_0$  of 8–40 nm; from top to the bottom:  $T$  of 1100–1400 °C,  $h_0 = 20$  nm. (b)  $h/h_0$  from x-ray reflectivity measurements (black open symbols) and TEM measurements (solid symbols) and voids' volume-per-surface fraction (red open symbols) evolution with temperature; (c) HR-STEM HAADF  $(1100)$  cross-sectional image of the C-face SiC/Si interface of the 20-nm-thick sample annealed at 1400 °C for 30 min and AbStrain analysis<sup>15</sup> of this image providing strain tensor components in Si with reference to its Bravais lattice.

evolution of the ratio is observed for  $h_0 = 20$  nm. First, it increases to 1.15 when temperature reaches 1200 °C. A further increase in temperature results in a stepwise increase in the ratio to 1.35 at 1300 °C and then to 1.43 at 1400 °C.

When the evolution of the surface fraction of voids with temperature [Fig. 2(c)] and that of  $h/h_0$  [Fig. 3(b)] are examined, it is obvious that they have likely a one-to-one correlation. Such a finding strongly supports an idea of the Si material redistribution from voids. We could further confirm such a correlation at the macroscopic scale. Figure 4(a) presents the results of the x-ray reflectivity measurements of the Si film at the bonding interfaces.

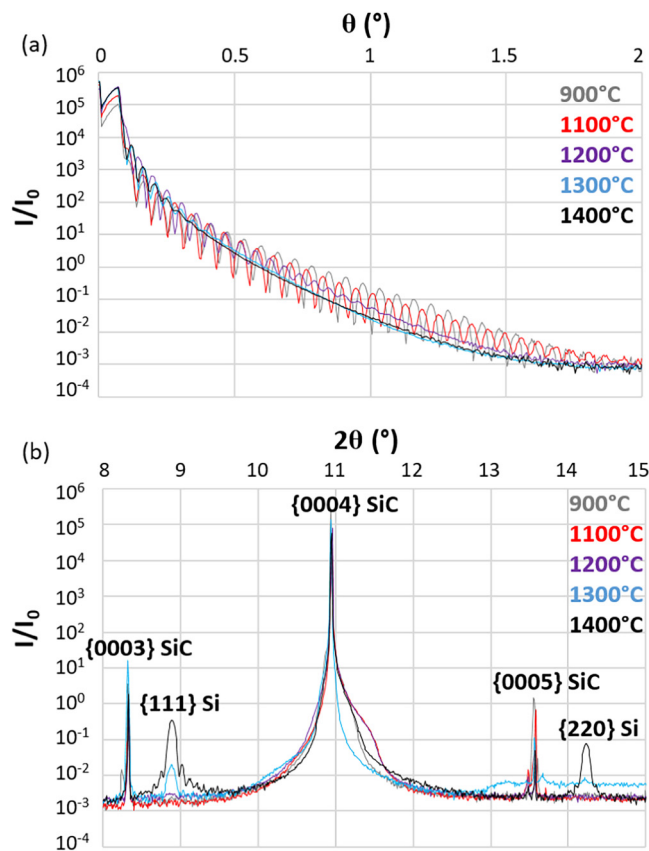
Each reflectivity curve shows interference (equal inclination) fringes with a certain amplitude and period  $T(2\theta)$ . The fringe period provides information on the thickness of the film.<sup>17</sup> The Si film thickness is obtained from the relation  $h = \frac{\lambda}{T(2\theta)}$ , where  $\lambda$  is the x-ray wavelength ( $\lambda = 0.4592$  Å in our experiments). As  $T(2\theta)$  decreases with temperature, the Si film becomes thicker with annealing temperature. The  $h/h_0$  ratio evolution with temperature which was extracted from these curves [Fig. 3(b), black open symbols] is in very good agreement with that obtained by the local TEM measurements [Fig. 3(b), black solid symbols].

The evolution of  $h/h_0$  with temperature can be compared to that expected from the Si material released by voids,  $\frac{1}{1 - \pi r^2 \rho_v}$  assuming silicon volume conservation. Here,  $\pi r^2$  is the

average projected area of the voids of radius  $r$  and  $\rho_v$  is the void's areal density. The observed one-to-one correlation between  $\frac{h}{h_0}$  and  $\frac{1}{1 - \pi r^2 \rho_v}$  [Fig. 3(b) (red symbols)] indicates that the Si material, contributing to the rise in Si layer thickness, comes from voids, and Si volume conservation during annealing is fully satisfied.

From the reflectivity curves, we also show that the contrast of the interference fringes decays faster with angle at higher annealing temperature. This is due to roughening of the internal surfaces ranging from 2 to 15 Å at the highest annealing temperature below the Si melting point. This evolution corresponds to a slight step bunching at SiC internal surfaces that already starts in the solid phase, which was confirmed by STEM images.

A crystallographic rearrangement of the Si structure accompanied with the grain thickening, previously detected by local TEM studies, was also confirmed by the measurements at the macroscopic scale. Figure 4(b) shows the x-ray  $\theta/2\theta$  diffraction spectra aligned in  $\theta/2\theta$  on the bottom substrate obtained for the sample with a 20 nm-thick Si film subjected to the second annealing at different temperatures. The spectra contain several peaks coming from the SiC and Si structures. The peaks at 7.8°, 10.44°, and 13.1° correspond to the {0003}, {0004}, and {0005} planes of 4H-SiC. The shoulder on the right hand side of the 004 SiC peak is caused by the slight tilt disorientation between the two SiC crystals (substrate and film) as part of the scattered intensity of the SiC film still



**FIG. 4.** (a) XRR of the silicon film at the bonding interface; (b) x-ray  $\theta/2\theta$  diffraction spectra obtained for the structures with a 20 nm-thick Si film subjected to successive first annealing at 900–1000 °C (gray curve) and second annealing at different temperatures ranging from 1100 to 1400 °C for 30 min.  $\lambda = 0.4592$  Å.

enters the detector slit. The peaks at  $8.38^\circ$  and  $13.73^\circ$  arise from the Bragg reflection from the  $\{111\}$  and  $\{220\}$  Si planes. This finding evidences the preferential alignment of  $\{111\}$  and  $\{220\}$  Si planes with  $\{0004\}$  SiC planes. The diffraction peaks from the Si layer appear at 1200 °C and their intensity increases with annealing temperature. It suggests a progressive texture and epitaxial alignment of the Si layer with the SiC substrates. The epitaxy of the  $\{111\}$  Si planes with SiC seems more favorable than for the  $\{220\}$  Si planes (intensity higher). The hexagonal symmetry of the 4H-SiC structure may be the cause for the favoring 111 3 fold texture evolution.

Eventually, the Si diffraction peaks reach a maximum intensity after annealing at 1400 °C and present a set of periodic fringes around. Based on the fringe spacing measured for the 111 Si diffraction peak, the thickness of the Si crystallites is estimated of 28.2 nm. This value is close to the Si film thickness of 29.5 nm which was extracted from the reflectivity curve. The slight difference is of the order of magnitude of the roughness indicating that Si crystallites extend throughout the entire film thickness.

Altogether, these data show a strong tendency of initially polycrystalline Si layer to get an epitaxial relation with the SiC substrates with high enough annealing temperature. SiC surfaces step bunching together with  $\{0001\}$  terraces creation is the driving force for silicon crystallographic rearrangement. The stability of such a transformation will be addressed in the next part of the work, where Si layer morphology evolution is studied as a function of isothermal annealing.

### C. Second isothermal anneal at $T < T_{mp}$ of 1300 °C

Figure 5 presents the top-view SEM images of the Si films of different thicknesses subjected to an annealing at 1300 °C for 4 and 240 min [the images of the corresponding structures annealed at 1300 °C for 30 min are shown in Fig. 2(a)].

The thinnest Si film contains both pits and voids after 4 min of annealing. A part of voids is coalesced. The voids remain the same in density and size after 240 min of annealing while the pits are mostly healed out. The 20 nm-thick Si film contains both pits and voids after 4 min of annealing. The voids are present in a much lower proportion than pits. The voids have a relatively small density of  $0.7 \mu\text{m}^{-2}$  which prevents their coalescence. Thus, such a short annealing time was not enough to allow the transformation of all the pits into the voids in this sample. The rest of the pits is either transformed into voids after 240 min of annealing or healed out, a state which has been already reached after 30 min of annealing. The 40 nm-thick Si contains mainly a high density of pits and a few voids after 4 min of annealing. After 240 min of annealing, pits were healed out while the density of voids remains the same.

These findings indicate that non-transformed pits can be effectively healed either at a high enough temperature during a relatively short period of time or at a moderate temperature during long enough annealing. In contrast, similar size of non-coalesced voids as well as the absence of changes in the void morphology after longer than 30 min annealing, show that voids have reached an equilibrium state. At this state, the driving forces for further thermal evolution of voids have disappeared. The transformation of the Si structure from a polycrystalline state to a single crystal obeying the epitaxial relationship with the SiC substrates may play a role in this evolution.

In the next part, we present the results of the study of Si layer morphology evolution under annealing at temperatures above the silicon melting point.

### D. Second anneal at $T > T_{mp}$

Starting at low temperatures, it takes a comparatively long time to reach a temperature higher than  $T_{mp}$ . Thus, before melting, the Si layers have been subjected to all the transformations revealed in the structures annealed at  $T < T_{mp}$ . It can be considered as the initial state of the system. The results of the eventual transformations of the SiC/Si/SiC structures after annealing at  $T > T_{mp}$  are presented in Fig. 6. Similarly to the structures annealed at  $T < T_{mp}$ , we investigate the effects of isochronal and isothermal annealing and the Si layer thickness.

Figures 6(a) and 6(b) show  $52^\circ$ -tilted top-view SEM images and bright-field TEM cross-sectional  $(1\bar{1}00)^{\text{SiC}}$  images, respectively, of the structures with a 20 nm-thick Si layer, which are arranged as



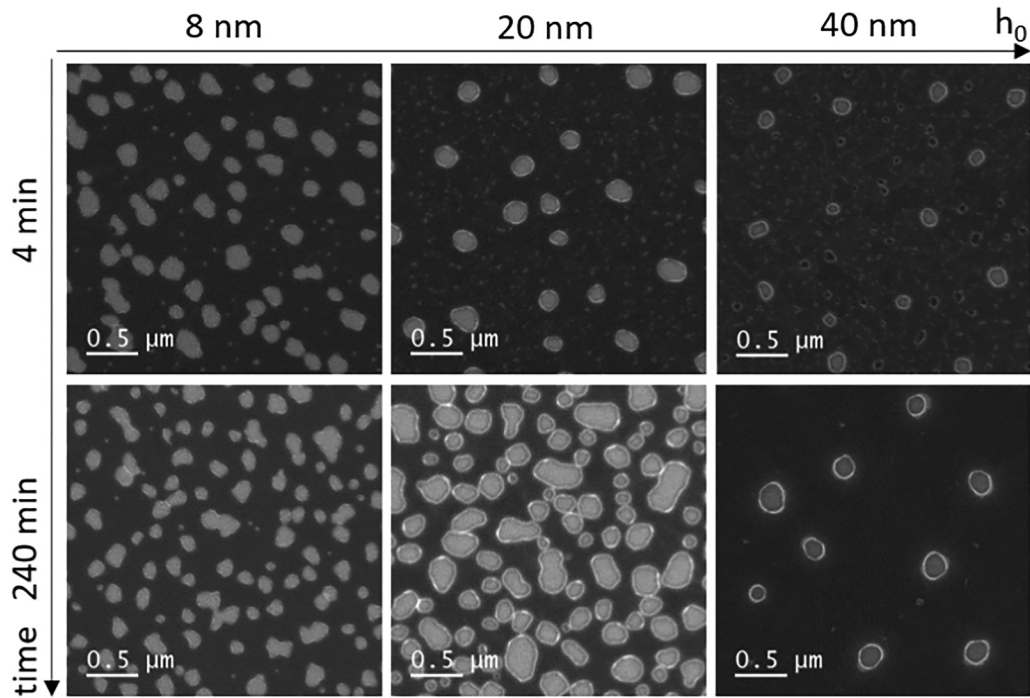
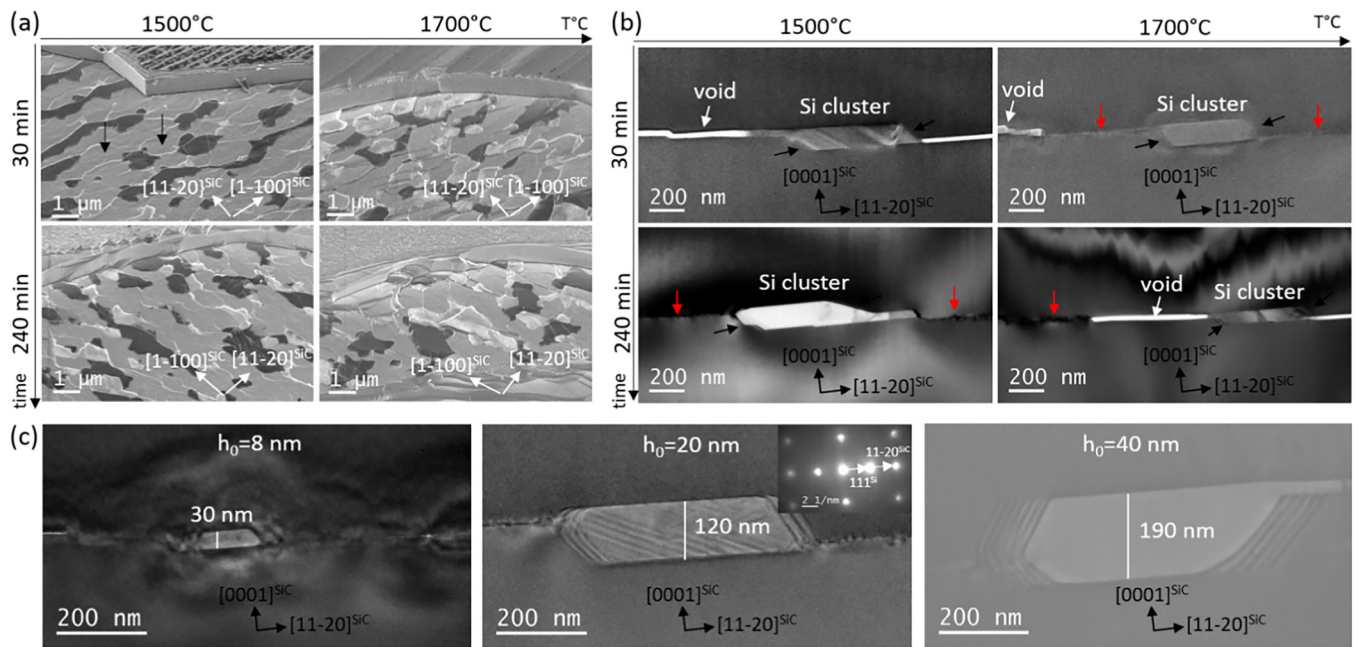


FIG. 5. Top-view SEM images of the Si films of different thicknesses after the second annealing at 1300 °C for 4 and 240 min.



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FIG. 6. (a) 52°-Tilted top-view SEM images; (b) bright-field cross-sectional (1100) TEM images, obtained for the structure with a 20-nm-thick Si film after annealing at 1500 and 1700 °C for 30 and 240 min; and (c) bright-field cross-sectional (1100) TEM images of the structures with three different Si film thicknesses: 8, 20, and 40 nm, annealed at 1700 °C for 30 min.

a function of annealing temperature, 1500 and 1700 °C (lines) and time, 30 and 240 min (columns). The most striking observation here is that the SiC interfaces underwent noticeable morphological evolution: they are no longer flat but present step bunching at both sides [see white contrasted lines in Fig. 6(a) and steps marked by black arrows in Fig. 6(b)]. The large terraces of a width of  $1.5\ \mu\text{m}$  [marked by black arrows in Fig. 6(a)] and steps of a height of 100 nm correspond to the  $(0001)^{\text{SiC}}$  and  $\{11\bar{2}4\}^{\text{SiC}}$  planes, respectively. The steps are elongated, in average, along the  $1\bar{1}00^{\text{SiC}}$  direction in accordance to the  $4^\circ$  miscut misorientation of the  $(0001)$  SiC wafer surfaces. The surface of the transferred SiC layer, which remained after cleaving out procedure [Fig. 6(a), upper part of the images], is also reconstructed with a periodicity of 300–800 nm and a step height of 20–50 nm depending on the annealing temperature. These values are significantly lower than those found for the internally bonded SiC surfaces. As a result, step bunching is far more effective when the Si layer is present. Annealing temperature or time do not impact significantly the height of the steps or the width of terraces, indicating that step bunching process has terminated already after annealing at 1500 °C for 30 min. We relate this effect to the observed redistribution of Si material.

Indeed, silicon is accumulated in the form of “ribbons” at the valleys preceding the SiC steps [see dark contrasted zones in Fig. 6(a) and “pockets” marked by the arrow in Fig. 6(b)]. Diffraction pattern taken over the Si inclusion [Fig. 6(c), inset] demonstrates that it has a monocrystalline structure with the epitaxial relation to the SiC wafers:  $(112)^{\text{Si}}//\{0001\}^{\text{SiC}}$ ,  $[111]^{\text{Si}}//11\bar{2}0^{\text{SiC}}$ ,  $[1\bar{1}0]^{\text{Si}}//1\bar{1}00^{\text{SiC}}$ . Most of the inclusions analyzed both in cross-sectional and plan-view configurations demonstrate similar Si-to-SiC structural relationship. This finding was further confirmed by the macroscopic x-ray diffraction measurements (not shown). It should be noted that these relations differ from those determined after annealing at  $T < T_{\text{mp}}$ . There, Si recrystallization presumably takes place over wide  $(0001)$  terraces rather than over very shallow steps. For  $T > T_{\text{mp}}$ , TEM observations [see Fig. 6(c)] show that the crystallization of silicon pockets upon cooldown may have processed laterally from the  $\{11\bar{2}4\}^{\text{SiC}}$  side steps.

The voids with a height of 20 nm are detected in all the samples between the Si ribbons [see white contrasted bands marked by white arrows in Fig. 6(b)]. The voids have an average lateral size of 2 and  $0.5\ \mu\text{m}$  for the annealing temperatures of 1500 and 1700 °C, respectively. Such a lateral shrink of voids with temperature is found to be assisted with their vertical shrink until reaching a direct SiC/SiC contact. The latter was not detected after annealing at 1500 °C for 30 min. In contrast, it does appear and interface closure progresses after annealing for a longer period of time or at higher temperatures [see regions marked by red arrows in Fig. 6(b)]. Based on the TEM images, the fraction of the closed SiC/SiC surface was estimated to be of 60% and 70% after annealing at 1700 °C for 30 min and 1500 °C for 240 min, respectively. These data indicate that continuous SiC/Si/SiC and SiC/SiC interface evolution is a thermally activated process mediated by silicon present between the two SiC substrates. In the next part, we address the effect of the amount of Si material, i.e., the Si layer thickness, on the interface evolution.

Three structures with as-deposited thickness of Si films of 8, 20, and 40 nm were annealed at 1700 °C for 30 min. Figure 6(c) shows the bright-field TEM cross-sectional  $(1\bar{1}00)^{\text{SiC}}$  images of the

corresponding structures. We observe that the height of steps increases with the Si film nominal thickness, reaching a value of 30, 120, and 200 nm for a 8, 20, and 40 nm-thick Si films, respectively. There is a proportional rise in the terraces' width between the steps. Terrace width increases from  $0.5\ \mu\text{m}$  for a 8 nm Si film to  $2\ \mu\text{m}$  for a 20 nm Si film and reaches a value of  $3\ \mu\text{m}$  for a 40 nm Si film. The step height-to-terrace width ratio varies from 0.06 to 0.07, i.e., it remains quasi-independent of the Si layer thickness. From a geometrical consideration, this value fits well the tangent of the  $4^\circ$  offcut angle. Based on these findings, more Si material leads to more prominent step bunching.

Finally, direct contact SiC/SiC interface was estimated to occupy 75%, 60%, and 50% of the whole interface in the structures with a 8, 20, and 40 nm-thick Si layers. Thus, for thinner Si films, the SiC/SiC interface closes more effectively.

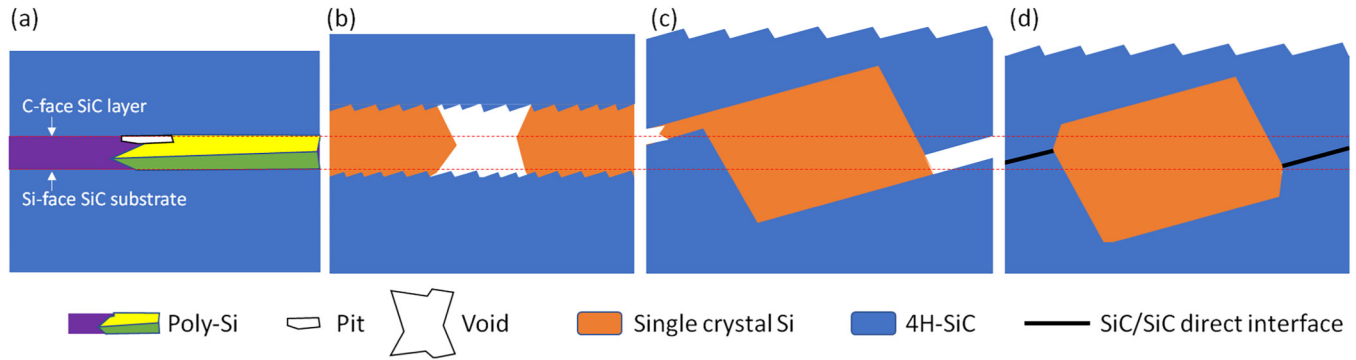
From this part of experiment, we learned that silicon strongly promotes SiC internal surface step bunching during annealing at  $T > T_{\text{mp}}$ . Step bunching occurs at the very beginning of Si layer melting and does not evolve further with temperature or time of annealing. Thicker silicon layers provide a greater degree of step bunching. In contrast, formation of larger areas with a direct SiC/SiC interface is favored for thinner Si layers, at higher annealing temperatures and time.

#### IV. DISCUSSION AND MODELING

The data collected on the morphology and crystalline phase evolution of a Si layer sandwiched between Si-face SiC substrate and C-face SiC layer with annealing at a temperature below and above  $T_{\text{mp}}$  allow for a construction of the following scenario (Fig. 7).

##### A. Evolution for $T < T_{\text{m}}$

We can describe the processes occurring during such a transformation by implying the classical approach of nucleation and dewetting theory. Solid-state dewetting is described as a mechanism of self-diffusion of the constituent material at grain boundaries, surfaces, or both. At the high temperatures considered here ( $T > 900\ \text{°C}$ ), the diffusivities are increased and diffusion is underlying all the observed evolution, from material displacement to crystal grain evolution. In addition, silicon is well above its ductile-brittle transition temperature and many defect-assisted plasticity phenomena can occur in the material. For  $T \geq 1100\ \text{°C}$  (i.e.,  $T/T_{\text{m}} > 0.8$ ), many phenomena like power-law creep, diffusional flow have been reported when the material is subjected to shear stress. Even for shear stresses of the order of  $10^{-3}$  of shear modulus, shear strain rates above  $10^{-4}\ \text{s}^{-1}$  are reported.<sup>18</sup> In our few nm-thick confined films, Laplace pressures are of this order of magnitude so that in the following solid silicon will be considered as a viscous liquid, with possible variations of surface tensions upon orientation. Note that at temperatures close or above the roughening transition, step mobility is very high so that surface behavior of this plastic solid should not be very different from a liquid. Similarities and differences between solid and liquid wetting have been discussed in recent studies.<sup>19</sup>



**FIG. 7.** Schematic illustrating the evolution of the system under different stages of annealing at  $T < T_{mp}$  and  $T > T_{mp}$ : (a)  $T = 900\text{--}1000\text{ }^\circ\text{C}$ ; (b)  $1100\text{ }^\circ\text{C} < T < 1414\text{ }^\circ\text{C}$ ; (c)  $1500\text{ }^\circ\text{C} < T < 1700\text{ }^\circ\text{C}$ ; and (d)  $T > 1700\text{ }^\circ\text{C}$ . Two horizontal dotted lines represent the initial position of the Si/SiC interfaces.

### 1. Pit nucleation and transformation

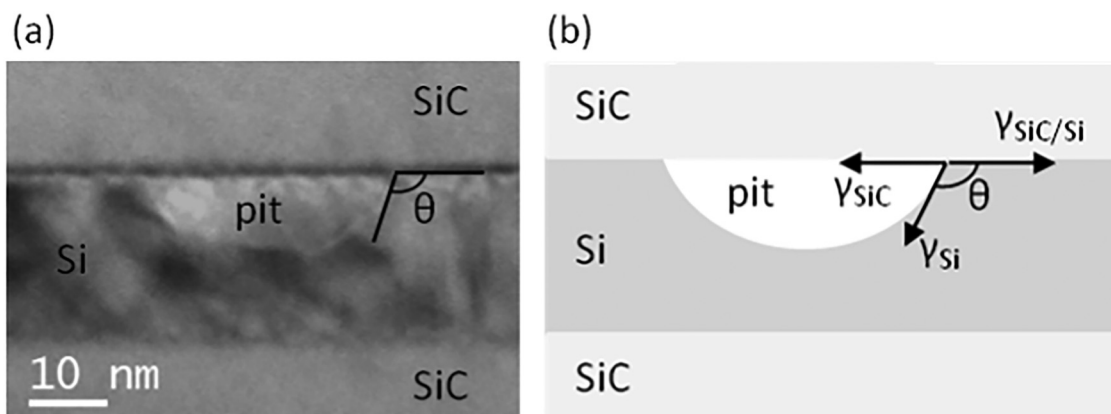
Already after the first annealing at  $900\text{--}1000\text{ }^\circ\text{C}$  [Fig. 7(a)], the pits are formed in the poly-Si layer at the C-face SiC/Si interface. Pits are likely to be created as a result of thin film solid-state dewetting in accordance with the state-of-the-art findings.<sup>20–22</sup> In our system, dewetting becomes possible due to a low binding energy between a polycrystalline Si and  $4^\circ$  offcut C-terminated surface of the SiC layer. Places with relatively high roughness of C-face SiC surface or where it is in contact with Si grain boundaries can be considered as the preferential sites for pits nucleation. Pit density's independence from the Si layer thickness supports this hypothesis. When observed by TEM [see Fig. 8(a)], pits have the shape of spherical caps with a Si/SiC contact angle larger than  $\pi/2$ . We assume Si only partially wets SiC. Hence, writing Young–Laplace equation, we obtain

$$\frac{\gamma_{\text{SiC}} - \gamma_{\text{SiC/Si}}}{\gamma_{\text{Si}}} = \cos \theta, \quad (1)$$

where  $\gamma_{\text{SiC/Si}}$ ,  $\gamma_{\text{Si}}$ , and  $\gamma_{\text{SiC}}$  are the surface tensions of SiC/Si, Si/vacuum, and SiC/vacuum interfaces, respectively. For the contact angles larger than  $\pi/2$ ,  $\cos \theta < 0$  and hence  $\gamma_{\text{SiC/Si}} > \gamma_{\text{SiC}}$ . The system will reduce its energy by “replacing” SiC/Si interfaces by SiC/vacuum interfaces, it tends to “dewet.”

From Eq. (1), the spontaneous formation of an interface pit is possible if  $\frac{\gamma_{\text{SiC}} - \gamma_{\text{SiC/Si}}}{\gamma_{\text{Si}}} \leq -1$ . When  $\frac{\gamma_{\text{SiC}} - \gamma_{\text{SiC/Si}}}{\gamma_{\text{Si}}} > -1$ , an interface pit should shrink and disappear unless it is stabilized, e.g., by rough surface asperities.<sup>23–25</sup> For the case of polycrystalline silicon with different grain orientations,  $\gamma_{\text{Si}}$  and  $\gamma_{\text{SiC/Si}}$  are expected to vary from grain to grain so that conditions for dewetting may be reached locally. Interface pit formation and growth can be facilitated at grain boundaries<sup>26</sup> and rough surfaces<sup>23</sup> due to the presence of convex surfaces, as predicted by Mullins *et al.* for solid-state dewetting in a layer-over-substrate system.<sup>27–29</sup> The opposite process of pit healing may occur due to  $\gamma_{\text{SiC/Si}}$  decrease with temperature (hence decrease of contact angle, better wetting). This decrease may be due to the experimentally observed appearance of epitaxial

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**FIG. 8.** (a) Bright-field cross-sectional ( $1\bar{1}00$ ) TEM image of a pit for a 20 nm-thick Si film after the first annealing at  $900\text{--}1000\text{ }^\circ\text{C}$  and (b) schematic of a pit illustrating the surface energies  $\gamma$  and the SiC/Si contact angle  $\theta$ .

relation between Si and SiC (see above paragraph in Sec. III B). Associated to this improved wetting, the energy barriers and critical sizes for pit growth will increase so that most of the existing pits will become unstable against healing. A similar example of the effect of the change of contact angle  $\theta$  on energy barriers and critical size is shown below on the void geometry.

### 2. Void formation and growth

When the height of a pit reaches the thickness of the film, a void is created with a radius  $r$  and height  $h$  [Fig. 9(a)]. From Young equation, silicon should have different contact angles  $\theta_c$  and  $\theta_{Si}$  with the top (C-face) and the bottom (Si-face) SiC surfaces. Yet, since  $\theta_c$  and  $\theta_{Si}$  are not too different at  $T > T_{mp}$ ,<sup>30</sup> for the sake of simplicity, for  $T < T_{mp}$ , we will use in the following a single average value  $\theta = \frac{1}{2}(\theta_c + \theta_{Si})$ .

We can analyze the nucleation and growth conditions for such a hole using again a simple capillary type energy analysis. The free energy change associated with a hole creation and growth is given by

$$\Delta E = \Delta E^{wall} + \Delta E^{base} + \Delta E^{\Delta P}, \quad (2)$$

where  $\Delta E^{wall} = \gamma_{Si} S^{wall}$  is the energy cost associated to the creation of the hole sidewall of surface  $S^{wall}$ ,  $\Delta E^{base} = 2(\gamma_{SiC} - \gamma_{SiC/Si}) S^{base}$  is the energy gain due to increase of the dewetted surface  $S^{base}$ ,  $\Delta E^{\Delta P} = -\Delta PV \cong -\Delta P \pi r^2 h$  is the work of the pressure difference  $\Delta P$  at the void/Si interface proportional to the void volume  $V$ . In the following discussion, we shall take  $S_{wall} \approx 2\pi r h$ , i.e., a cylinder approximation for the sidewall surface area, while  $S_{base} = \pi r^2$ . These approximations allow one to capture the dependence of different terms in (2) while keeping simple expressions. As has been established by the experiments, the void height changes with annealing satisfying Si volume conservation. Following the work of Srolovitz and Safran,<sup>26</sup> we assume that the density of voids can be presented as  $\rho_v = \frac{1}{\pi r_0^2}$ , where  $\pi r_0^2$  is the average maximum surface area containing a single void. The thickness of a layer without and

with voids can be formally presented as the volume-per-surface fraction  $h_0 \pi r_0^2 \rho_v$  and  $h \pi (r_0^2 - r^2) \rho_v$ , respectively. Due to the Si mass conservation, we get for the silicon thickness  $h$ ,

$$h = h_0 \frac{r_0^2}{(r_0^2 - r^2)}. \quad (3)$$

The energy barrier for stable void nucleation can be reached by maximizing the potential  $\Delta E$  of the system with respect to a change of radius hole  $r$  while the mechanical equilibrium can be reached by its minimizing. By substituting  $\gamma_{Si} \cos \theta$  for  $\gamma_{SiC} - \gamma_{SiC/Si}$  [Eq. (1)] and introducing a variable  $x = \frac{r}{r_0}$ , we get for the  $\Delta E$  variation,

$$d\Delta E = 2\pi \left( \frac{h_0(\gamma_{Si}(x^2 + 1) - \Delta P r_0 x)}{(x^2 - 1)^2} + 2\gamma_{Si} \cos \theta r_0 x \right) dr = 0. \quad (4)$$

Thus, at equilibrium, the following condition should be satisfied,

$$\Delta P = \gamma_{Si} \left( \frac{x^2 + 1}{r_0 x} + \frac{2 \cos \theta (x^2 - 1)^2}{h_0} \right). \quad (5)$$

Because external hydrostatic pressure and pressure inside the void are zero, the pressure balance within Si imposes that  $\cos \theta < 0$  and

$$\begin{cases} \Delta P_{c/eq} = \gamma_{Si}(x^2 + 1) \left( \frac{1}{r_1} - \frac{1}{r_2} \right) = 0, \\ r_1 = r_0 x, \\ r_2 = -\frac{h_0(x^2 + 1)}{2 \cos \theta (x^2 - 1)^2}. \end{cases} \quad (6)$$

Here,  $\Delta P_{c/eq}$  is an expression for the Laplace pressure of curved surfaces with principal radii of concave curvature  $r_1$  and convex

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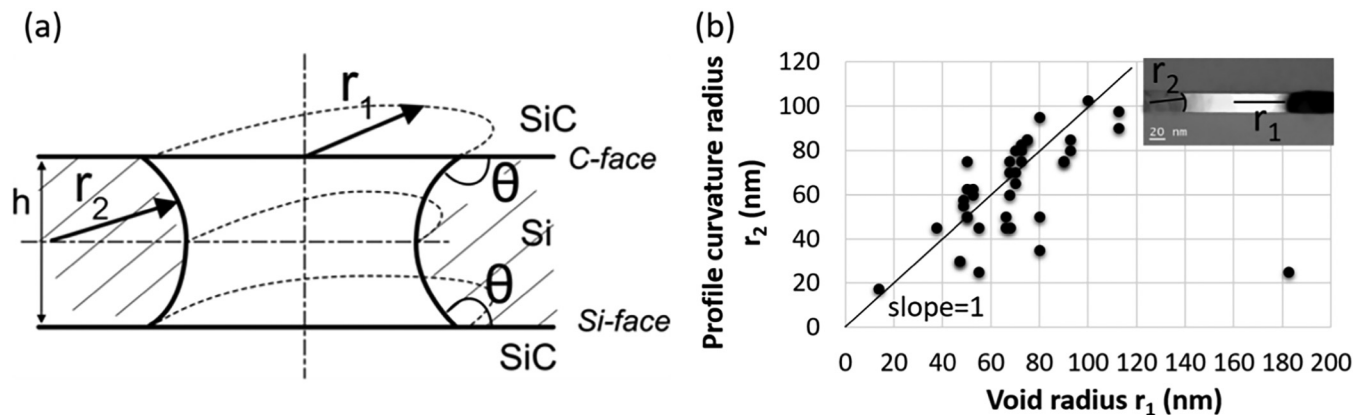


FIG. 9. (a) Schematic of the equilibrium situation of the hole with curved surfaces at pressure  $P = 0$ . The two principal radii of curvature are then opposite and (b) plot of  $r_2$  (profile curvature radius) as function of  $r_1$  (void radius) as measured from TEM images.



curvature  $r_2$ . Figure 9(b) presents the evolution of  $r_2$  as a function of  $r_1$  (here,  $r_1 = r$ ), measured in the TEM images, evidencing that in average  $r_1 \cong r_2$ . This indicates that in our system, the equilibrium situation corresponds to  $\Delta P_{c/eq} \approx 0$ . With  $\Delta P = 0$ , the free energy change of the system of Eq. (2) reads

$$\Delta E|_{\Delta P=0} = 2\gamma_{Si}\pi r_0^2 \left( \frac{h_0}{r_0} \frac{x}{1-x^2} + \cos\theta x^2 \right). \quad (7)$$

This expression shows directly the different dependencies with radius of the (positive) wall and (negative) base terms in the energy. As in the classical homogeneous nucleation theory, this difference in the  $r$  dependence gives the energy barrier (see below): while the (linear) wall term dominates at small  $r$ , the dewetting tendency due to dewetted surface areas (quadratic) will dominate at larger radii. This situation would not change when a more exact expression (e.g., catenoid surface area) for the wall surface area has been used, as the first term would have kept a linear  $h$  proportional term. This term proportional to  $h$  can be viewed as the effect of confinement to dewetting.

Figure 10 shows the  $\Delta E|_{\Delta P=0}$  normalized by  $2\gamma_{Si}\pi r_0^2$  extracted for 8, 20, and 40 nm-thick Si layers annealed at 1300 °C. Here, we used  $\gamma_{Si} = 0.75 \text{ J}\cdot\text{m}^{-2}$  and the values  $r_0^8 = 96 \text{ nm}$ ,  $r_0^{20} = 117 \text{ nm}$ , and  $r_0^{40} = 253 \text{ nm}$  which were estimated from Fig. 2(b).

Each of the curves presents a maximum peak at  $r_c = x_c r_0$  ( $x_c \ll 1$ ) corresponding to the energy barrier for void nucleation and a minimum peak at  $r_{eq} = x_{eq} r_0$  ( $x_{eq} \approx 1$ ) corresponding to the minimum energy state of the system appearing during void growth. The exact values of  $r_c$  and  $r_{eq}$  can be extracted by solving Eq. (6). Their approximate values can be estimated by developing Eq. (6) for  $x \ll 1$  and  $x \approx 1$  and

$\frac{h_0}{r_0} \ll 1$  providing

$$\begin{cases} x_c \approx -\frac{r_0}{h_0} \left( \cos\theta + \sqrt{\cos^2\theta - \left(\frac{h_0}{r_0}\right)^2} \right) \approx -\frac{h_0}{2 r_0 \cos\theta}, \\ x_{eq} \approx 1 - \frac{1}{\sqrt{-\left(\frac{1}{2} + 4\frac{r_0}{h_0} \cos\theta\right)}}. \end{cases} \quad (8)$$

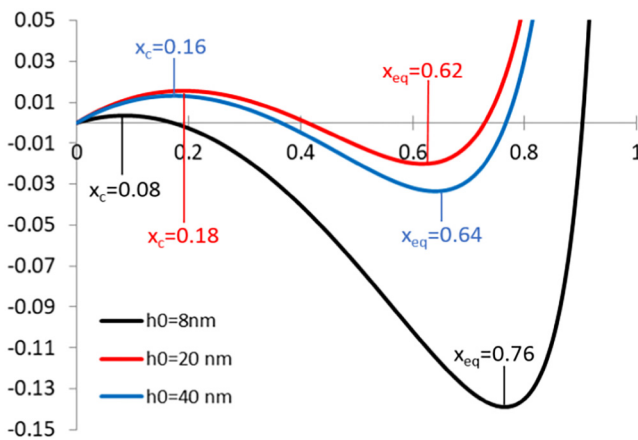
By using  $\theta = 120^\circ$  and experimentally obtained values for  $r_0^{h_0}$ , we get  $x_c$  values of 0.08, 0.18, and 0.16 (Fig. 10) and  $r_c$  values of 8, 21, and 41 nm for the Si film thicknesses of 8, 20, and 40 nm, respectively. The smallest voids observed in the corresponding SEM images have a radius of 10, 20, and 45 nm in agreement with the fact that voids with a smaller radius than the critical radius are unstable and tend to heal. From Eqs. (7) and (8), an expression for the energy barrier can be obtained,

$$\Delta E = \gamma_{Si}\pi h_0^2 \left( -\frac{1}{2 \cos\theta} \right). \quad (9)$$

Both expressions (8) and (9) indicate that in our partial wetting conditions [ $\theta > 90^\circ$ ,  $\cos(\theta) < 0$ ], a decrease of contact angle (associated, e.g., to lower  $\gamma_{SiC/Si}$ ) will increase both energy barriers and critical radius, making void growth or film dewetting more difficult.

Similarly, the values for the void equilibrium radius can be estimated to be of 73, 72, and 162 nm in the samples with  $h_0$  equal to 8, 20, and 40 nm, respectively. While being within the range of radii measured experimentally for the largest voids, these values exceed that of average radii measured experimentally. Such a discrepancy can be explained by the approximation made on surface tensions and contact angles. Those parameters are expected to vary with the annealing temperature. Alternatively, an increase in the Si layer thickness with void development may not be the only reason for their limited growth at long times. We have seen that the silicon crystal structure also evolves with time from a polycrystal with small grains to a strongly textured single crystal which is co-oriented with the SiC structure. As a consequence, both SiC/Si interface energies and Si surface energies are expected to change upon annealing. It has been noted that when temperature increases, the contact angles between Si and SiC decrease, going to values smaller than  $\pi/2$  for liquid silicon over SiC.<sup>31–33</sup> If  $\cos\theta > 0$ , the driving force for dewetting will be reduced and no equilibrium minimum can be found [Eq. (7)].

We also observed more substantial dewetting in the 20 nm-thick Si film when compared to the thinner and thicker films. One possible explanation for this behavior can be a change in Si grain size across different Si films, as well as a higher surface roughness of the C-face of the SiC layer in the 20 nm-thick Si layer structure, which could result in a higher density of pit nucleation centers. Another hypothesis is that the kinetics of dewetting and the kinetics of recrystallization of poly-Si into single crystal compete with each other based on film thickness. A thinner film recrystallizes faster toward the epitaxial relationship with SiC. As the system progresses to a lower SiC/Si interface energy, the driver



**FIG. 10.** Evolution of the free energy of a void of radius  $r$  normalized by  $2\gamma_{Si}\pi r_0^2$  showing the critical nucleation ratio  $x_c = \frac{r_c}{r_0}$  and the equilibrium ratio  $x_{eq} = \frac{r_{eq}}{r_0}$  for the three different thicknesses  $h_0$  of 8, 20, and 40 nm ( $r_0^8 = 96 \text{ nm}$ ,  $r_0^{20} = 117 \text{ nm}$ ,  $r_0^{40} = 253 \text{ nm}$ ,  $\theta = 120^\circ$ ).

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for dewetting disappears earlier. On the other hand, an excessive Si film thickness is unfavorable for the pit-to-void transformation, which reduces void density.

More complete capillary models for both pit and hole free energy calculation could be developed to account for a non-90° contact angle using, e.g., a catenoid shape for the hole. This would eventually change the dependence with radius in Eq. (7) and decrease the energy barrier at small  $r$  in the strongly non-wetting case. Yet, the energy barrier values calculated, e.g., using Eq. (9), are much larger than  $k_B T$  ( $k_B$  is the Boltzmann constant) showing that pit and void nucleation remains an essentially heterogeneous nucleation process. Eventually, simulations using Kinetic Monte Carlo may be necessary to fully describe the shape evolution from a pit generated at an interface to a piercing void. Curitto *et al.*<sup>34</sup> developed such calculations for solid-state dewetting of a film over a substrate. Our observations support their vacancy-clustering simulations predicting the formation of interface voids, which may eventually span to the entire film creating a void, depending on the interaction energy values.

## B. Evolution for $T > T_{mp}$ : Liquid Si behavior

When the system has been subjected to all the previously described transformations and temperature is further increased above  $T_{mp}$ , silicon melts. The presence of liquid Si is the cause of the pronounced step bunching that happens both at C-face and Si-face SiC inner surfaces [Figs. 7(c) and 7(d)]. These steps have heights that are five to seven times larger than that of steps formed on the surface of the transferred SiC layer. Because carbon dissolves efficiently in molten Si, it can be further transported with an extremely large diffusion coefficient of around  $5 \times 10^{-8} \text{ m}^2/\text{s}$ ,<sup>35</sup> which is even larger than in a gaseous atmosphere.<sup>36,37</sup>

During this step bunching process mediated by liquid Si, C atoms being released from the step facets are transferred above the steps over the (0001) terraces. When Si is in the molten state, carbon transport is fast and surface reconstruction of the SiC vicinal surface with 4° offcut occurs rapidly. Small steps with small terraces are rapidly replaced by large steps and large terraces. When the step height (on each surface) is equal to the film thickness, the volume of silicon is insufficient to maintain a continuous film covering of the whole surface area and to carry on the carbon transport; the continuity of the silicon film between two steps is broken and carbon transport from step to step can no longer be achieved. The step bunching mediated by molten silicon stops at this point. This creates a quasi-closed cavity filled with liquid Si [Figs. 6(a) and 7(c)]. These cavities are roughly parallel to the offcut/step edge direction. Around these silicon-filled linear cavities, SiC surfaces can come in direct contact but voids created by liquid silicon dewetting may also be occasionally observed.

Such a proposed scenario fits well our observations. A thicker Si layer produces more prominent step bunching and provides less surface fraction of the direct SiC/SiC contact. Consistently, a larger annealing temperature, the longer time or smaller Si layer nominal thickness promote more efficient closure of the SiC/SiC interface.

## V. CONCLUSIONS

Motivated by the growing interest in bonding of materials dedicated to high-power electronics, we studied the morphological

and crystalline phase thermal evolution of a Si film sandwiched between Si-face 4H-SiC substrate and C-face 4H-SiC layer, transferred by SmartCut™ technology. In particular, we addressed the effect of the Si film thickness, annealing temperature, and time on the changes in the initially amorphous Si layer.

At the lowest annealing temperature studied (900–1000 °C), Si layer becomes polycrystalline and its dewetting arises from the roughest C-face SiC surface through a heterogeneous nucleation process. Dewetting starts by the formation of pits not crossing the layer at interfaces.

Further thermal annealing at temperatures below Si melting point results either in healing of most of the pits or their transformation into voids piercing the whole Si film. Si atoms released from the voids contribute to an increase in Si layer thickness, keeping the process conservative. A capillary model of the evolution of the free energy of the system showed the specific effect of confinement on dewetting and predicted that such an increase in the Si layer thickness could result in the appearance of some equilibrium state when the voids stop growing. Large dewetting and increase of the film thickness is experimentally evidenced for thinner silicon films (8–20 nm). For thicker films (40 nm), dewetting stops before reaching a high surface coverage. This may be due to poly-Si structure transformation into a single crystal with an epitaxial relation to SiC.

When temperature increases above the Si melting point, liquid Si promotes the step bunching at both SiC inner surfaces thanks to a strongly enhanced transport of Si and C atoms. When steps and terraces from opposite sides come together, quasi-closed pockets form, which act as a reservoir for liquid Si. For a sufficiently long duration or at a high enough temperature, the interface locally closes around these pockets. As a result, Si inclusions formed during cooling are surrounded by SiC/SiC direct contact interface. The thinner is the Si film, the larger the surface fraction of the direct SiC/SiC interface. It reaches a value of 75% with the thinnest Si film of 8 nm.

The established morphological and microstructural changes in the SiC/Si/SiC system subjected to annealing at moderate temperatures and that exceeding Si melting point provides a solid foundation for a more in-depth understanding of physical phenomena occurring during fabrication of substrates dedicated to high-power electronics and their reaction on extreme temperatures.

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## AUTHOR DECLARATIONS

### Conflict of Interest

The authors have no conflicts to disclose.

## Author Contributions

**Maëlle Le Cunff:** Conceptualization (lead); Data curation (lead); Formal analysis (equal); Investigation (lead); Methodology (lead);

Writing – original draft (lead). **François Rieutord**: Conceptualization (equal); Formal analysis (equal); Investigation (supporting); Methodology (supporting); Supervision (supporting); Writing – review & editing (equal). **Didier Landru**: Conceptualization (supporting); Investigation (supporting); Methodology (supporting); Supervision (supporting); Writing – review & editing (supporting). **Oleg Kononchuk**: Conceptualization (supporting); Investigation (supporting); Methodology (supporting); Supervision (supporting); Writing – review & editing (supporting). **Nikolay Cherkashin**: Conceptualization (equal); Formal analysis (equal); Investigation (supporting); Methodology (equal); Supervision (lead); Writing – review & editing (equal).

## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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