



HAL
open science

Repetitive Short-circuits on 650 V GaN

Adrien Lambert, Hervé Morel, Dominique Planson, Luong Viêt Phung,
Dominique Tournier, Pascal Bevilacqua, Laurent Guillot

► **To cite this version:**

Adrien Lambert, Hervé Morel, Dominique Planson, Luong Viêt Phung, Dominique Tournier, et al..
Repetitive Short-circuits on 650 V GaN. PCIM Europe 2024, Jun 2024, Nuremberg, Germany. hal-
04626451

HAL Id: hal-04626451







<https://hal.science/hal-04626451>

Submitted on 26 Jun 2024

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Repetitive Short-circuits on 650 V GaN

Adrien Lambert^{1,2} , Hervé Morel¹ , Dominique Planson¹ , Luong Việt Phung¹ ,
Dominique Tournier¹ , Pascal Bevilacqua¹, Laurent Guillot² 

¹ INSA Lyon, Université Claude Bernard Lyon 1, Ecole Centrale de Lyon, CNRS, Ampère, UMR5005, France

² STMicroelectronics, France

Corresponding author: Adrien Lambert, Adrien.lambert@st.com

Speaker: Adrien Lambert, Adrien.lambert@st.com

Abstract

The study consists in analyzing the robustness of 650 V GaN HEMT components in case of short-circuits. The objective is to develop a test bench for repetitive short-circuits to a component. Electrical characterizations will be carried out before and after the short-circuit cycles to identify the possible parameters drift of the tested devices, to identify the failure mechanisms. Parametric variations have been observed.

1 Introduction

Wide-band gap (WBG) components, and specifically gallium nitride (GaN) High Electron Mobility Transistor (HEMT), are expected to be highly promising in the field of power electronics. Indeed, these transistors have enviable performances with reduced conduction and switching losses and thus a high cutting frequency, up to a few MHz. Nevertheless, a proven robustness and reliability are essential for their commercialization on a large scale, in particular in the automotive field with traction control system of electric vehicles or in the aeronautics field. With simultaneous high-voltage and high-current, short-circuits represent one of the most undesirable events due to the significant amount of energy to be dissipated [1]. Two types of short-circuit are mainly distinguished, type I (a hard switching fault, the component is gated on under full tension) and type II (a fault under load, the fault appears while the component is gated on). Type I, considered as the most frequent and de facto preferred for testing, is studied here.

The study of short-circuits began a few years ago, with initial work observed in 2013 [2]. However, it remains limited in several respects. The normally-off technology of p-GaN and cascode components has been studied almost exclusively. Current studies of enhanced mode (e-mode) components

based on p-GaN components have revealed that the highest voltages could only be achieved at the cost of concessions (overheated environment, increased gate resistance) ([1], [2], [3], [4], [5], [6], [7]). To the best of our knowledge, very few, if any, papers focus on normally-on technology depletion mode (d-mode). What is more, current studies are mainly concerned with the robustness of components to a single short-circuit and the time to failure.

The study presented here differs in several ways: normally-on components, MIS-HEMT technology (insulated gate HEMT[1]) and normally-off (p-GaN[1]) components are chosen. P-GaN technology is chosen as this structure seems to be preferred in the current industrial development.

Component	V _{th}	I _d	R _{ds_ON}
D-mode	-12.5 V	10 A	250 mΩ
p-GaN Batch 1	1.8 V	15 A	120 mΩ
p-GaN Batch 2	1.7 V	11 A	150 mΩ

Table 1 Different types of studied components

In addition, it has been chosen to study the impact of repetitive, non-destructive short-circuits, as the severe damage of the component complicates the study. What is more, in a real-life application, the aim is to have only non-destructive short-circuits, repeated a few times in the life of the converter.

These short-circuits are interspersed with electrical characterizations to identify parametric variations and gain a better understanding of degradation and failure mechanisms. The study of induced damage is therefore a key point and it will contribute to the design of more short-circuits robust chips.

2 Test Set-Up

2.1 Technical Choices

Previous short-circuit studies has often reported high overvoltage (>100 V) limiting the drain-source voltage range during short-circuit testing [1]. Because of the very fast current fronts typical of GaN technology, any parasitic inductance in the PCB power loop leads to a significant overvoltage at the component level and turns out to be deleterious.

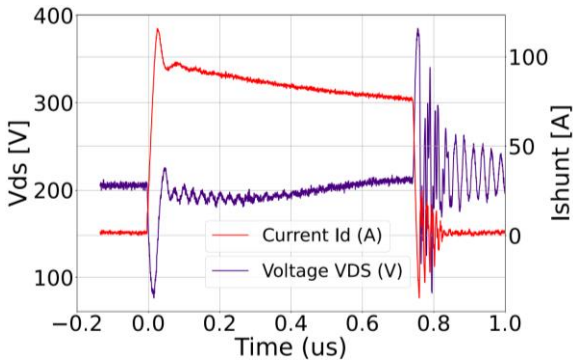


Fig. 1 Typical drain-source voltage and drain current measured at short-circuit

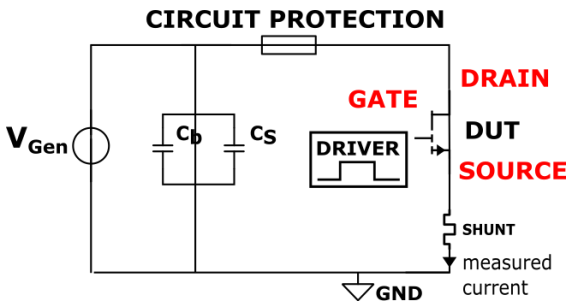


Fig. 2 Electrical diagram of the test bench

For the studied DUTs, with a short-circuit current of around 50 A (low estimate) and a typical switching time of 20 ns, a parasitic inductance of 80 nH causes 200 V of overvoltage! The circuit has therefore been designed to reduce the wiring inductance as much as possible. The protection element, often active switch like IGBT, considered highly inductive, is replaced here by an SMD fuse, which likely preserves the circuit before its destruction. To reproduce short-circuit conditions, and in particular the rapid rise of a high-current, while minimizing the voltage drop, two capacitors

of 2 μF (ceramic with ultra-low ESR, C_s) and 133 μF (polypropylene, C_b) respectively are connected in parallel. The test bench consists of three key elements: the power mother board with capacitors, fuse, and current measurement shunt; the "device" daughter board with the transistor encapsulated in its sarcophagus, and the driver section for -24 V / 0 V or -3 V / + 6 V control.

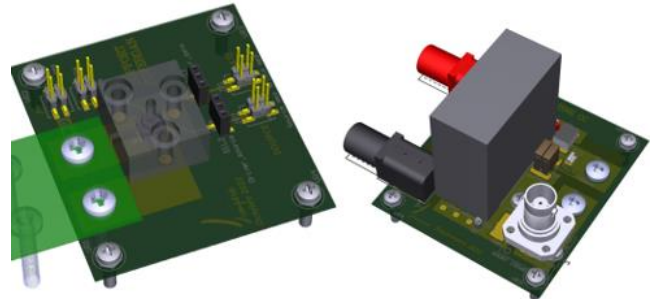


Fig. 3 Device Daughter Board and Power mother Board

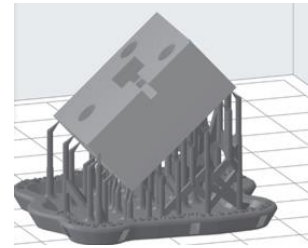


Fig. 4 3-D printed sarcophagus

To reduce component handling, which could affect these electrical properties, the daughter board has been designed to be easily connected to the Keysight B1505A characteristic tracer. In addition, to avoid soldering/unsoldering of components on this daughter board, and thus cause significant thermal stress, a 3D-printed sarcophagus was designed to maintain the component and ensure pressure conduction (Fig. 4).

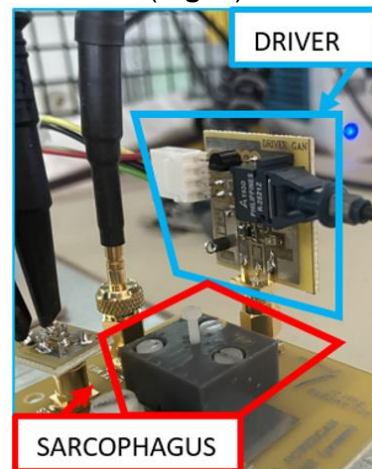


Fig. 5 Daughter Board with Attached Driver

Similar electrical characterizations with a brazed component ensured that the sarcophagus did not interfere with the component electrical properties.

2.2 First Optimisation of the Test-Bench Set-up with D-mode components

2.2.1 First Short-circuits

Particular care has been taken to reduce parasitic inductances in advance. This involves careful routing and optimised compactness, as well as surface-mounted components with reduced ESL (Equivalent Series Inductances).

Despite this, the first short-circuits caused significant disturbance and the bench had to be adjusted. The first short-circuit was conducted for drain-source voltage V_{DS} of 10 V. Non-negligible overvoltages are observed at turn-off on V_{GS} and V_{DS} signals. For $V_{DS} = 50$ V, the signals oscillate at the risk of damaging the component or even causing it to break. Solutions therefore had to be found.

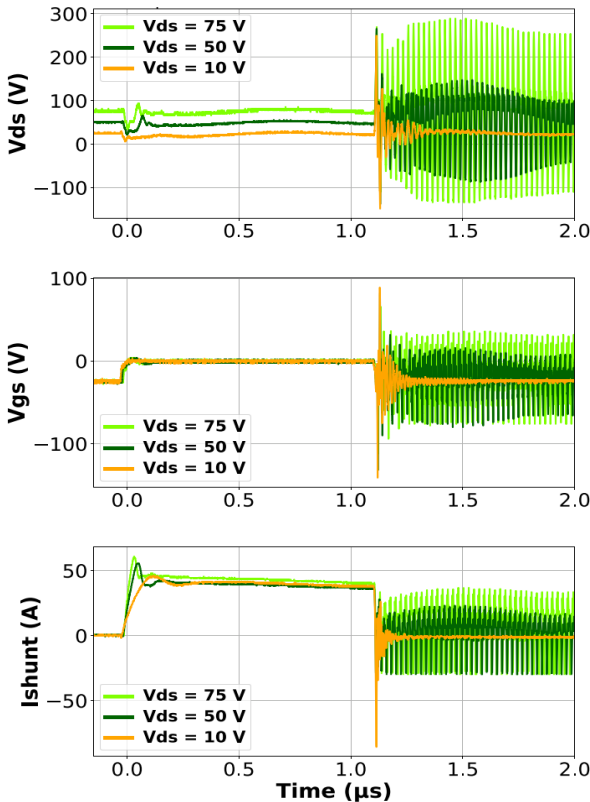
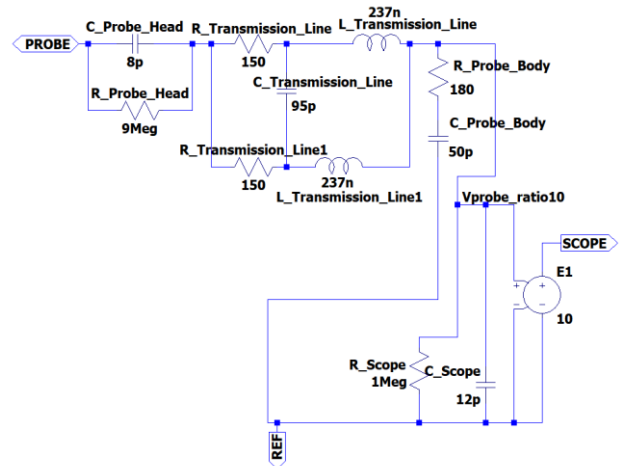


Fig. 6 First short-circuit with unstable behaviour

2.2.2 Impact of Voltage Probes (V_{DS} , V_{GS})

The observed overvoltages and oscillations necessarily raise the impact of the probes to the extent it can be questioned if the observed perturbations are an artifact of the probes or are truly undergone by the component. For this

purpose, a spice simulation of the experimental bench has been developed.



The spice simulation presents the significant interest of being able to access the voltages within the component to compare them to the voltages observed through the probes. A passive probe model is therefore developed

Fig. 7 Probe Spice model inspired by [8], [9], [10]

According to the results of simulation, the probes do not necessarily represent the reality of the signals observed on the oscilloscope. Different types of probes are tested. The V_{GS} signal is considered to be the most critical, so the study of the impact of the probes is focused on this signal. Three types of probes were studied: passive, differential and optically isolated differential. The different types of probes are summarized in the table below.

Type	Manufacturer	Reference
Passive Probe	Tektronix	TPP0500B
Differential Probe	Tektronix	THDP0100
Optically isolated differential probe	Tektronix	TIVM1

Table 2 Different types of used probes

Several tests are carried out at a reduced voltage $V_{DS} = 10$ V. In the case of differential probes, V_{GS} signals are directly obtained while it is calculated by subtracting the V_G and V_S signals when using passive probes.

Fig. 8 shows the full sequence of short-circuit while Fig. 9 focuses on the turn-off, the most-critical judged moment.

The differential probe, instead of improving the measurement, exacerbates the noise. The differences in the V_{GS} signal depending on the type of probe used are clearly visible. The differential probe is surprisingly the most disturbed, perhaps

because its use requires an electronic box, potentially disturbed by the magnetic field radiated by the experimental bench. Passive probes therefore turn out not to be the worst. The least noisy signal comes from the optically isolated probe.

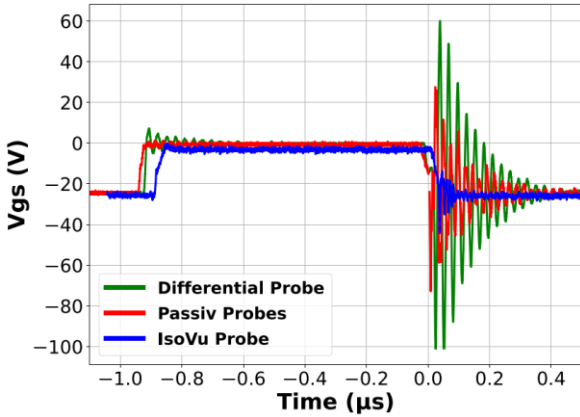


Fig. 8 Comparison of probes during short-circuit (full sequence)

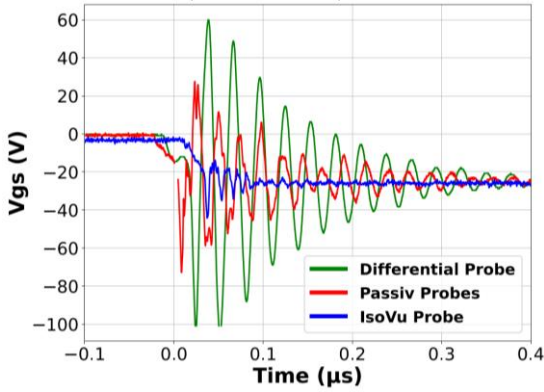


Fig. 9 Comparison of probes during short-circuit (zoom on Turn-OFF)

2.2.3 Impact of Current Sensing (I_s)

The shunt has its own inductance, and adding it to the board causes parasitic inductances. It was therefore investigated to what extent the shunt could have an impact.

It was studied whether the direction of the shunt ground position had an influence. Different test configurations were carried out. For config. 1, the ground leg of the shunt was soldered to the ground side of the high-voltage supply (in red on the diagram below), while for config. 2, the shunt ground was soldered to the source side of the device (in blue on the diagram below). The reduction of the loop formed by the shunt legs was also studied, to reduce the parasitic inductance caused. This corresponds to the optimized case and to configurations 4 and 5. Config. 3 corresponds to the absence of a shunt.

Type of config.	Technical choices
Config. 1	shunt mass side of PS ground
Config. 2	shunt mass side of DUT
Config. 3	no shunt
Config. 4	optimized shunt, mass side PS
Config. 5	optimized shunt, mass side DUT

Table 2 Different configurations to analyse the impact of shunt

Fig. 10 shows the entire duration of the short-circuit, while Fig. 11 shows a zoom of V_{DS} during the turn-off. It can be seen that, although the direction of the shunt is of little importance in terms of overvoltages on V_{DS} with very similar overvoltage between config 1 and 2, reducing the parasitic inductance generated by the shunt loop significantly reduces the overvoltage on V_{DS} from 75 V.

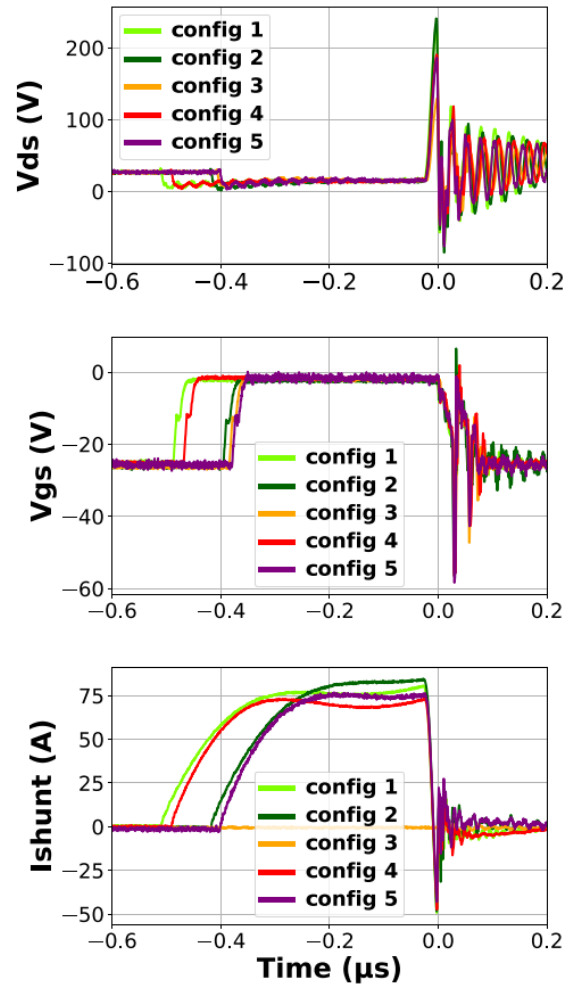


Fig. 10 Short-circuits measures considering several configurations

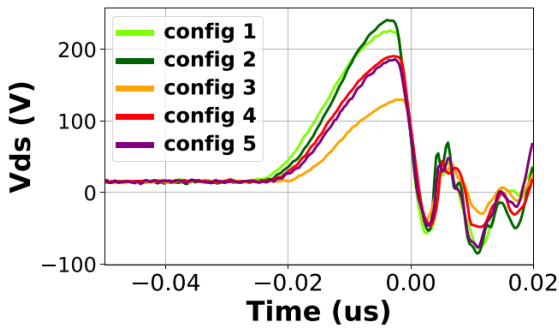


Fig. 11 Short-circuits (zoom on Turn-OFF)

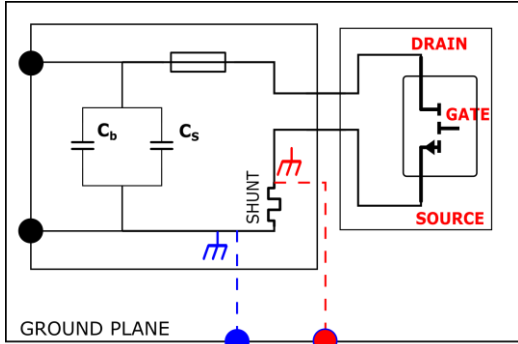


Fig. 12 Configuration 1 (blue) or 2 (red)

Reducing the parasitic inductances of the shunt significantly reduced the power loop and V_{DS} oscillations during Turn-OFF. A gradual rise in voltage could then be achieved for normally-ON components. Config.1 has been maintained. Tests for longer conduction times were also carried out. Tests for longer conduction times were also carried out. It can be noted in Fig.13 that the overvoltage is constant, what underlines it only depends current and inductance.

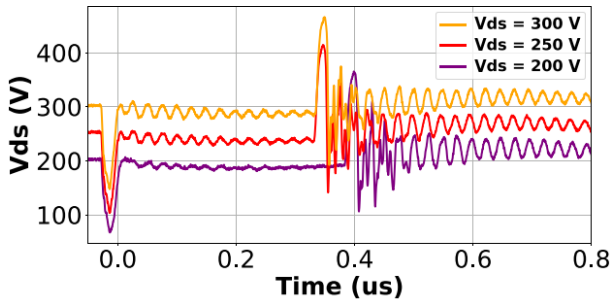


Fig. 13 Short-circuit for a gradually increased V_{DS}

2.3 Second Optimisation for N-OFF Components

The study is extended to normally-OFF devices, with p-GaN devices from two manufacturers (called batch 1 and batch 2) with similar characteristic. While the tests on the batch 1 did not pose any problems for drain-source biases of 100 V and 200 V (Fig. 14), it turns out to be different for batch 2. Various ways of improvement have been explored.

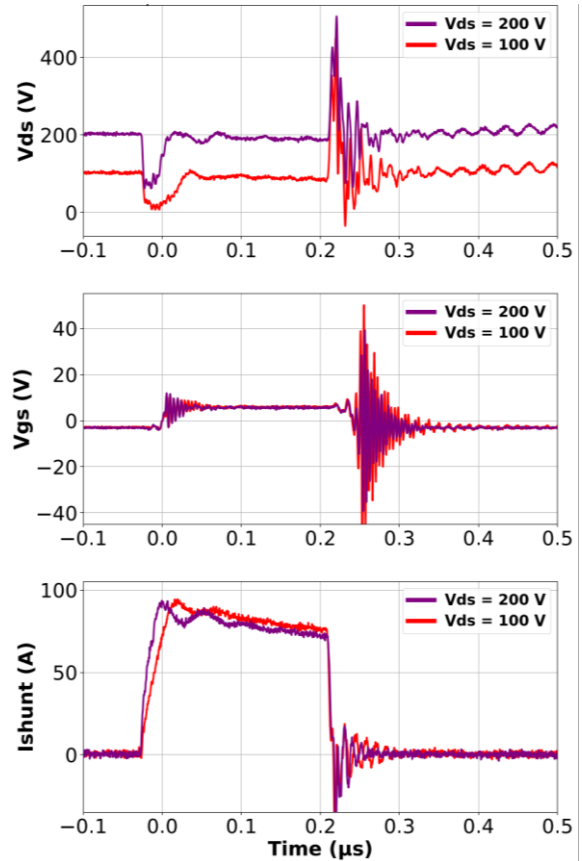


Fig. 14 Short-circuit for batch 1 component

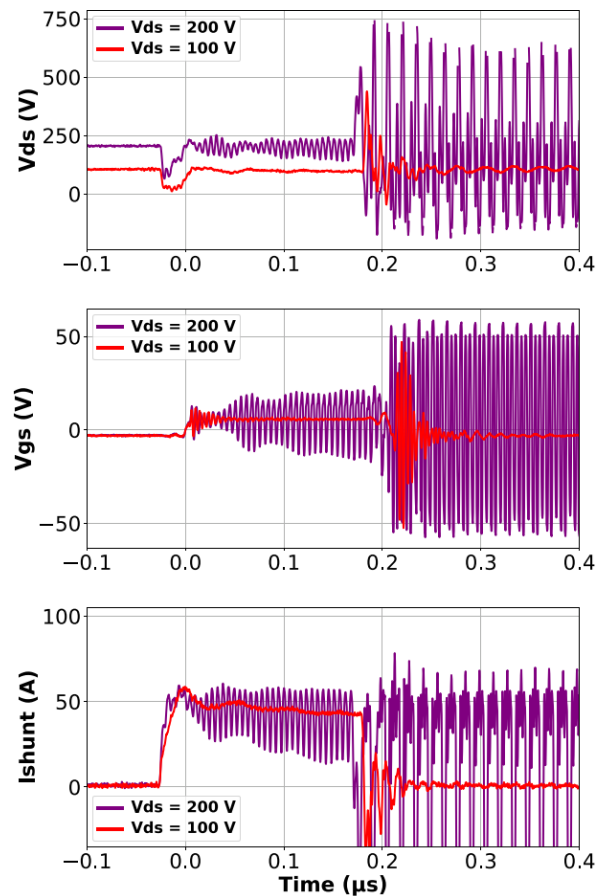


Fig. 15 Short-circuit for batch 2 component

2.3.1 Impact of the Gate-resistance

Increasing the gate-resistor was the first idea.

Indeed, by increasing gate-resistance, the authors [11] have observed an improvement in signals that had previously been disturbed by short-circuiting. It was tested to increase the R_{gOFF} resistance to $33\ \Omega$ compared with $22\ \Omega$ previously used. It did not improve the shape of signals at both $V_{DS} = 100\ V$ and $200\ V$. Given the lack of improvement and the fact that R_{gOFF} cannot be increased indefinitely, as the industry favours low value of gate-drive resistance to minimise losses, the impact of R_{gOFF} is not studied further.

2.3.2 Impact of Common Mode Current

Considering the absence of any improvement to the experimental bench and in view of the very high disturbance of the V_{GS} signal, it was decided to study the common-mode currents at the driver. The study focuses on the wire connection between the driver power supply board and the driver board.

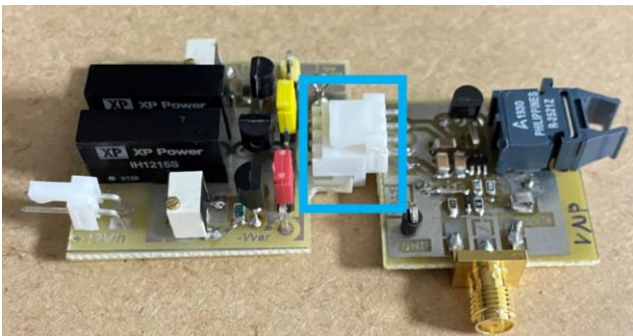


Fig. 16 Driver Power Supply (left) and driver Boards (right)

The initial configuration includes four connection wires ($V+Drive$, $V-Drive$, $+5V\ opto$, GND) between the driver power supply card and the driver. A first attempt at improvement was made by removing the wires by pinning the cards via the white connectors shown in the photo above. This first solution is unsatisfactory, and even degrading. Ferrite torus are then inserted into the wire connection

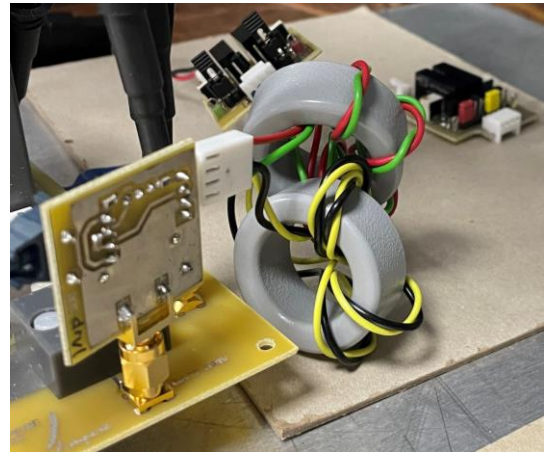


Fig. 17 Insertion of Ferrite Torus in the driver wires

The wires are first looped twice around the ferrite cores.

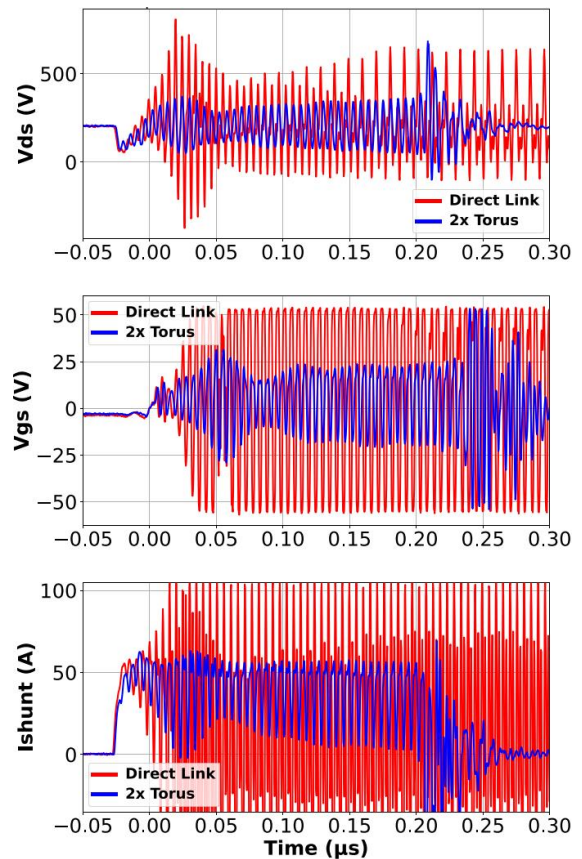


Fig. 18 Comparison between a direct connection without or with ferrite torus (looped twice)

The signals shown in **Fig. 17** demonstrate a appreciable reduction of disturbance. Considering that it was decided to increase the looping through the torus from two to five times. The first improvement is noticeable at $V_{DS} = 100\ V$. At $V_{DS} = 200\ V$, shown in **Fig. 18**, the results were indisputable with a significant stabilization.

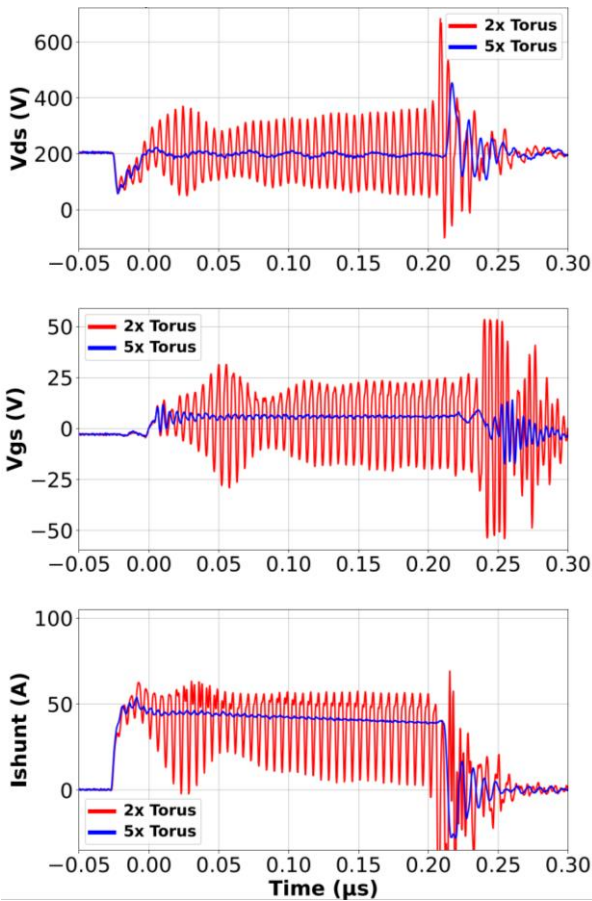


Fig. 19 Comparison between a connection with ferrite torus looped twice or five times

3 Results

The bench has been optimized to allow repetitive short-circuits of variable duration and V_{DS} polarization. Progressive voltage increases are achieved.

A distinction is made in this study between normally-ON, or D-mode, components from manufacturer 1 and normally-OFF or P-GaN components from manufacturers 1 and 2.

The components are subjected to a series of short-circuits of variable duration and variable V_{DS} polarization. Before and after each series of short-circuits, the components are characterized using a B1505 electrical tracer to record parameters such as Threshold Voltage (V_{th}) and on-state resistance (R_{dsON}). Each initial series of measurements includes the "Triple-Sens" [12] V_{th} reset protocol, allowing a reliable initial V_{th} value to be taken into account.

3.1 D-mode

Optimization of the test bench enables the voltage to be ramped up to the breaking point with a

maximum polarization $V_{DS} = 325$ V.

The B01505 characterizations reveal a variation in the threshold voltage. Figures ... and ... show respectively the variation of V_{th} in value or in relative terms to its initial value before short-circuit. This V_{th} variation is shown as a function of the energy accumulated during successive short-circuits. The study was continued for components in batch B, for polarization $V_{DS} = 200$ V and conduction times varying from 400 ns to 1 μs .

Fig. 20 shows the last three consecutive short-circuits experienced by component 17B. The failure before the end of the last short-circuit demonstrates the fatigue of the component due to the accumulation of successive short-circuits.

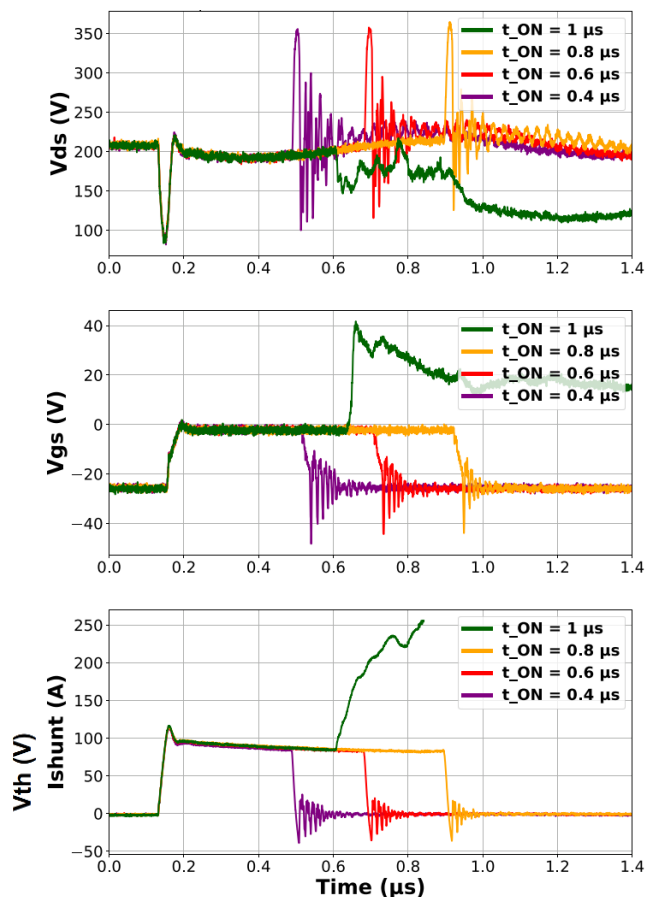


Fig. 20 Breakage of batch B component before the end of short-circuit

3.1.1.1 Static Variation

Fig. 21 and **Fig. 22** illustrate the influence of repetitive short-circuits on the threshold voltage, in some cases with a variation of more than 10%.

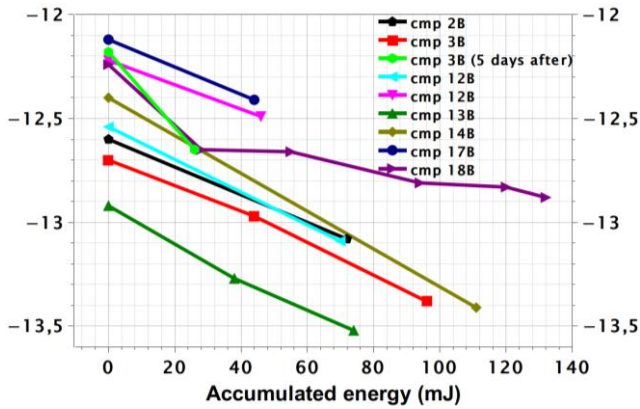


Fig. 21 V_{th} variation (in values) for D-mode Batch B

It is interesting to note the overall trend emerging from the multiple tests on the components in batch B, with a general reduction in threshold voltage to values even more negative than the initial value.

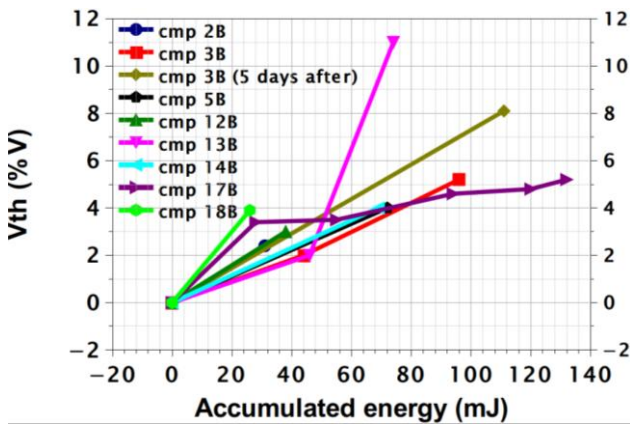


Fig. 22 V_{th} variation (in %) for D-mode Batch B

3.1.1.2 Dynamic Variation

As it is represented in the **Fig. 23**, an increase of the drain current was noted during the repetitive short-circuits on a part.

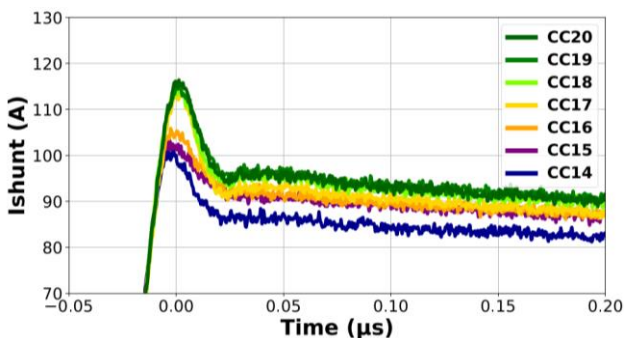


Fig. 23 Zoom on the drain current of component 17B during a series of consecutive short-circuits.

3.2 Normally-Off

3.2.1 P-GaN Batch 1

The p-GaN components in batch 1 are highly robust, which means that conduction times can be extended to as little as 10 μs . It was also possible to carry out a voltage rise, with a recorded break for $V_{DS} = 400 \text{ V}$ and 2 μs of conduction as shown in **Fig. 24**. The progressive degradation of the V_{GS} and V_{DS} signals at turn-ON can be seen as the voltage increases in **Fig. 24**.

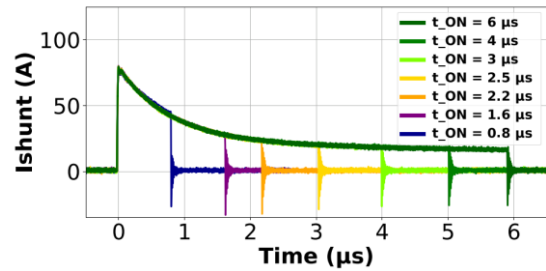


Fig. 24 Drain current signal for a progressive Increase of the conduction time for p-GaN component

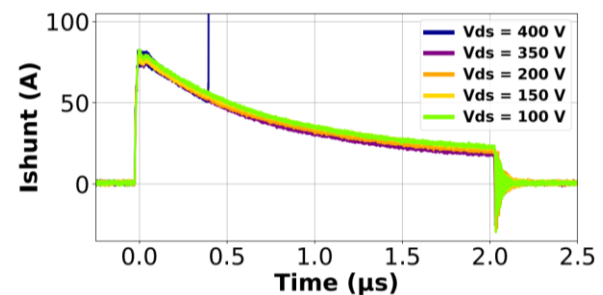
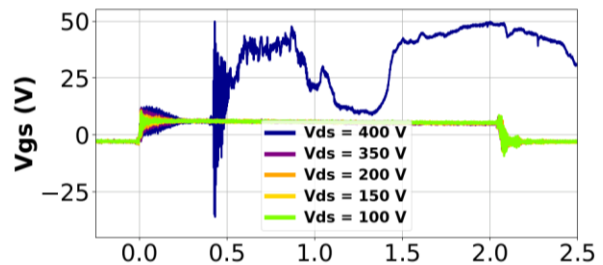
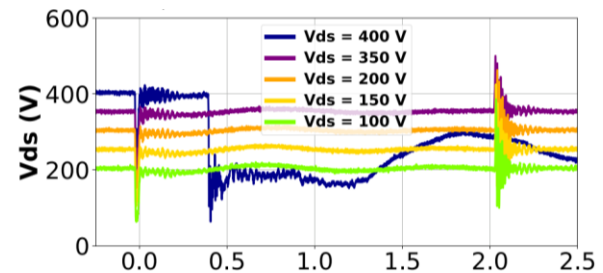


Fig. 25 V_{DS} , V_{GS} and drain current signals during a Rise in V_{DS} for p-GaN component with a breakage at $V_{DS} = 400 \text{ V}$

3.2.1.1 V_{th} Variation

Significant V_{th} variations have been observed as shown in Fig. 26 and Fig. 27.

To make these measurements reliable, witness component number 34, known as the "Golden Device" is used. This golden device is not short-circuited, but is characterized at the same time as other component. Small variation in V_{th} for the Golden device compared to short-circuited components demonstrates the impact of short-circuits on the variation in threshold voltage. It would be interesting to develop a measurement protocol which includes a temperature calibration.

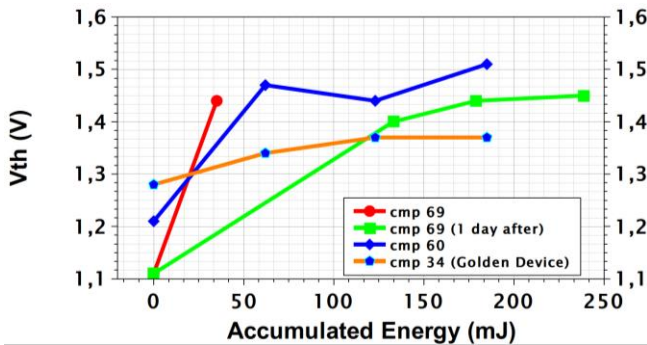


Fig. 26 V_{th} variation (in values) for p-GaN Batch 1

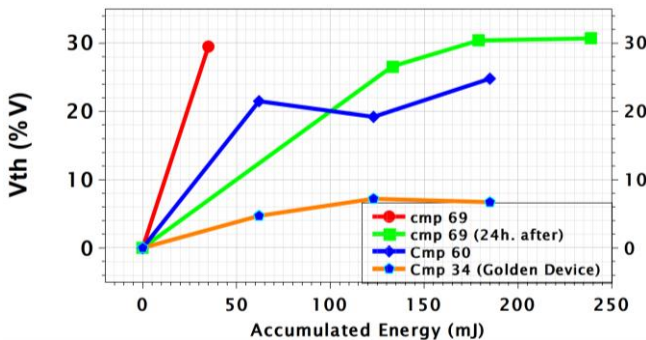


Fig. 27 V_{th} variation (in %) for p-GaN Batch 1

3.2.1.2 Rds-ON Variation

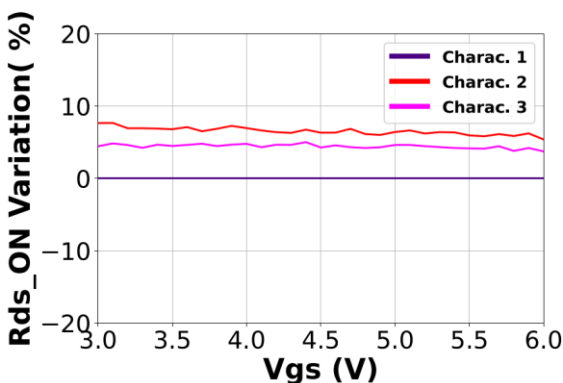


Fig. 28 Rds-ON variation for p-GaN batch 1

In view of the large variation in threshold voltage, an analysis of the possible variation in Rds-ON is

carried out. In the same way as for the V_{th} study, a component is taken as golden device. With a variation of Rds-ON below 1% between each characterization, it demonstrates that variation observed in short-circuited component is imputable to this specific stress. Fig. 28 shows a variation of Rds-ON between 5 and 10% for a short-circuited component.

3.2.2 P-GaN Batch 2

Although the p-GaN components in Batch 2 are also more robust than the D-mode components studied, they broke more easily than p-GaN batch 1 with a maximum V_{DS} of 300 V. Component failure does not always occur during conduction or at turn-off, as shown in the Fig. 29 below, which illustrates component failure AFTER turn-off.

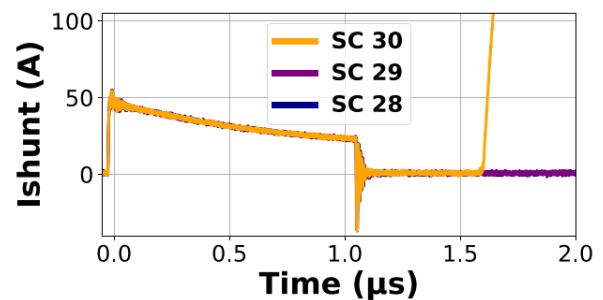


Fig. 29 Breakage after turn-off for p-GaN batch 2

3.2.2.1 V_{th} Variation

The potential variation of V_{th} is also studied and gives results considered similar to p-GaN batch 1, although slightly lower in variation and leads to Rds_on study.

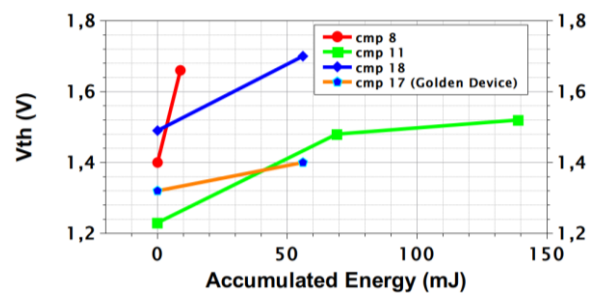


Fig. 30 V_{th} variation (in values) for p-GaN batch 2

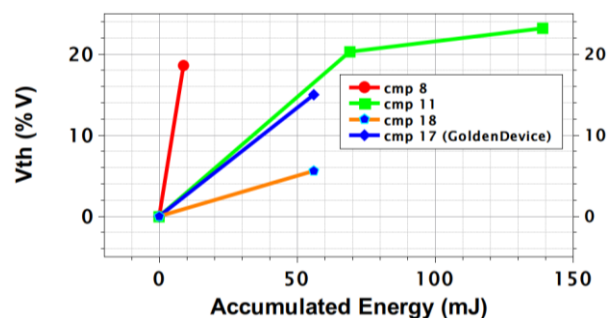


Fig. 31 V_{th} variation (in %) for p-GaN batch 2

3.2.2.2 Rds-ON Variation

As the batch 1, the variation of Rds-ON is studied. After a series of short-circuits, a variation of more than 10% is noted in **Fig. 32** in comparison to the initial situation, before the short-circuits. In the same way as batch 1, a golden device was taken, with a variation of less than 1% in the absence of short circuit, what demonstrates the impact of short-circuit.

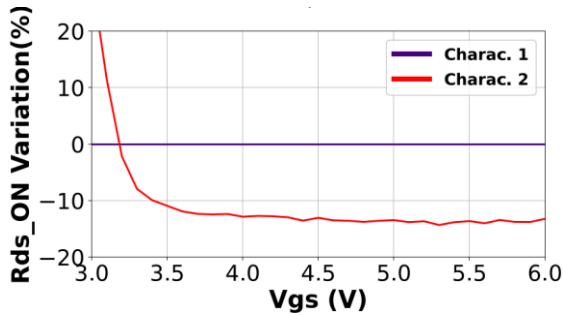


Fig. 32 Rds-ON variation for p-GaN batch 2

4 Conclusion

By optimizing the test bench, repetitive short-circuits were applied to normally-ON and normally-OFF components. Degradations were observed with non-negligible drift of static parameters such as the threshold voltage V_{th} and the on-state resistance. In the case of normally-ON components, a few dynamic variations of the short-circuit drain current were observed.

References

- [1] M. Landel, « Étude de la robustesse de transistors GaN en régime de court-circuit », p. 263.
- [2] C. Abbate, « Thermal instability during short-circuit of normally-off AlGaIn/GaN HFETs », *Microelectron. Reliab.*, 2013.
- [3] H. Li *et al.*, « Robustness of 650 V Enhancement-Mode GaN HEMTs under Various Short-circuit Conditions », p. 9.
- [4] T. Oeder, « Electrical and thermal failure modes of 600V p-gate GaN HEMTs », *Microelectron. Reliab.*, p. 6, 2017.
- [5] M. Riccio *et al.*, « Experimental analysis of electro-thermal interaction in normally-off pGaIn HEMT devices », p. 6.
- [6] M. Fernández *et al.*, « Short-Circuit Study in Medium Voltage GaN Cascodes, p-GaN HEMTs and GaN MISHEMTs », *IEEE Trans. Ind. Electron.*, p. 10, 2017.
- [7] P. J. Martínez, « Unstable behaviour of normally-off GaN E-HEMT under short-circuit », *Semicond Sci Technol*, 2018.
- [8] J. S. de Oliveira, « A Methodology for designing SiC and GaN device based converters for automotive applications ».
- [9] K. Ammous et H. Morel, « Analysis of Power Switching Losses Accounting Probe Modeling », *IEEE Trans. Instrum. Meas.*, vol. 59, n° 12, 2010.
- [10] K. Mbaitelbe, « Inductance dans son environnement: Caractérisation des inductances planaires intégrées dans les conditions d'utilisation de l'électronique de puissance ».
- [11] P. Xue, L. Maresca, M. Riccio, G. Breglio, et A. Irace, « Experimental Study on the Short-Circuit Instability of Cascode GaN HEMTs », *IEEE Trans. ELECTRON DEVICES*, vol. 67, n° 4, p. 7, 2020.
- [12] T. G. Bade, H. Hamad, A. Lambert, H. Morel, et D. Planson, « Threshold Voltage Measurement Protocol "Triple Sense" Applied to GaN HEMTs », 2023.