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# Modeling of IC Buffers from Channel Responses via Machine Learning Kernel Regression

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**Abstract**—This paper investigates the potential of a fully behavioral approach for the generation of accurate models of digital IC buffers based on conventional kernel regressions. The proposed approach does not assume a specific model structure like the classical two-piece model representation which has been massively used in literature, offering a promising and viable alternative to facilitate the modeling of nonlinear electrical devices. The collected results represent a first proof-of-concept, aimed at demonstrating the strengths of the proposed alternative modeling approach.

**Index Terms**—digital integrated circuits, buffer modeling, signal integrity, high-speed interconnects, kernel regression.

## I. INTRODUCTION

Since the early 1990s, there has been an growing interest of the signal and power integrity community in generating accurate and efficient simulation models of digital IC buffers for the quality and reliability assessment of high-speed digital channels.

The above trend was stimulated by the birth and by the subsequent improvements of the input output buffer information specification (IBIS) which was strongly supported by the electronic design automation (EDA) and silicon vendors [1]. IBIS suggests a physical-consistent modeling approach based on basic building blocks inspired by the constitutive elements composing the various IC buffers, with all the required features and recent technological advancements (including drivers and receivers, single-ended and differential technology, power-supply effects and pre/de-emphasis). IBIS models for single-ended and differential drivers assume a two-piece structure in which the output port current of the buffer is defined by the weighted combination of two submodels describing the device behavior in either the high or the low logic state. This assumption facilitates model estimation, allowing researchers concentrating on model advancements and additional features.

Based on the above picture, IC buffer modeling inspired by the IBIS idea has always been the mainstream solution which is well supported by both the EDA tools and companies, representing the natural playground for research (e.g., see [2] and references therein). A wide variety of research papers can be found in the literature, with the common background of assuming a two-piece structure and with the main differences

on the type and structure of submodels, ranging from physical-consistent modeling approaches to more behavioral solutions (mostly Artificial Neural Networks (ANNs) or Recurrent Neural Networks (RNNs)) [3]–[11].

In addition, some attempts in addressing the problem of IC modeling via a fully black-box behavioral approach based on ANNs have been followed [12], [13]. Even if a good accuracy was observed, some inherent critical aspects still have to be solved in order to have a robust modeling framework. ANNs generally require a possibly large number of neurons, a clever algorithm for training and for forcing a physical consistent behavior of models in a typical simulation environment, and a careful design of the training sequences, being this latter aspect also shared by the approaches in which a two-piece structure is assumed. In addition, a possible alternative blind modeling solution should be able to be flexible and general, to accommodate the inherent multiport electrical characteristic of IC buffers.

Among the above requirements, a key role is played by the simplification of the modeling procedure, including the training which should be done on-the-fly, i.e., based on the observation of device responses in a typical application scenario, without specific requirements and setup for custom excitation. Some preliminary efforts were tried along the years [14]–[16], however failing to match an ultimate solution to the development of a general, simple, accurate and scalable approach to device modeling.

Undoubtedly kernel-based machine learning regression can be seen as a promising candidate for the above modeling problem [17], [18]. The linear model structure adopted by kernel regressions has the key advantage of radically simplifying the training phase when a “relatively small” set of training data is used, compared to the more flexible ANN structures [17], [19], [20].

In this paper, the kernel ridge regression (KRR) is used for the identification of the dynamic nonlinear characteristic of a single-ended IC buffer, offering a first preliminary study on the feasibility and strengths of this alternate approach. Emphasis is given on model generation through a simple behavioral procedure based on the observation of the IC transient responses during normal operation of devices.



state-of-the-art kernel functions such as the polynomial kernel, since it has shown superior performance in several realistic complex regression problems (see as an example the results in [22]). The effectiveness of alternative kernel functions will be considered in future research.

It is important to remark that even if the training of the NARX model is carried out by considering the static map in (3), the resulting model obtained from the KRR in (4) is evaluated as a recurrent model.

#### IV. RESULTS

The results in this section are aimed at verifying the feasibility of the proposed approach, also stressing its overall benefits in terms of model accuracy. The considered test case is a plain CMOS driver composed of four cascaded stages which has demonstrated to be representative for the typical rich nonlinear dynamical behavior of this class of circuits.

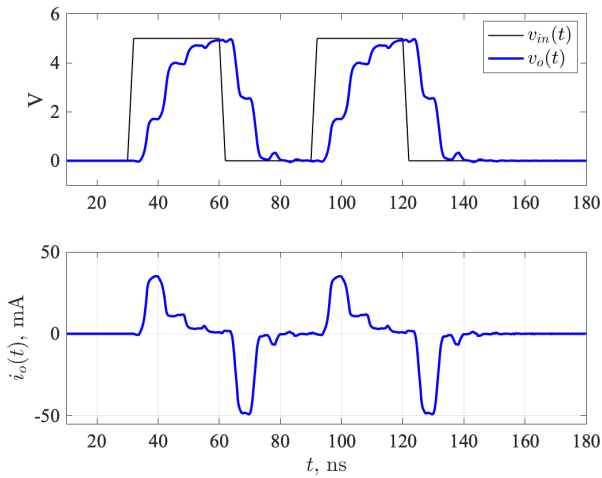


Fig. 2. Test waveforms: transient responses of the example device driven by a “010100” bit stream and loaded by an interconnect with  $Z_0 = 50\Omega$  characteristic impedance and  $T_d = 3$  ns delay.

Figure 2 shows the output port voltage  $v_o(t)$  and current  $i_o(t)$  responses of the example driver for a typical distributed load defined by a mismatched interconnect. The device is driven by a “010100” bitstream forced by a trapezoidal input signal  $v_{in}(t)$ . The sampled output port current response is assumed as the reference sequence for model testing (i.e., validation).

Figure 3 shows, for the same logic activity “010100” of the driver, the output port current and voltage responses observed for three different loads. In the figure, the paired voltage and current responses are labeled as set #1, #2 and #3. Two lumped loads and one distributed interconnect with characteristics different from the one considered for model testing are considered.

A first experiment is carried out by generating a KRR-based model built via the procedure outlined in Sec. III and by considering one set of training waveforms only (i.e. set #1 in this case). Figure 4 compares the reference output port current

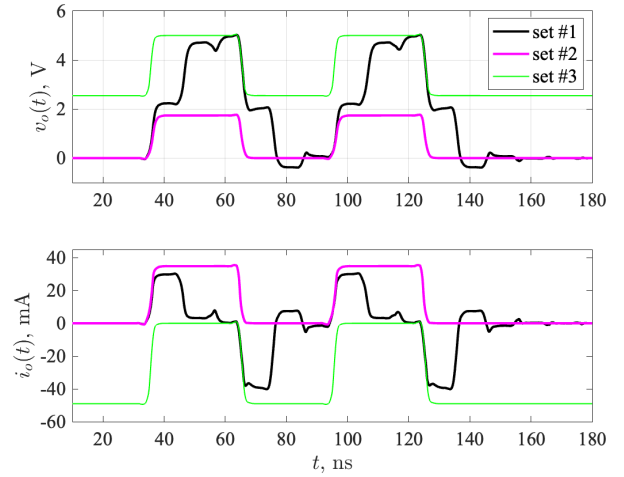


Fig. 3. Training waveforms: transient responses of the example device loaded by three different distributed or lumped loads different from the one considered for validation. Set #1: transmission line with  $Z_0 = 75\Omega$  and  $T_d = 5$  ns; set #2: shunt connection between a  $50\Omega$  resistor and a  $10$  pF capacitor; set #3:  $50\Omega$  in series with the power supply battery

waveform to either the static mapping or the recurrent response obtained by the estimated KRR model, highlighting that a qualitative signature of the current response is captured only. One single dynamical load appeared not sufficient to allow the generalization of the KRR regression to obtain accurate results. The positive aspect is the nearly overlapped responses of the static mapping and the recurrent KRR prediction.

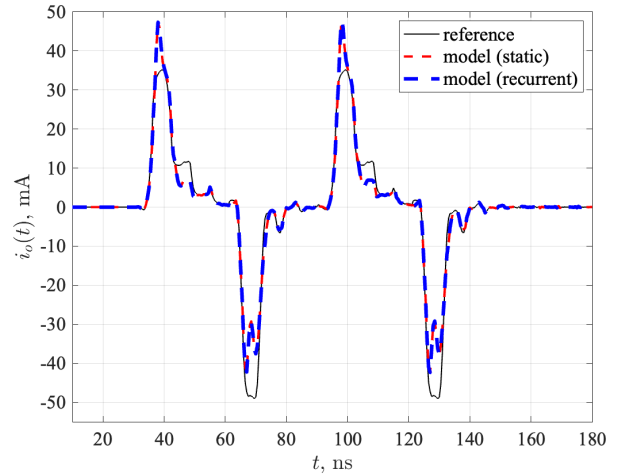


Fig. 4. Model validation (*single training sequence*): comparison between the reference output current of the test set shown in Fig. 2 and the model prediction obtained by both the static and the recurrent versions of the proposed machine learning regression. The training responses labeled as set#1 in Fig. 3 are used for the model generation.

A second experiment is instead carried out by generating a model with a procedure which uses all the three sets of device responses of Fig. 3, yielding a major improvement on model accuracy, as can be appreciated in the comparison of Fig. 5.

This additional test confirms the potential of the proposed method in matching a very good accuracy of models. KRR regressions allows to implement a simple modeling procedure. Also, the time required by model estimation is limited and it does not introduce critical practical aspects. The training time on a MacBook Pro (M1, 2022) is on the order of dozens of seconds (104 s for the latter test).

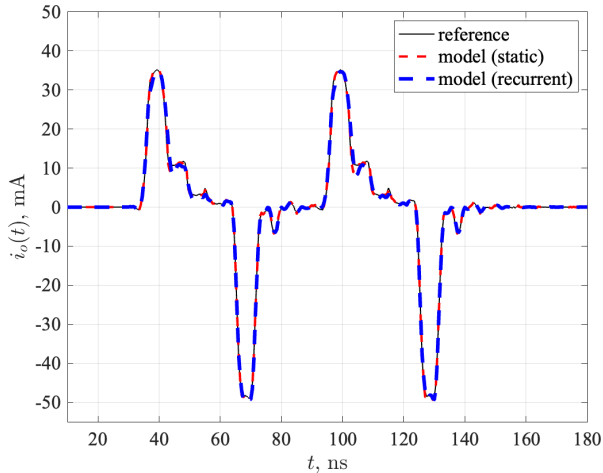


Fig. 5. Model validation (*multiple training sequences*): comparison between the reference output current of the test set shown in Fig. 2 and the model prediction obtained by both the static and the recurrent versions of the proposed machine learning regression. All the three training responses in Fig. 3 are used for the model generation.

## V. CONCLUSIONS & FUTURE WORK

This paper investigates the effectiveness of an alternative approach for the modeling of IC buffers based on the KRR. Specifically, the KRR is used to learn the static map provided by a NARX model approximating the actual nonlinear dynamic characteristic of a digital IC driver. The regression model is trained by considering the observations of voltages and currents at the device ports for different load conditions defined with the aim of exploring the possible operating conditions of the device. The resulting model can be then evaluated as a recurrent model. The overall model accuracy has been assessed by considering a new load configuration (i.e., different from the load used during the training phase) by comparing the model predictions with the corresponding results obtained by SPICE. The results highlighted the excellent accuracy of the proposed model. On the other hand, additional research work has to be carried out to assess the effectiveness of the presented modeling framework on different structures (e.g., differential IC drivers and/or the inclusion of the power supply effects), as well as the possibility of integrating the resulting model in a SPICE-like solver.

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