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Speculative High-Level Synthesis of RISC-V Processors

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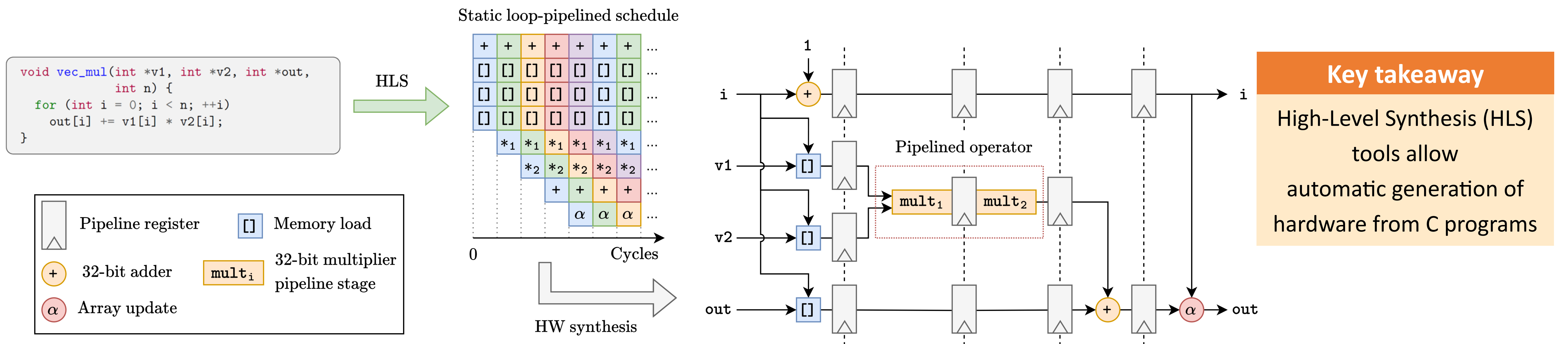
Designing a RISC-V CPU *should* be as simple as writing an Instruction Set Simulator

Introduction

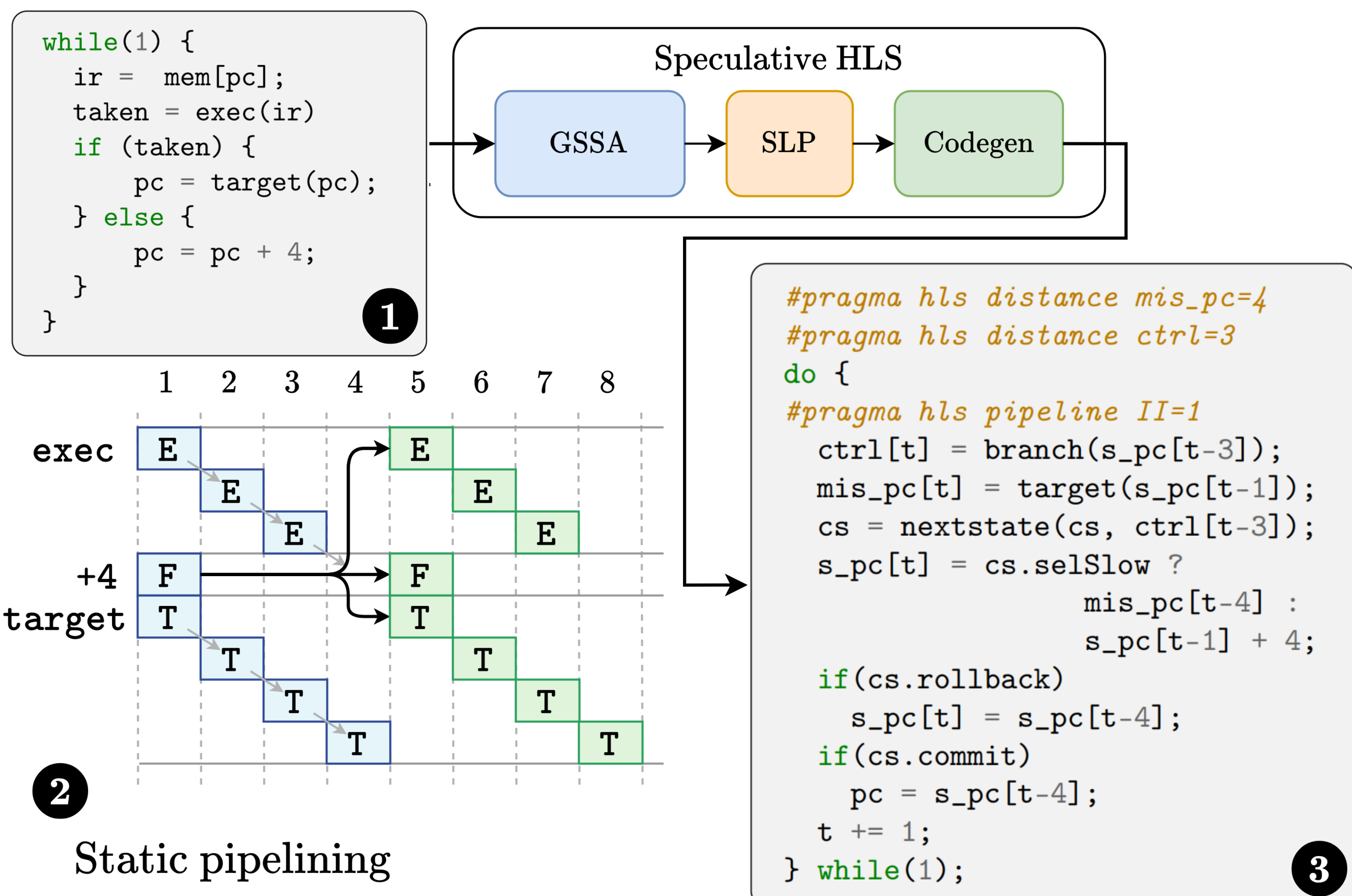
Context: Increasing need for customizable architectures for embedded applications.

Problem: Micro-architectural design is tedious and error-prone, how do we make such customizations available to everyone?

Our approach: Leverage High-Level Synthesis to **synthesize micro-architectures** from a single instruction set simulator in C.

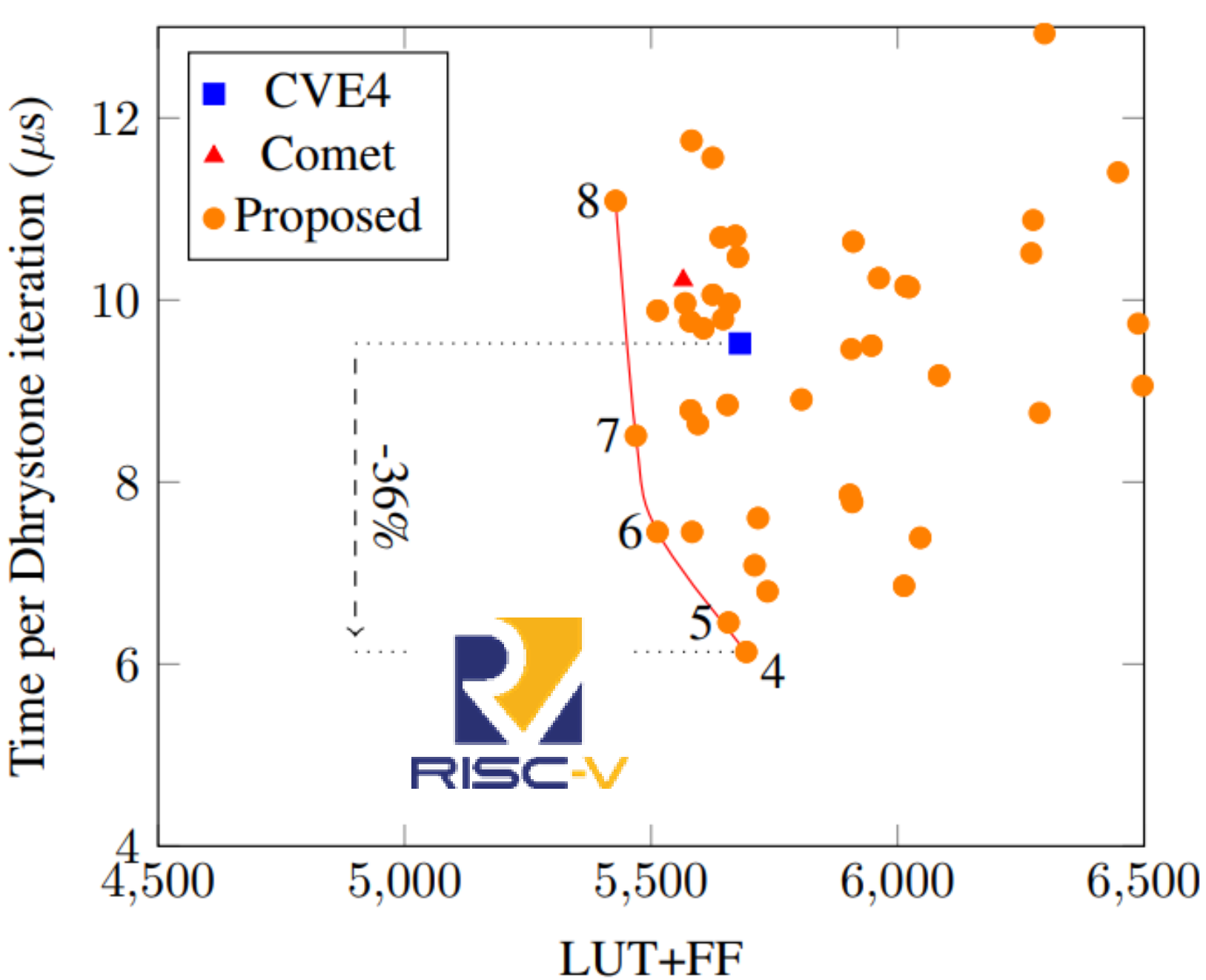


From ISS to RISC-V Processors



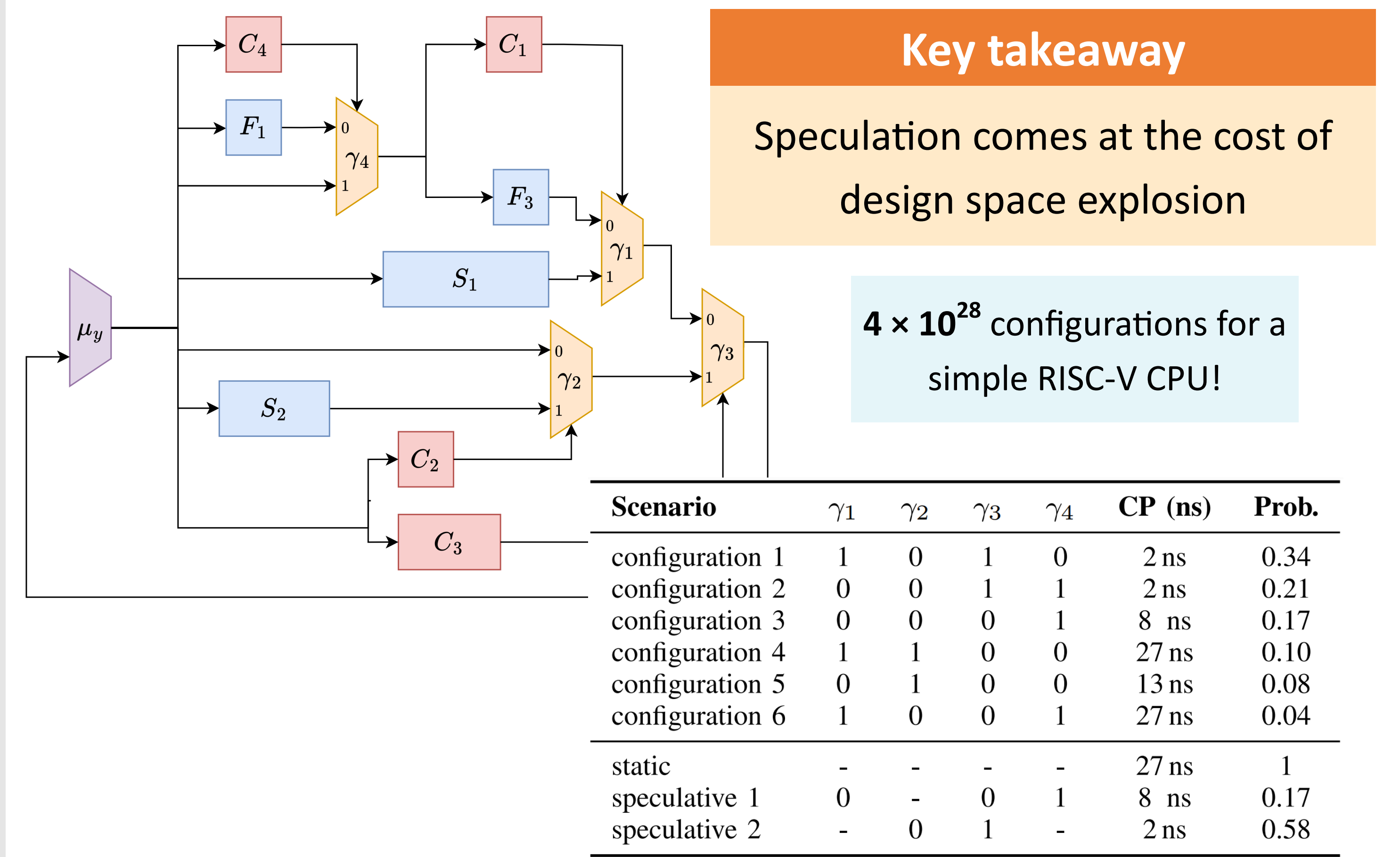
SpecHLS [1]

- Speculative HLS toolchain
- Backend-agnostic automatic transformation



Key takeaway
Synthesizing RISC-V CPUs is possible [2], but time-consuming!

Efficient Design Space Exploration

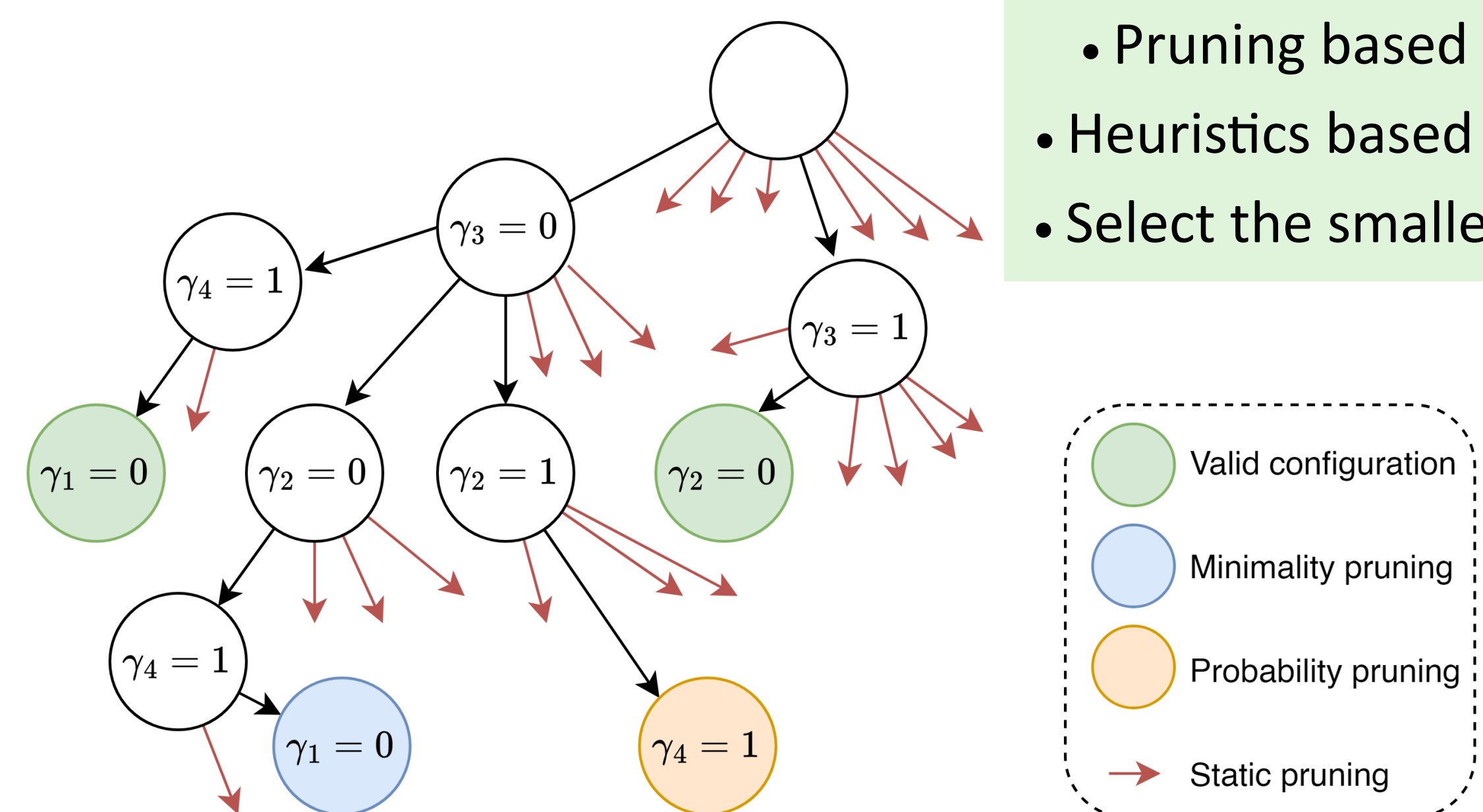


Exploring speculation opportunities

- Proposed algorithm based on Branch-and-Bound approach [3]
- Design space exploration leveraging *intertwined speculations* to obtain the best designs

Pruning configurations

- Pruning based on probability
- Heuristics based on achievable II
- Select the smallest configuration



Conclusion

- We need speculation to synthesize processor cores [2, 4].
- Processor design from an ISS using **speculative pipelining** enables **fast iteration times** and **intuitive** design exploration.

References

- [1] Gorius, J.-M., Rokicki, S., and Derrien, S. (2022). *SpecHLS: Speculative Accelerator Design using High-Level Synthesis*. IEEE MICRO.
- [2] Gorius, J.-M., Rokicki, S., and Derrien, S. (2022). *Design Exploration of RISC-V Soft-Cores through Speculative High-Level Synthesis*. ICFPT'22.
- [3] Leothaud, D., Gorius, J.-M., Rokicki, S., and Derrien, S. (2024). *Efficient Design Space Exploration for Dynamic and Speculative High-Level Synthesis*. FPL'24.
- [4] Derrien, S., Marty, T., Rokicki, S., and Yuki, T. (2020). *Toward speculative loop pipelining for high-level synthesis*. TCAD.