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Real-Time SER Measurements of CMOS Bulk 40 nm and 65 nm SRAMs Combined with Neutron Spectrometry at the JET Tokamak during D-D and D-T Plasma Operation

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Abstract — We performed SER characterization of decananometer SRAMs combined with neutron spectrometry in the deuterium-tritium-fueled JET tokamak, demonstrating the impact of machine operation on the reliability of electronics in conditions approaching those of future fusion reactors.

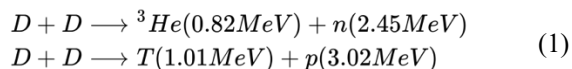
Keywords— CMOS, deuterium–tritium (D-T), fusion, neutron, real-time experiment, single event effects (SEE), soft-error rate (SER), single-event upset (SEU), static random-access memory (SRAM), tokamak, JET, WEST, JT-60SA, DTT, STEP.

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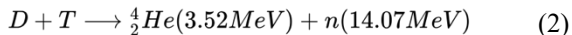
Real-Time SER Measurements of CMOS Bulk 40 nm and 65 nm SRAMs Combined with Neutron Spectrometry at the JET Tokamak during D-D and D-T Plasma Operation

I. INTRODUCTION

Controlled thermonuclear fusion is a promising energy source currently being investigated by many nations. The main current designs for controlled thermonuclear fusion reactors are based on magnetic confinement (tokamaks) and laser inertial confinement [1]. Both are fueled with deuterium (D) or a mixture of deuterium and tritium (T). A fusion reactor fueled with pure deuterium produces 2.45 MeV neutrons from one of the following two main reactions, which have equal probability of occurrence:



A fusion reactor fueled with a mixture of deuterium and tritium produces 14.07 MeV neutrons after the main reaction:



In both cases, individual neutrons coming from the plasma and reaching an electronic circuit after passing through shielding can interact instantaneously with the constituent materials of a discrete semiconductor device or those of an integrated circuit. They can produce a wide range of single event effects (SEEs), such as single event upsets (SEUs), single event functional interrupts (SEFIs) or single event hard errors, including single event latchups (SELs), gate ruptures or burn-outs [2]. These SEEs can damage or destroy electronic devices or sensors, corrupt signals in digital circuits, corrupt data or programs in memories, microprocessors, microcontrollers, FPGAs, etc. Note that in the field of high-energy physics and particle physics, modern accelerators may face a similar problem. For example, in the Large Hadron Collider (LHC) at CERN, electronics are exposed to thermal neutrons and intermediate-energy neutrons (defined up to 20 MeV), which are close to the energies of fusion-induced neutrons but with different energy distributions (harsher spectra, up to GeV of energies), causing SEEs that can affect machine availability [3,4].

In the context of the intense neutron fields produced by future fusion power reactors, the transport of the fields outside the reaction chamber and their impact on the reliability of the machine electronics distributed in the facility building (for command, control, and diagnostics) must be anticipated and carefully evaluated to ensure machine operation, long-term dependability, and safety of the installation, for the protection of the investment and people involved. This has motivated the first exploration studies of neutron-induced SEUs on

electronics in existing fusion devices, in anticipation of more advanced demonstration machines such as JT-60SA, DTT or STEP, such as those we have carried out in recent years on the W-Tungsten Environment in Steady-state Tokamak (WEST) [5,6] during the C5 [7,8] and C7 [9] campaigns with deuterium plasmas and, in the present work, on the Joint European Torus (JET) Tokamak during the very last D-D (C45) and D-T (C46) campaigns of the machine.

The JET tokamak is a fusion research machine located at the Culham campus for Fusion Energy in Oxfordshire, UK. It was commissioned in 1983 and is currently operated by the UKAEA to carry out the scientific program defined by EUROfusion consortium [10]. The machine has a major radius of 3 meters, and the D-shaped vacuum chamber is 2.5 m wide and 4.2 m high; the total plasma volume within it is 90 m³. At the time of its design in the 80's, it was the largest tokamak ever built. Between 2009 and 2011, JET was upgraded to adopt concepts being used in the development of the ITER experimental tokamak. In 2021, using D-T fuel, JET produced 59 megajoules of fusion energy during a five-second plasma pulse, beating its previous 1997 record of 21.7 megajoules [10, 11].

Using the same robust real-time (RT) 65 nm SRAM soft error rate (SER) test setup as in [7,9] (hereafter referred to as RTSER test bench) and the DIAMON (Direction-Aware Isotropic and Active Monitor) neutron spectrometer [12], as well as a 40 nm SRAM test setup extensively studied by CERN [4] (hereafter referred to as CERN test bench), this study at JET quantifies the effects of neutrons from a large tokamak operating with D-D and D-T plasmas on the SER of two different SRAM technologies (40 and 65 nm nodes) representative of modern integrated electronics. Contrary to our previous studies at WEST, and due to the intensity of the neutron fields generated by JET, the test benches were not placed directly in the experimental hall next to the machine, but in a partially radiation-shielded environment (in the basement of the JET tokamak building, under the reinforced concrete slab – thickness 1,045 mm – supporting the experimental chamber). In this sense, the study is even more relevant, since the error rates obtained are directly representative of the level of unreliability to be expected in areas of a tokamak building where a lot of electronic equipment or equipment housing electronics can be installed. In the remainder of this summary, after describing the configuration of the experiments, we report the bit flip distributions obtained for the two generations of SRAMs during the JET D-D and D-T campaigns, in direct relation to the neutron spectra measured during each individual plasma pulse at the same location as the tested memories. The implications of these results for future fusion devices are also discussed, as well as perspectives for future work.

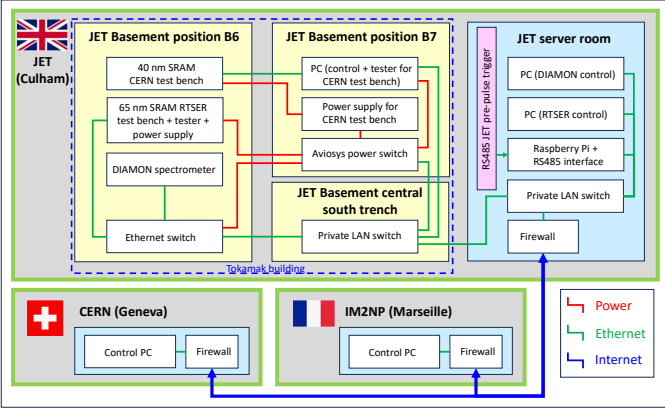


Fig. 1. General layout of the JET-SEE experiment.

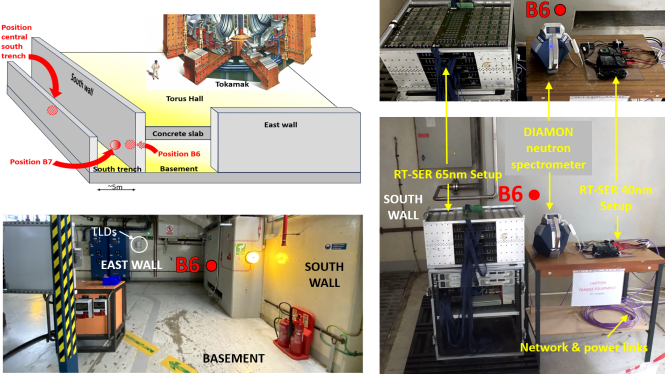


Fig. 2. Positions B6, B7 and the central south trench inside the JET tokamak building (top left), and installation of the test benches and of the DIAMON spectrometer in position B6.

II. EXPERIMENTAL DETAILS

Fig. 1 shows the general layout in which the RTSER and CERN test benches and the DIAMON spectrometer have been integrated to carry out these experiments at JET. Fig. 2 shows the positions B6 and B7 and the central southern trench in the JET tokamak building, and shows pictures of the complete setup in position B6. Position B6 was chosen because it provides a sufficiently high neutron flux during D-T plasma pulses to obtain good SEEs statistics on the RTSER and CERN test benches, while minimizing the risk of neutron-induced failures of the auxiliary equipment (tester, power supply, Ethernet switch) of the RTSER test bench and of the spectrometer. This position B6 is equipped with thermoluminescent dosimeters (TLD) for neutron fluence measurements, which will be used for the analysis of the neutron energy spectra measured with the DIAMON spectrometer. Position B7 in the south trench is separated from position B6 by the east concrete wall, which attenuates the neutron flux by a factor of approximately 100, thereby further reducing the risk of neutron-induced failure of the IC electronics installed in position B7.

For the interpretation of the experimental results, it is crucial to measure the local neutron flux and energy spectrum at the location of the tested electronic memories. For this purpose, we installed in position B6 in the immediate vicinity of the RTSER and CERN test benches a DIAMON spectrometer from RAYLAB [12], identical to that used during the SEE experiments in the WEST tokamak [7,8]. This spectrometer

was connected to a private local area network (LAN) via the Ethernet switch of the RTSER test bench to allow its control by a Raspberry Pi PC installed in the JET server room. This Raspberry Pi PC was equipped with an RS485 interface that received a JET pre-pulse trigger 30 seconds before the start of each plasma pulse. After receiving this trigger, the Raspberry Pi PC sends a request to the DIAMON spectrometer via the LAN to start a spectrum measurement and to stop it after a defined time (2 minutes) that is longer than the maximum plasma pulse duration (45 seconds) plus the countdown time (30 seconds) and shorter than the time between consecutive pulses (about 20 to 30 minutes).

During the SEE experiments at JET, the RTSER test bench was used in the same format as for the previous experiments at WEST (see details in [7,9]). We recall here that this setup contains a bank of 384 SRAM circuits fabricated in 65 nm CMOS bulk by STMicroelectronics using a boro-phospho-silicate-glass-free manufacturing process. Each memory circuit contains 8.5 Mbits of single-port SRAM (no deep N-well) with a bit cell area of $0.525 \mu\text{m}^2$, operating at a nominal core voltage of 1.2V. During measurements, the tester scans the entire memory map ($384 \times 8.5 \times 1024^2 = 3.422 \text{ Gb}$) once every 2.5 seconds [13].

The CERN test bench consists of two identical motherboards, each containing a 32 Mbit SRAM fabricated in 40 nm bulk CMOS by Integrated Silicon Solution Inc. (ISSI). The motherboards allow the memory to be written with an initial pattern (checkboard) and the SEUs to be read every 1 to 5 minutes. The ISSI SRAM was chosen for this experiment because of its large thermal neutron cross-section and high sensitivity in the range of 0.1-10 MeV compared to other memories. It has been well characterized in several facilities with neutrons, protons, and heavy ions, and specifically for these tests at JET, its response as a function of neutron energy is well known [14]. In addition, this memory has been modeled in FLUKA and the neutron SEU cross sections at different energies have been benchmarked to the measured values. One of the two setups (motherboard and memory) was completely shielded with boron carbide in order to record SEUs induced by non-thermal neutrons. The shielding consists of a flexible layer 0.5 cm thick composed of natural boron for 80% of its weight and resulted in an efficient absorption of neutrons below 1 eV [15]. The two motherboards were connected to a power supply and a control PC which were installed in B7 to reduce the risk of neutron-induced failure.

The RTSER memory bank and its auxiliaries (tester, power supply and Ethernet switch), as well as the CERN test bench power supply and control PC, were powered by an Aviosys power switch to allow remote launch of an OFF/ON cycle in the event of a malfunction. This power switch was installed in position B7 to reduce the risk of neutron-induced malfunctions.

The RTSER tester and power supply were connected to the private LAN via the Ethernet switch to allow their control from a PC installed in the JET server room. The CERN test bench control PC and the Aviosys power switch were also connected to this private LAN. This private LAN was connected to the JET firewall to allow the control of all the equipment connected to it and the downloading of the experimental data recorded by the CERN and RTSER test benches and by the DIAMON spectrometer, via the Internet, from the CERN premises in Switzerland and from the IM2NP premises in France.

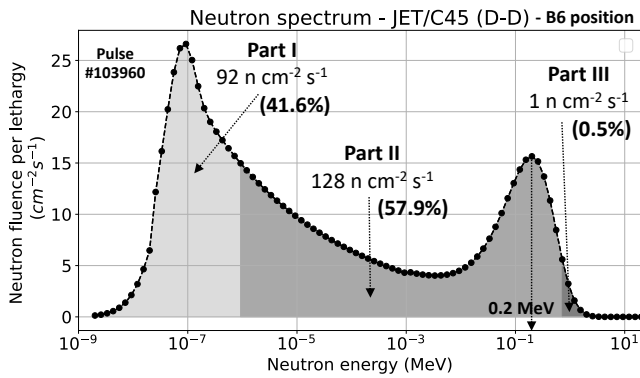


Fig. 3. Neutron energy spectrum measured by DIAMON at the device level during the C45 campaign and corresponding to the D-D plasma pulse #103960.

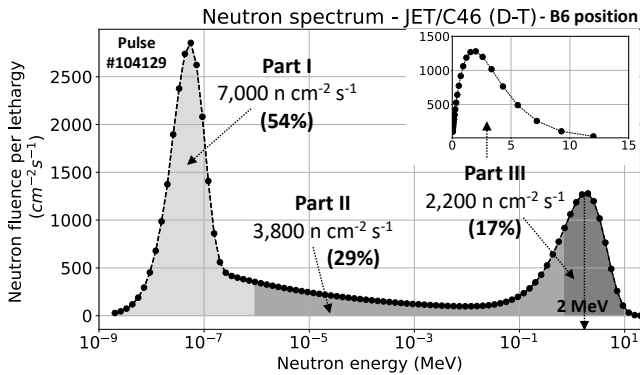


Figure 4. Same legend as figure 3, but for the C46 campaign (D-T plasma pulse #1034129).

III. EXPERIMENTAL RESULTS

Figures 3 and 4 show two examples of neutron energy spectra measured by DIAMON at position B6 during C45 (D-D plasma, pulse #103960) and C46 (D-T plasma, pulse #104129). As usual for the atmospheric spectrum, we report the fluence in three energy regions: Part I ($E < 10^{-6}$ MeV), Part II (10^{-6} MeV $< E < 1$ MeV) and Part III ($E > 1$ MeV). These spectra result from the degradation of the initial neutron energy (2.45 MeV for D-D plasma pulses and 14.07 MeV for D-T plasma pulses) by the shielding they passed through (mainly the concrete ceiling slab of the basement of the tokamak building) before arriving at position B6, where a large part of them was thermalized by bouncing off the concrete walls, floor and ceiling of B6. The spectrum of the D-T plasma pulse (#104129) shows a peak at an energy (2 MeV) ten times higher than the peak (at 0.2 MeV) present in the spectrum of the D-D plasma pulse (#103960), and a fluence in region III about 30 times higher than in the spectrum of pulse #103960. It also has a higher fluence in region I (thermal neutrons).

Figures 5 and 6 show the distribution of the number of neutrons produced per pulse as a function of pulse duration for the C45 and C46 campaigns. Pulses with one or more coincident SEUs detected by the RTSER 65 nm setup are colored red. As expected, SEUs occur mainly during the pulses that produced the largest number of neutrons. During C45, almost all SEUs occurred during pulses that produced more than 10^{16} neutrons. During C46, virtually all pulses producing more than 10^{17} neutrons induced SEUs.

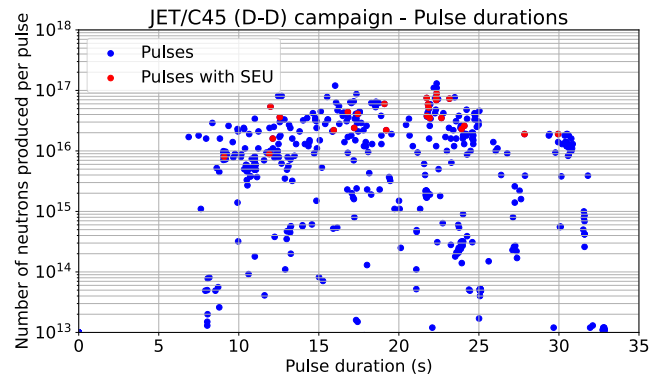


Fig. 5. Number of neutrons per machine pulse vs. pulse duration during the JET C45 campaign (D-D plasma). Pulses with one or more coincident SEUs are colored red.

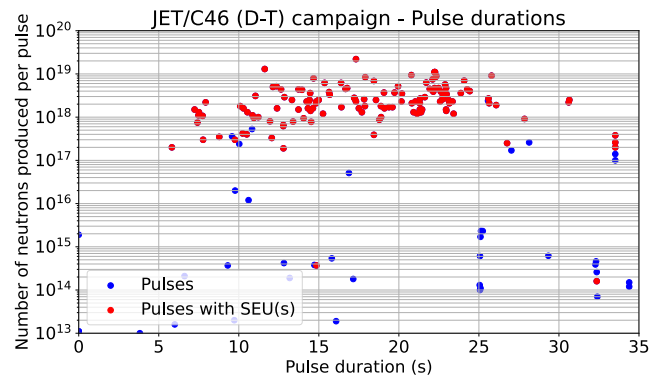


Fig. 6. Same legend as figure 5, but for the C46 campaign (D-T plasma).

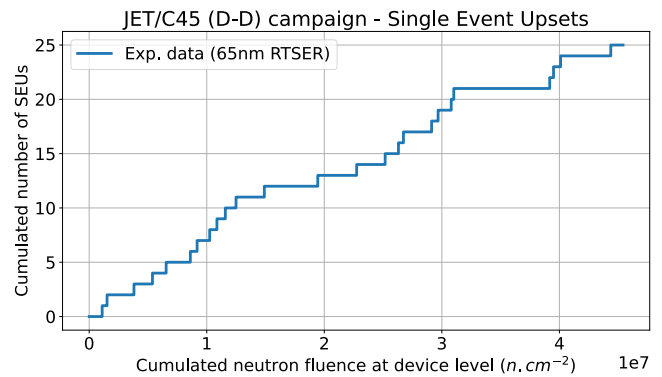


Fig. 7. Single event upset distribution (65nm RTSER) as a function of the cumulated neutron fluence at device level for all the events detected during the C45 campaign (D-D plasma).

For C46, the pulses with SEUs are more often long pulses than short pulses (64% of the pulses with SEUs have a duration longer than the average, which is 18.6 s). This preliminary result will be discussed in the final paper in relation to the analysis reported in [9] of the effect of tritium production during long D-D plasma pulses on the SER and the rate of MCUs.

Figure 7 shows the accumulation of SEUs recorded by the RTSER test bench as a function of the cumulative fluence during the C45 campaign. A total of 25 events were recorded for a cumulative fluence of 4×10^7 n/cm². These 25 SEUs correspond to 23 single bit upsets (SBUs), 1 multiple cell upset of multiplicity 2 (MCU(2)) and 1 MCU(3).

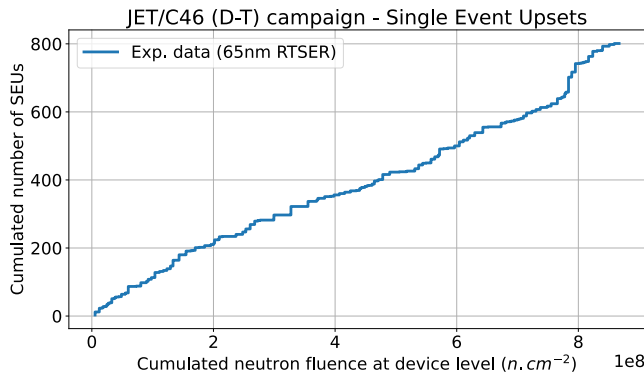


Fig. 8. Same legend as figure 7, but for the C46 campaign (D-T plasma).

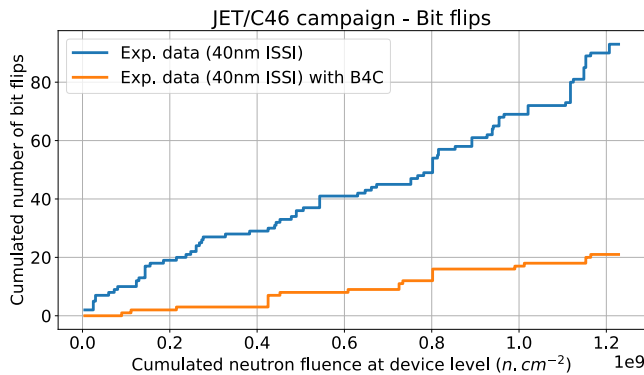


Fig. 9. Bit flip distributions (CERN test bench) as a function of the cumulated neutron fluence at the device level for all the events detected on the two motherboards (one bare, the other covered with B4C) during the C46 campaign (D-T plasma).

Figures 8 and 9 show the accumulation of SEUs and bit flips on the RTSER and CERN test benches as a function of the cumulative fluence during the C46 campaign, respectively. For the 65nm SRAM, a total of 802 SEUs were recorded by the RTSER test bench for a cumulative fluence of 8.7×10^8 n/cm². These events include 685 SBUs, 77 MCU(2), 36 MCU(3), 2 MCU(4), 1 MCU(6) and 1 MCU(9). For the 40 nm SRAM, 114 bit flips (including 21 due to non-thermal neutrons and 93 due to neutrons of the full spectrum) were recorded by the CERN test bench for a cumulative fluence of 1.2×10^9 n/cm². The RTSER test bench recorded a lower cumulative fluence than the CERN test bench because it suffered a period of unavailability during C46. The blue graphs in Figs. 8 and 9 both show an accelerated growth in the accumulation of bit-flips just before the end of the C46 campaign, which will be discussed during the detailed analysis of the experimental results, taking into account the evolution of the neutron energy spectra during C46 and just before the end of C46. The final paper will also report and discuss the size and time distributions of SBUs and MCUs for both experiments versus the characteristics of machine pulses. We will focus in particular on the pulses with the highest number of SEUs, as shown in Fig. 10. For the 65 nm SRAM for example, we recorded up to 44 SEUs (40 SBUs, 3 MCU(2) and 1 MCU(3)) during the pulse that produced the largest number of neutrons during the C46 campaign (pulse #104675, duration of 17.3 s, total of 2.2×10^{19} neutrons). These results, and their predictions for longer pulses and larger reactors, clearly pose a reliability challenge for the electronics in the tokamak building.

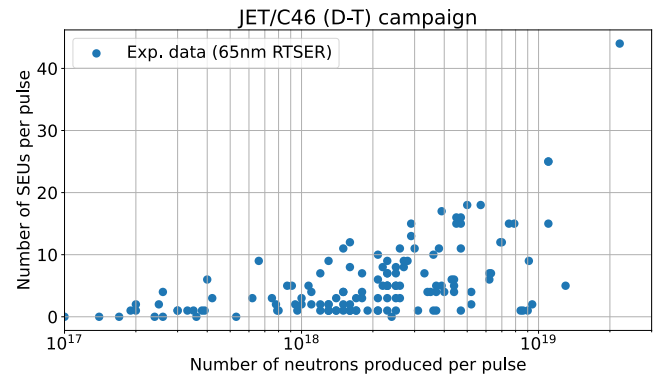


Fig. 10. Number of SEUs per pulse versus the total number of neutrons produced per pulses during the C46 campaign (D-T plasma).

In conclusion, this study, like the previous ones conducted at the WEST tokamak and other facilities [7,8,9], is part of a larger detailed multi-year study that has begun in 2020 and continue for several years. This global effort will enable us to provide the necessary input data for the design of shielded areas that will ensure a neutron environment fully compatible with the operation of commercial off-the-shelf (COTS) electronic systems without the need for neutron SEE qualification.

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