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### ► To cite this version:

Raphaël Dawant, Matthieu Gaudreau, Marc-Antoine Roy, Pierre-Antoine Mouny, Matthieu Valdenaire, et al.. Damascene versus subtractive line CMP process for resistive memory crossbars BEOL integration. *Micro and Nano Engineering*, 2024, 23, pp.100251. 10.1016/j.mne.2024.100251 . hal-04607951

**HAL Id: hal-04607951**

**<https://hal.science/hal-04607951>**

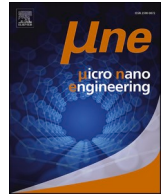
Submitted on 11 Jun 2024

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## Damascene versus subtractive line CMP process for resistive memory crossbars BEOL integration

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### ARTICLE INFO

#### Keywords:

CMP  
Resistive memory  
Crossbar array  
Damascene  
Subtractive line  
BEOL  
Integration

### ABSTRACT

In recent years, resistive memories have emerged as a pivotal advancement in the realm of electronics, offering numerous advantages in terms of energy efficiency, scalability, and non-volatility [1]. Characterized by their unique resistive switching behavior, these memories are well-suited for a variety of applications, ranging from high-density data storage to neuromorphic computing [2]. Their potential is further enhanced by their compatibility with advanced semiconductor processes, enabling seamless integration into modern electronic circuits [3]. A particularly promising avenue for resistive memory lies in its integration at the Back-End-of-Line (BEOL) stage of semiconductor manufacturing [4]. BEOL integration involves processes that occur after the fabrication of the transistors, primarily focusing on creating interconnections that electrically link these transistors. Integrating resistive memories at this stage can lead to compact, efficient, and high-performance architectures, pivotal for in-memory computing applications where data storage and processing are co-located [5]. This paper studies three ways to integrate TiO<sub>x</sub>-based resistive memory into passive crossbar array structures, using chemical mechanical polishing (CMP) processes, focusing on identifying the optimal integration techniques.

### 1. Introduction

In recent years, resistive memories (ReRAM) have emerged as indispensable components for mixed-signal circuits, pivotal for executing vector-by-matrix multiplication (VMM) in artificial neural networks [1]. 1T1R memory arrays, combining a resistive switching element (1R) with a transistor (1T), have been widely studied and demonstrated breakthroughs in broad implementation of neuromorphic computing [4–6]. Yet, the technology is constrained by its cell size and the high conductance of devices, necessitating the use of large, energy-demanding peripheral circuits and challenging the drive towards miniaturization and improved energy efficiency [7]. In contrast, passive ReRAM circuits offer a substantial density advantage when integrated monolithically in the Back-End-of-Line (BEOL) [3]. In a  $n \times n$  passive ReRAM array, due to the smaller footprint of the ReRAM in the BEOL compared to transistors located in the Front-End-of-Line (FEOL), the

footprint of the  $2n$  transistors, necessary for addressing  $n^2$  ReRAM, often surpasses the footprint of the memory elements themselves in passive configurations [2]. Even for larger arrays where the total area of  $2n$  transistors becomes lower than that of the  $n^2$  memory array, ReRAM arrays can utilize the inherent potential for 3D integration provided by the BEOL process. In 1T1R configurations, the footprint is primarily constrained by the transistor size. However, in passive arrays, challenges arise from the density of memory elements and the interconnections that form the circuit, referred to as a crossbar array. Consequently, there is significant interest in developing dense crossbar memory array structures that can be fabricated at the BEOL level to enhance the massive advantage of passive circuits. Inspired by the technique used to fabricate the CMOS interconnections, this paper aims to study different approaches to integrate crossbar arrays in the BEOL and enhance the 3D integration.

Main process flow used for BEOL interconnects: (e) Subtractive Al

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interconnect fabrication with IDL planarization [8]. (f) Cu Dual Damascene interconnect based on metal polishing [9]. (g) Ru interconnect combined with Semi-Damascene process [10] and (h) TopVia Subtractive Ru interconnect [11].

As shown in Fig. 1(a), passive ReRAM circuits consist of metallic crossbar electrodes arrayed with a switching memory located at the intersection of each electrode (see Fig. 1(b)). This circuit can perform direct VMM by taking advantage of Ohm's and Kirchhoff's laws. The ReRAM used as the switching element are devices composed of a metal-insulator-metal (MIM) junction, as illustrated in Fig. 1(c). As shown in Fig. 1(d), applying a positive or negative voltage to the MIM junction can lead to the migration of ions in the insulating layer, creating a change in the junction's resistance. Different integration schemes for the MIM junction are compatible with the CMOS production lines and support a high interconnection density. Traditional methods, such as subtractive aluminum (Al) interconnects, shown in Fig. 1(e), involving Al line etching followed by interlayer dielectric (ILD) deposition and planarization, have established precedents [8]. However, the copper (Cu) dual Damascene process, which entails etching vias and trenches in ILD before the metal deposition and CMP (see Fig. 1(f)), remains the standard approach for advanced nodes [9]. Other innovative proposals for advanced CMOS nodes include subtractive metal line techniques complemented by semi-Damascene processes, as shown in Fig. 1(g) [10], and the TopVia subtractive method (see Fig. 1(h)) [11]. All of these proposals enable the creation of a planar V and metal line block that can be repeated multiple times. Based on these integration strategies, two primary categories can be distinguished by the method employed to level the surface: the Damascene approach, characterized by the polishing of the metal, and the subtractive method, where the dielectric is

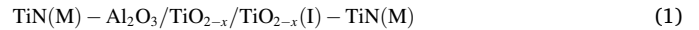
polished. The next section presents different integration schemes that use these techniques to fabricate crossbar arrays and assesses their practicality for BEOL integration.

## 2. Fabrication process

We developed three integration schemes to fabricate passive resistive memory crossbar arrays: a Damascene approach (a), a single-subtractive approach (b), and a double-subtractive approach (c). Fig. 2 shows the process flow of the three fabrication approaches. The Damascene (a) and subtractive approaches (b–c) are distinguished by the planarization method used. The differences between the single (b) and double-subtractive approaches (c) come from the patterning of the TiO<sub>x</sub>/Ti switching layers (SL). In the single-subtractive approach, the SL is patterned and etched a single time with the top electrode (TE). In the double-subtractive process, the SL is patterned and etched a first time with the bottom electrode (BE) and a second time during the patterning of the TE, which results in the patterning of the SL only at the intersection of each electrode without adding another lithography mask.

### 2.1. Process flow

For all the integration schemes tested, the MIM junction is composed of:



The selected switching stack was chosen for its analog properties, demonstrating multi-bit precision in prior studies [12–14], and its proven applicability for VMM operations in passive ReRAM crossbar

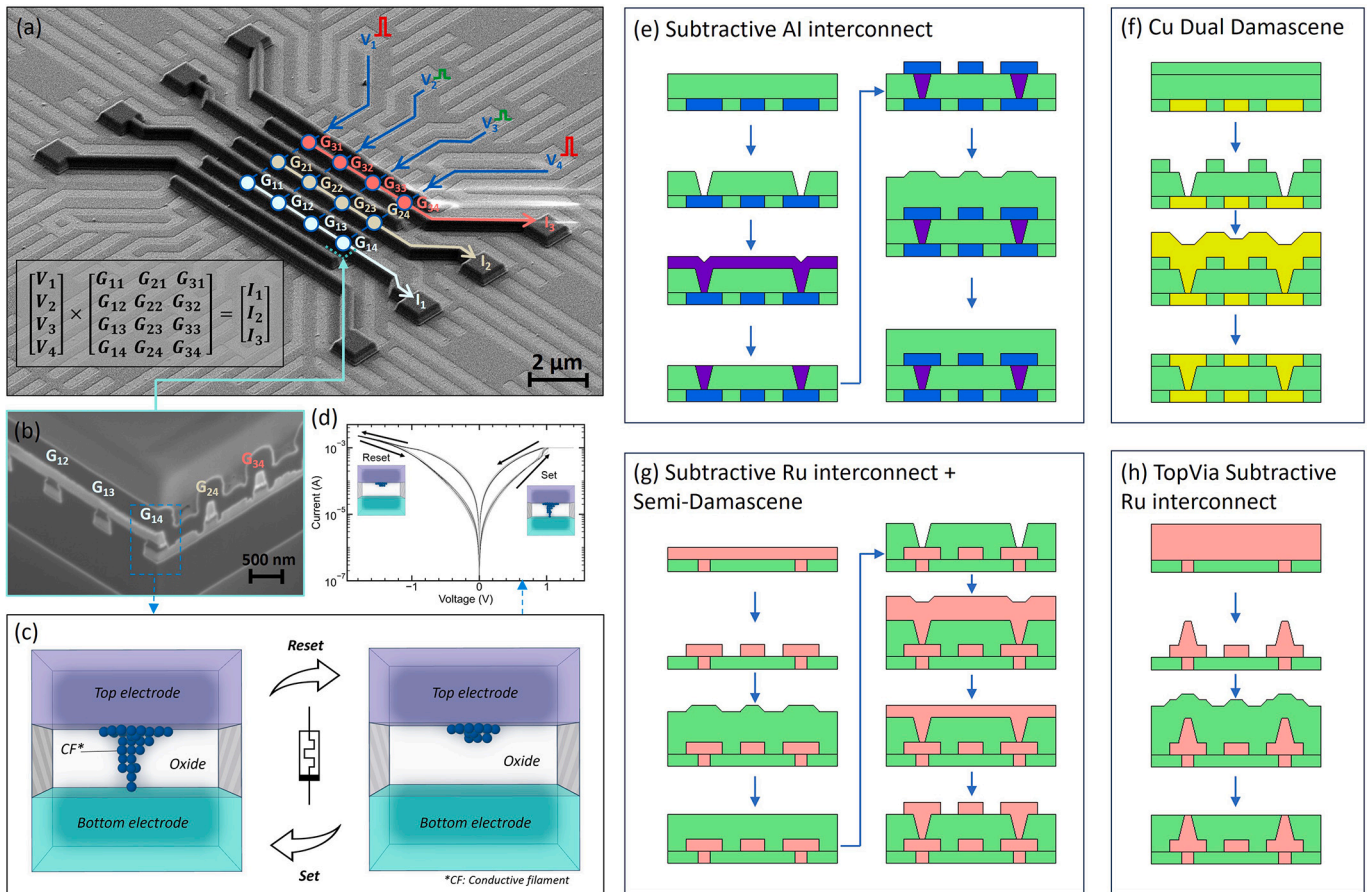
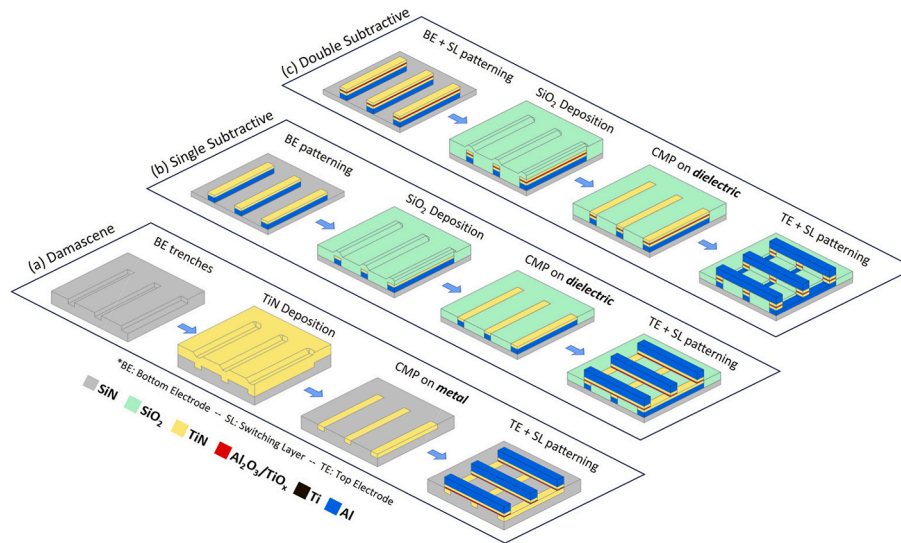


Fig. 1. (a) SEM image of a crossbar array illustrating the use of resistive memory for dense in-memory computing, with (b) a FIB cross-section showing the MIM capacitance of the memory. (c) Diagram of the MIM junction depicting ion migration that enables switching between 'Set' and 'Reset' states in resistive memories, and (d) the current-voltage graph displaying the switching behavior.



**Fig. 2.** Process flow for the three approaches: (a) Damascene: BEs are etched in the SiN substrate. A 600-nm TiN layer is sputtered and polished by CMP. The switching stack (Al<sub>2</sub>O<sub>3</sub>/TiO<sub>2-x</sub>/Ti/TiN) is deposited followed by the deposition of the Al TE. The SL and the TE are patterned. (b) Single Subtractive: Patterning of Al/TiN BEs, A 600-nm SiO<sub>2</sub> layer is deposited and planarized via CMP. Subsequent steps are as in the Damascene approach. (c) Double Subtractive: Follows the initial steps of the single-subtractive method, but after Al/TiN BEs deposition, the SL is added immediately. BEs and SL are defined. SiO<sub>2</sub> deposition and CMP follow, with TE deposition and patterning. During this step, a second etching of the SL at electrode intersections concludes the process.

[7,15].

The TiN metallic layers are at least 30 nm thick to prevent oxygen diffusion from the insulator stack inside the potential Al metallic contact electrodes. The insulator part of the MIM junction is a switching stack of Al<sub>2</sub>O<sub>3</sub> (1.4 nm) deposited via atomic layer deposition, and TiO<sub>2-x</sub> (30 nm) deposited by reactive sputtering, along with Ti (10 nm)/TiN (30–70 nm). The vacuum was not broken between the deposition of the TiO<sub>2-x</sub>, Ti, and TiN layers. The stoichiometry of TiO<sub>2-x</sub> was tuned by controlling the reactive sputtering regime and the oxidation state of the target as described in a previous study [16]. With this process, we did demonstrate stable state retention at room temperature [16].

### 2.1.1. Damascene

For the Damascene approach, illustrated in Fig. 2(a), BEs were defined by electron beam lithography and patterned using inductively coupled plasma (ICP) etching within SiN to a depth of 150 nm. A 600 nm thick TiN metallic layer was deposited by sputtering and polished by CMP until the excess metal between electrodes was removed. The switching stack was deposited with 30 nm of TiN followed by the TEs of Al, 200 nm thick, by evaporation. The switching stack and the TEs were patterned using electron beam lithography (EBPG5200) and ICP etching with BCl<sub>3</sub>/Cl<sub>2</sub>/Ar chemistry.

### 2.1.2. Single subtractive

For the single-subtractive approach, shown in Fig. 2(b), a metallic stack of Al/TiN BEs with a corresponding thickness of 150/70 nm was deposited by sputtering. The BEs were defined by electron-beam lithography and patterned by ICP etching using BCl<sub>3</sub>/Cl<sub>2</sub>/Ar chemistry. A 600 nm thick SiO<sub>2</sub> layer was deposited by PECVD and planarized via CMP. The overburden was removed until the metal electrodes were revealed. For the remainder of the process, the fabrication steps were the same as the Damascene approach. The switching stack was deposited with the 200 nm Al TE in the same way as explained in the Damascene approaches, then patterned using electron beam lithography and ICP etching with BCl<sub>3</sub>/Cl<sub>2</sub>/Ar chemistry.

### 2.1.3. Double subtractive

For the double-subtractive approach, the metallic stack of Al/TiN BEs deposition is directly followed by the deposition of the SL using the same deposition techniques as presented for the previous approach but

with a thicker top TiN layer of 70 nm. The BEs and the SL were defined by electron-beam lithography and patterned by ICP etching using BCl<sub>3</sub>/Cl<sub>2</sub>/Ar chemistry. A 600 nm thick SiO<sub>2</sub> layer was deposited by PECVD and planarized via CMP until the metal electrodes were visible. The same CMP recipe as the single-subtractive approach was used. TEs of Al, 200 nm thick, were then deposited by evaporation. The TEs were patterned using electron beam lithography and ICP etching with BCl<sub>3</sub>/Cl<sub>2</sub>/Ar chemistry as in the previous approaches but this was directly followed by a second etching of the SL using the mask of the TE. This results in the self-aligned patterning of the SL only at the intersection of each electrode, as shown in Fig. 2(c).

### 2.2. CMP development

CMP is a critical step to obtain good planarity and enable the integration inside the planar levels of interconnections in the BEOL, as well as a 3D integration. It is a process that employs both chemical reactions and mechanical abrasion to remove materials to achieve a leveled surface. It requires the use of specific slurry solutions containing abrasive particles to control the rate of material removal and surface finish. Several factors influence the choice of the slurry: the material to be polished, the removal rates, and the selectivity between the different materials, among other parameters. In the case of the Damascene approach, high material removal rate (MRR) selectivity is desired between the TiN BE metal and the SiN substrate. On the other side, single and double-subtractive approaches require a good selectivity between the SiO<sub>2</sub> used to encapsulate the device and the TiN electrode. To address these requirements, we considered two types of slurries:

Silica-oxide-based slurries are usually used for the polishing of both SiO<sub>2</sub> and SiN but can also be used for the polishing of TiN with the addition of an oxidizing agent such as H<sub>2</sub>O<sub>2</sub> or NaClO. The detachment of the polished material is facilitated by mechanical contact between the particles and the sample. These slurries are generally basic to promote hydration reactions [17–19].

Cerium-dioxide-based slurries are typically used to polish oxides and stop on nitride materials. The particles are softer than silicon dioxide slurries. Abrasion occurs in two steps [20]: First, the cerium dioxide molecule attaches to the silicon oxide surface, and then, the mechanical contact between the pad and the sample removes it along with the oxide [19,21]. No literature has been found regarding the abrasion mode of

CeO<sub>2</sub> on TiN. Nevertheless, preliminary tests have shown potential for TiN polishing and will be studied in the next section. More details on the mechanism for both of these slurries can be found in Supplementary Data, Sections 1–2.

CMP processes are also highly dependent on the layout density, and a non-uniform layout can result in unwanted effects, such as erosion and dishing, which can negatively affect the planarization process. For these reasons, we used filling dummy structures to obtain a density of structures between 40%–60%, and large structures were stripped to limit the maximum dimension/spacing in the three approaches studied.

### 2.2.1. Metal polishing

The highest selectivity between TiN and SiN was achieved by the CeO<sub>2</sub>-based slurry with 1% H<sub>2</sub>O<sub>2</sub> (see Supplementary Data, Section 3). However, it has been demonstrated that CeO<sub>2</sub> slurry is ineffective in polishing topographic structures [22]. CeO<sub>2</sub> particles tend to agglomerate at the bottom of trenches [25], preventing mechanical contact with the pad required to remove the metal. In our tests, we observed that planarization was ineffective when the topography of the trenches was greater than 50 nm. For this reason, we used dummy structures below 500 nm, 150 nm depth trenches, and a 600 nm thick TiN layer. This results in a smoother surface that decreases the topography below 50 nm. Due to the good CeO<sub>2</sub> selectivity and the fact the filling structure matches the dimension of the electrode, erosion was reduced and planarity below 10 nm was achieved. This approach imposes strict design rules with a maximum dimension of 500 nm. Note that we were able to use SiO<sub>2</sub>-based slurry with micrometer dummy structures to planarize the surface and use CeO<sub>2</sub> to end the process, resulting in higher topography (see Supplementary Data, Section 4).

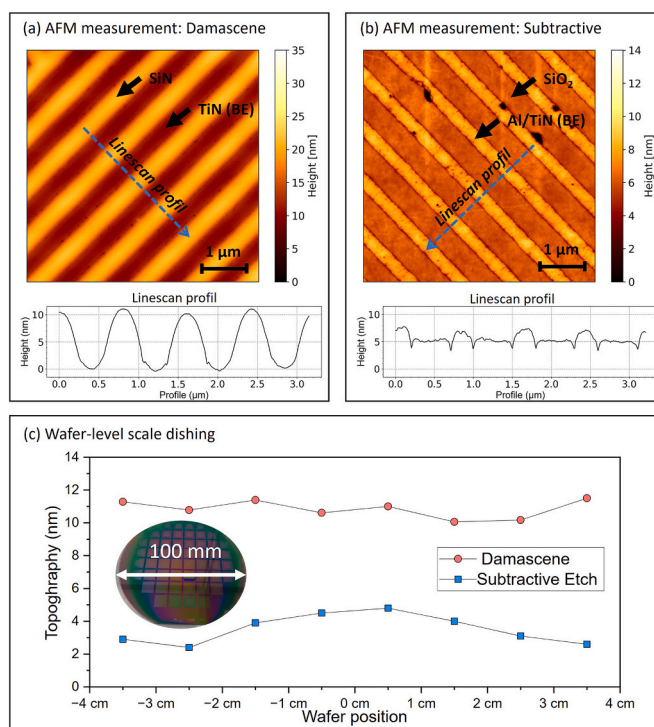
### 2.2.2. Dielectric polishing

The CMP is performed on SiO<sub>2</sub> for both the subtractive and double-subtractive approaches. Most processes for resistive memory passive crossbar array fabrication used similar approaches and revealed the bottom electrode by plasma etching [7]. Note that we tested planarizing the structure and revealing the structure by plasma etching but this approach yielded poor results (see Supplementary Data, Section 5). Nevertheless, similar to the top via subtractive interconnect [11], CMP can be used to reveal the bottom electrode. In this case, the TiN layer acted as the stop layer. The slurry with the highest SiO<sub>2</sub>/TiN selectivity considered in this study is a SiO<sub>2</sub>-based particle (50 nm) slurry without any additive. The selectivity for this process is close to 1 (0.95). Because both materials have almost the same MRR, the challenge is end-point detection (EPD). For this reason, we use a relatively thick TiN layer of 70 nm as a buffer. 30 nm thick TiN is required to be efficient as an oxygen barrier, meaning that 40 nm of TiN can be polished. The EPD could be enhanced by adding a SiN layer on top of the TiN electrode to function as a stop layer, similar to the STI process [26], with a CeO<sub>2</sub>-based slurry. The SiN on top of TiN could be selectively removed etching processes.

## 3. Results and discussion

### 3.1. Morphological characterization

Fig. 3(a,b) depicts the atomic force microscopy (AFM) measurements of the devices following CMP for the Damascene and subtractive approaches, and Fig. 3(c) compares the dishing measured by AFM on different devices over a 100-mm wafer. The Damascene approach exhibits a higher dishing, of  $11 \pm 1$  nm, while the subtractive process has a dishing of  $3 \pm 1.5$  nm. Although the subtractive technique has better planarity, it is essential to keep in mind that the EPD is also more difficult to find due to the low selectivity. Furthermore, the low dishing observed correlates with the low selectivity, as both materials are polished at a similar rate. For the Damascene approach, uniform dishing is observed over the wafer. In contrast, for the subtractive approach, a



**Fig. 3.** Topographical comparison: (a) AFM measurement after CMP of the Damascene approach (b) and the subtractive approaches. (c) Dishing comparison across a 4-in. wafer, highlighting Damascene's higher dishing versus the subtractive approaches.

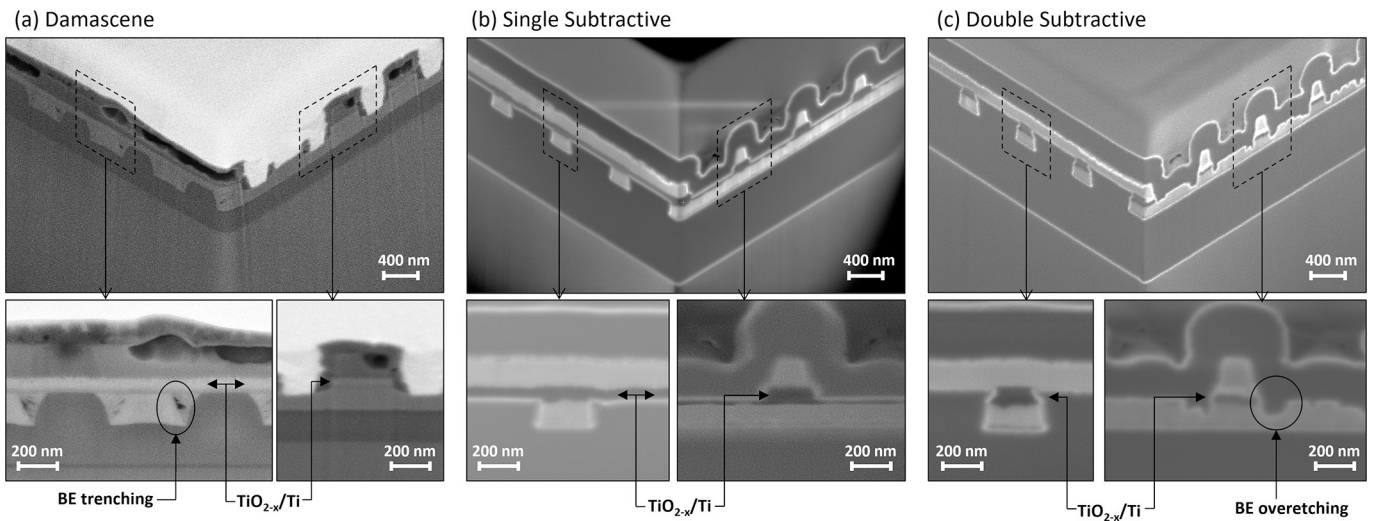
higher polishing rate is observed at the center of the wafer compared to the edges. Note that we didn't observe significant differences between the single and double-subtractive etching since both are SiO<sub>2</sub> polishing stopping on TiN.

Fig. 4 shows Focused ion beam (FIB) microscopic images of the fabricated devices for the three approaches. As shown in Fig. 4(a), the Damascene approach exhibits a trenching effect on the BEs, which is caused by the different orientations of the grain during the deposition of TiN. This creates a defective surface and air gap, which hinders the scaling down of interconnects. A similar trenching effect is also observed in the single and double-subtractive approach but occurs within the dielectric layer. As will be shown in the next section, this effect drastically degrades the performance of Damascene devices when scaling down the electrode. In contrast, in the single and double-subtractive approaches, this is limited by the resolution of the lithography.

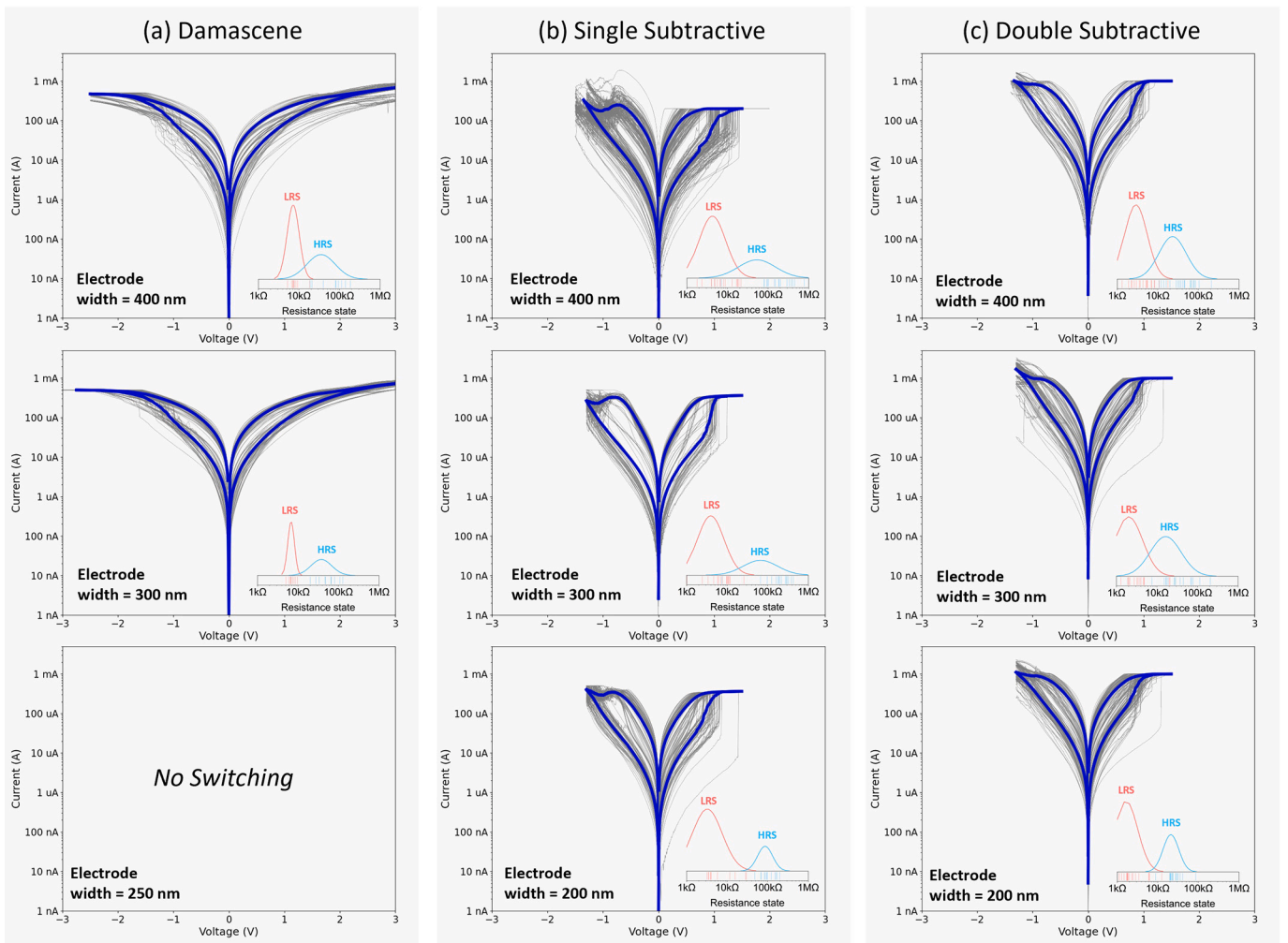
Fig. 4(c) shows the result of the overetching after the second memory patterning in the double-subtractive approach. It results in the memory layer's being patterned only at the intersection of the BE and TE, unlike in the single-subtractive and Damascene approaches, where the memory layer is patterned with the TE. Non-uniform overetching in the BE can be observed close to the intersection. This originates from the chlorine-based gases used to etch the memory stack, which also etch the Al/TiN of the BE. This could be improved by using an etching stop layer between the Al and the TiN with a metallic layer that sustained chlorine gases like W.

### 3.2. Electrical characterization

The devices performances for the three approaches were studied through current–voltage (*I*–*V*) characteristics. The impact of varying the widths of the electrodes was also investigated. For each approach and device dimension, 20 devices were tested by applying 5 bidirectional voltage sweeps. The high resistance state (HRS) and low resistance state (LRS) are defined at 0.2 V. A switching cycle occurs when the



**Fig. 4.** Cross-sectional comparison: (a) FIB cross-section of the Damascene process highlighting trenching effect. (b) FIB for the single-subtractive showing a cleaner etch profile, and (c) FIB for the double-subtractive demonstrating the results of the second etching with distinct memory layer patterning at the electrode intersections.



**Fig. 5.** I–V Characteristics for (a) Damascene, (b) single, and (c) double-subtractive approaches, showing mean cycling curves for devices with different width in blue and corresponding HRS/LRS histogram inset. Damascene devices exhibit higher SET/RESET voltages (2.5/3 V) compared to the subtractive approaches (1/1.3 V), attributed to higher TiN electrode resistance for Damascene. Damascene shows lower ratios, with significant degradation below a width of 300 nm due to the trenching effect. The best performance is seen in the single-subtractive approach. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

device transitions from HRS to LRS with a 2:1 ratio. If the transitions do not meet this ratio, the device is not considered to have switched during that cycle. A device is only considered to be cycling if it undergoes two or more successful transitions. Otherwise, the device is considered faulty.

Fig. 5(a–c) shows the I–V switching cycle for devices with electrodes from 400 to 200 nm wide. The mean characteristic of cycling devices is shown in blue. The single and double-subtractive approaches have similar SET/RESET voltages of approximately 1/1.3 V. For Damascene, the SET/RESET voltage was approximately 2.5/3 V. The higher switching voltage of Damascene is explained by the higher voltage drop along the TiN electrodes owing to their higher resistance. Fig. 5(a–c) inset shows the HRS and LRS histogram for each cycling device for the different approaches and dimensions. The Damascene approach exhibits a lower HRS/LRS ratio with an LRS and HRS of approximately 7 k $\Omega$  and 50 k $\Omega$ , respectively. For electrodes with widths less than 300 nm, none of the tested devices exhibits a cycling behavior. This can be explained by the trenching effect caused by the filling of the TiN inside the SiN trenches, showing that the trenching effect is the limiting factor for the scaling down, whereas, for the single and double-subtractive approaches, the scaling down is limited by the lithography resolution. The best ratio observed in this study was for the single-subtractive approach with an electrode width of 300 nm and a ratio of 35. The second-best ratio is with the same approach with an electrode width of 200 nm with a ratio of 20, but also with a lower device-to-device variability.

Since the active layer is the same for all three approaches, the lower performance in the Damascene can be explained by the trenching effect. For the double-subtractive approach, the differences can arise from the process flow. In the double-subtractive process, Al/TiN BEs and Al<sub>2</sub>O<sub>3</sub>/TiO<sub>2-x</sub>/Ti/TiN memory stacks were subsequently deposited without any other fabrication steps. In the single-subtractive process, before the deposition of the memory stack, the SiO<sub>2</sub> surface was polished by CMP and stopped on the TiN layer. The overpolishing of the CMP on the TiN reduces its roughness. This could indicate that the improvement of the roughness of the interface between the BE and memory stack improves the performance of the device.

#### 4. Conclusion and perspectives

This study demonstrates that Damascene and subtractive approaches are viable for integrating resistive memory. The low planarity below 10 nm, obtained after the CMP process, shows that the devices can be integrated inside the BEOL level of interconnects. Moreover, it enhances the stacking of the devices on top of each other, enabling 3D crossbar arrays.

The electrical measurements obtained are consistent with the current state-of-the-art performance for TiO<sub>x</sub>-based resistive memory [7]. The Damascene approach suffers from worse electrical performance in terms of the SET/RESET voltage and the HRS/LRS ratio. The trenching effect and the formation of void cavities degrade the interface between the bottom electrode and the memory, limiting the scalability of the technology, as shown by the electrical measurements. In contrast, the subtractive approaches have been shown to have certain advantages since they allow a higher aspect ratio, critical for reducing access resistance and increasing the number of memories in a single passive crossbar [2]. In addition, the subtractive approaches allow better metal stack optimization. Unlike the Damascene process, where the polishing of the metal limits the choices of the material for the BE, the subtractive etch process is compatible with the use of various materials. For example, the use of an Al layer beneath the TiN in the subtractive approaches decreases the access resistance and improves the conductance. These approaches present complexities in controlling the EPD. However, there is potential for further optimization in this regard, indicating that these challenges can be addressed in future iterations of the process. The single-subtractive approach achieves the best performance: for an electrode width of 300 nm, we obtain an HRS/LRS around 250/7 k $\Omega$ .

Although the double-subtractive approach demonstrated worse performance in this study, its process flow allowed the deposition of MIM memory without breaking the vacuum. This could lead to better interfaces between the memory stack and electrodes. Moreover, this approach has shown promising results at cryogenic temperatures for quantum applications [27]. Finally, drawing inspiration from the Top-Via subtractive approach [11], the electrode line could be defined with a first lithography mask, followed by a second mask to define pillar-shaped memory. The same CMP process used in both subtractive approaches can be used, as shown in this study [28]. This allows excellent control of the sizes of the memory and electrodes, although with an additional lithography mask compared to the double-subtractive approach.

#### Declaration of generative ai and ai-assisted technologies in the writing process

During the preparation of this work, the authors used ChatGPT 4 in order to aid in refining the phrasing and rectifying typographical errors. After using this tool/service, the authors reviewed and edited the content as needed and take(s) full responsibility for the content of the publication.

#### Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

#### Data availability

Data will be made available on request.

#### Acknowledgments

This work was supported by the Natural Sciences and Engineering Research Council of Canada (NSERC) HIDATA project 506289-2017 and Mitacs Accelerate program IT19472.

#### Appendix A. Supplementary data

Supplementary data to this article can be found online at <https://doi.org/10.1016/j.mne.2024.100251>.

#### References

- [1] S.S. Varshita Gupta, Shagun Kapur, A. Grover, Resistive random access memory: a review of device challenges, IETE Tech. Rev. 37 (2020) 377–390, <https://doi.org/10.1080/02564602.2019.1629341>.
- [2] A. Amirsoleimani, F. Alibart, V. Yon, J. Xu, M.R. Pashouhandeh, S. Ecoffey, Y. Beilliard, R. Genov, D. Drouin, In-memory vector-matrix multiplication in monolithic complementary metal–oxide–semiconductor–memristor integrated circuits: design choices, challenges, and perspectives, Adv. Intell. Syst. 2 (2020) 2000115. <https://onlinelibrary.wiley.com/doi/pdf/10.1002/aisy.202000115>.
- [3] T. Zanotti, C. Zambelli, F.M. Puglisi, V. Milo, E. Pérez, M.K. Mahadevaiah, O. G. Ossorio, C. Wenger, P. Pavan, P. Olivo, D. Ielmini, Reliability of logic-in-memory circuits in resistive memory arrays, IEEE Trans. Electron Devices 67 (2020) 4611–4615.
- [4] C.-X. Xue, T.-Y. Huang, J.-S. Liu, C. Ting-Wei, H.-Y. Kao, J.-H. Wang, T.-W. Liu, S.-Y. Wei, S.-P. Huang, W.-C. Wei, Y.-R. Chen, T.-H. Hsu, Y.-K. Chen, Y.-C. Lo, T.-H. Wen, C.-C. Lo, R.-S. Liu, C.-C. Hsieh, K.-T. Tang, M.-F. Chang, 15.4 a 22nm 2mb reram compute-in-memory macro with 121-28tops/w for multibit mac computing for tiny ai edge devices, 2020, pp. 244–246.
- [5] P. Yao, H. Wu, B. Gao, J. Tang, Q. Zhang, W. Zhang, J.J. Yang, H. Qian, Fully hardware-implemented memristor convolutional neural network, Nature 577 (2020) 641–646.
- [6] F. Cai, J.M. Correll, S.H. Lee, Y. Lim, V. Bothra, Z. Zhang, M.P. Flynn, W.D. Lu, A fully integrated reprogrammable memristor–cmos system for efficient multiply–accumulate operations, Nature Electronics 2 (2019) 290–299.
- [7] H. Kim, M.R. Mahmoodi, H. Nili, D.B. Strukov, 4K-memristor analog-grade passive crossbar circuit, Nat. Commun. 12 (2021) 5198.

- [8] G. Banerjee, R. Rhoades, Chemical mechanical planarization historical review and future direction, *ECS Trans.* 13 (2008), <https://doi.org/10.1149/1.2912973>.
- [9] Microelectronic applications of chemical mechanical planarization. <https://www.wiley.com/enus/Microelectronic+Applications+of+Chemical+Mechanical+Planarizationp-9780470180891>, 2024. Accessed on 2023-11-24.
- [10] G. Murdoch, M. O'Toole, G. Marti, A. Pokhrel, D. Tsvetanova, S. Decoster, S. Kundu, Y. Oniki, A. Thiam, Q. Le, O. Varela Pedreira, A. Lesniewska, G. Martinez-Alanis, S. Park, Z. Tokei, First demonstration of two metal level semi-damascene interconnects with fully self-aligned vias at 18mp, in: 2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), 2022, pp. 1–2.
- [11] K. Motoyama, D. Metzler, C. Park, N. Lanzillo, L. Zou, S. Ghosh, K. Choi, A novel integration scheme for self-aligned Ru topvia as post-Cu alternative metal interconnects, in: 2023 IEEE International Interconnect Technology Conference (IITC) and IEEE Materials for Advanced Metallization Conference (MAM)(IITC/MAM), 2023, pp. 1–3.
- [12] F. Alibart, L. Gao, B.D. Hoskins, D.B. Strukov, High precision tuning of state for memristive devices by adaptable variation-tolerant algorithm, *Nanotechnology* 23 (2012) 075201.
- [13] F. Alibart, E. Zamanidoost, D.B. Strukov, Pattern classification by memristive crossbar circuits using ex situ and in situ training, *Nat. Commun.* 4 (2013), <https://doi.org/10.1038/ncomms3072>.
- [14] A. El Mesoudy, G. Lamri, R. Dawant, J. Arias-Zapata, P. Gliech, Y. Beilliard, S. Ecoffey, A. Ruediger, F. Alibart, D. Drouin, Fully CMOS-compatible passive TiO<sub>2</sub>-based memristor crossbars for in-memory computing, *Microelectron. Eng.* 255 (2022) 111706.
- [15] F.M. Bayat, M. Prezioso, B. Chakrabarti, H. Nili, I. Kataeva, D. Strukov, Implementation of multilayer perceptron network with highly uniform passive memristive crossbar circuits, *Nat. Commun.* 9 (2018), <https://doi.org/10.1038/s41467-018-04482-4>.
- [16] A. El Mesoudy, D. Machon, A. Ruediger, A. Jaouad, F. Alibart, S. Ecoffey, D. Drouin, Band gap narrowing induced by oxygen vacancies in reactively sputtered TiO<sub>2</sub> thin films, *Thin Solid Films* 769 (2023) 139737.
- [17] H.J. Kim, Abrasive for chemical mechanical polishing, in: *Abrasive Technology-Characteristics and Applications*, IntechOpen, 2018, pp. 183–201.
- [18] D.-H. Feng, R.-B. Wang, A.-X. Xu, F. Xu, W.-L. Wang, W.-L. Liu, Z.-T. Song, Mechanism of titanium-nitride chemical mechanical polishing, *Chin. Phys. B* 30 (2021) 028301.
- [19] M. Krishnan, J.W. Nalaskowski, L.M. Cook, Chemical mechanical planarization: slurry chemistry, materials, and mechanisms, *Chem. Rev.* 110 (2010) 178–204.
- [20] T. Hoshino, Y. Kurata, Y. Terasaki, K. Susa, Mechanism of polishing of SiO<sub>2</sub> films by CeO<sub>2</sub> particles, *J. Non Cryst. Solids* 283 (2001) 129–136.
- [21] R. Manivannan, S. Ramanathan, The effect of hydrogen peroxide on polishing removal rate in CMP with various abrasives, *Appl. Surf. Sci.* 255 (2009) 3764–3768.
- [22] J.C. Yang, D. Oh, G. Lee, C. Song, T. Kim, Step height removal mechanism of chemical mechanical planarization (CMP) for sub-nano-surface finish, *Wear* 268 (2010) 505–510.
- [25] D. Lim, J. Ahn, H. Park, J. Shin, The effect of CeO<sub>2</sub> abrasive size on dishing and step height reduction of silicon oxide film in STI-CMP, *Surf. Coat. Technol.* 200 (2005) 1751–1754.
- [26] K.M. Robinson, K. DeVriendt, D.R. Evans, Integration issues of CMP, in: M.R. Oliver (Ed.), *Chemical-Mechanical Planarization of Semiconductor Materials*, Springer-Verlag, Berlin, 2004, pp. 351–417.
- [27] P.-A. Mouny, R. Dawant, B. Galaup, S. Ecoffey, M. Pioro-Ladrière, Y. Beilliard, D. Drouin, Analog programming of CMOS-compatible Al<sub>2</sub>O<sub>3</sub>/TiO<sub>2</sub>x memristor at 4.2K after metal-insulator transition suppression by cryogenic reforming, *Applied Physics Letters* 123 (2023) 163505. <https://pubs.aip.org/aip/apl/articlepdf/doi/10.1063/5.0170058/18174487/16350515.0170058.pdf>.
- [28] R. Dawant, S. Ecoffey, D. Drouin, Multiple material stack grayscale patterning using electron-beam lithography and a single plasma etching step, *J. Vac. Sci. Technol. B* 40 (2022) 062603. <https://pubs.aip.org/avs/jvb/articlepdf/doi/10.1116/6.0002116/16571016/062603online.pdf>.